AN1051

TRANSMISSION LINE EFFECTS IN PCB APPLICATIONS

A thorough digital design must transcend the "1" and "0" scope of strictly digital considerations and venture into the traditionally analog world of transmission lines. The effects of transmission lines are evident in all interconnections. However, with the advent of devices possessing extremely fast rise and fall times, these effects are more pronounced. The results of these effects, delays or ringing along an interconnection, can cause unpredictable behavior. To minimize these undesirable events, additional care is required during the design of interconnections and termination. Figure 1 illustrates stair-stepping delays and ringing.

The basic guideline used to determine if a printed circuit board (PCB) trace needs to be examined for transmission line effects is that, if the smaller of the driving device's rise or fall time is less than the twice the time required for a switching wave to propagate through a trace, the transmission line effects are not masked during the rise or fall time of the driving device. The factor of twice the propagation time through a trace is not as arbitrary as it might seem; this factor allows for the switching wave to be transmitted from the driving device, travel through the PCB trace to the receiving device, reflect off the receiving device, and return to the driving device. With this guideline established, the rise and fall times and propagation times of a trace become paramount in transmission line analysis.

1. QUAD DESIGN's Transmission Line Calculator (TLC) 1385 Del Norte Rd., Camarillo, California
2. PARASITIC PARAMETERS is a registered trademark of Pacific Numerix Corp., 1200 Prospect St., Suite 300, La Jolla, California.
3. Viewsim System Development (View/SD) is a subset of Workview Series II which are registered trademarks of Viewlogic Systems Inc., 293 Boston Post Rd. West, Marlborough, MA.
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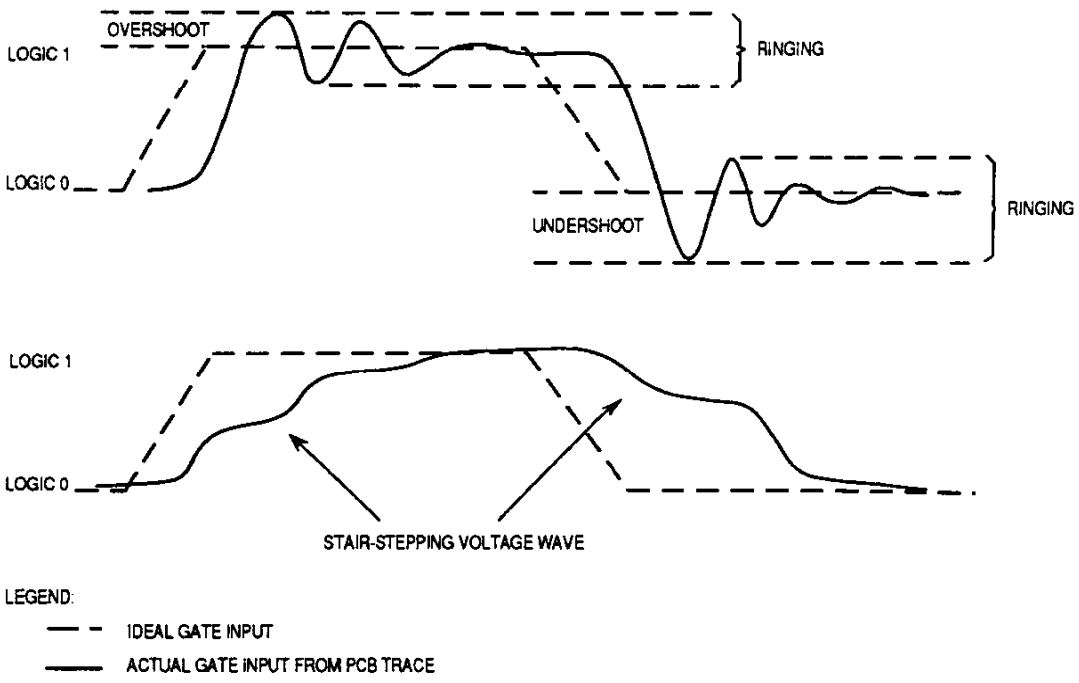


Figure 1. Transmission Line Effects

As devices have been designed to run at higher speeds, their rise and fall times have diminished. Propagation times through a PCB trace depend on the PCB materials and the routing and loading of the trace. Conventional PCB materials have not changed to sustain performance at the faster rise and fall times of driving devices. This situation, as well as the fact that routing and loading can vary greatly from trace to trace, has elevated the importance of investigating PCB traces for transmission line effects.

The lumped capacitive load model shown in many data books is not sufficient for a detailed examination of transmission line effects in PCBs.

Two key elements to consider in transmission line analysis are the PCB traces' characteristic impedance, Z_O, and propagation delay, T_{PD}. The characteristic impedance is the ratio of the voltage to the current in a circuit; thus it describes what current and voltage parameters the driving and receiving devices connected to a trace will experience. Mismatches in impedance between segments of the trace and devices connected to the trace cause reflections, which result in performance-limiting ringing and delays. The propagation delay is important

because it predicts if the effects of these reflections will be hidden during the rise and fall times of a circuit. To account for these elements, more detailed hand-analysis methods, such as the lattice diagram and the Bergeron plot methods presented in this document, are required. The lattice diagram requires the following information: the rise and fall times of the driving devices, the output impedances of the driving devices, the input impedances of the receiving devices, and the capacitive loading values of the receiving devices. The Bergeron plot method requires the output voltage versus current curves for the driving devices and the input voltage versus current curves and the capacitive loading values of the receiving devices. A complete study also requires information about the PCB, such as the dielectric constant for the insulating materials used, the cross-section trace geometry, and the trace length.

Transmission line effects need to be examined prior to final PCB layout. Not all scenarios can be improved by adding termination. Occasionally, a trace with several segments and loads will have too much delay associated with the reflections and the characteristics of the driving device. In some cases, termination may absorb the reflections, but in other cases, it may overload the driving device, preventing it from operating at its prescribed rate. Hand analysis helps to highlight potential problem areas and can provide general rules used in PCB layout once a system designer gains expertise with an output driver type, but, to account for complex routing patterns, computer programs with transmission line and layout emphasis provide more detailed solutions than hand analysis. More comprehensive solutions using computer programs that provide graphical analysis are available, such as QUAD DESIGN's TLC[1], Pacific Numerix's PARASITIC EXTRACTOR™[2], Viewlogic's Viewsim/SD™[3], Quantic Laboratories Greenfield®[4] and Racal-Redac's Saber/CADAT™[5]. The Simulation Program with Integrated Circuit Emphasis (SPICE) also has provisions for transmission line analysis. It is important that the designer knows basic transmission line theory to evaluate these programs' limitations and features.

Motorola understands the importance and complexity of this issue and is developing a solution that includes a tutorial on basic transmission line theory, a set of enhanced input and output electrical characteristics , and the release of models of the M88000 Family output buffers for use in transmission line programs. Solutions, from hand-analysis methods to results of transmission line programs, are useful in predicting transmission line effects, which need to be correlated with the hardware to verify the basic observations from the paper calculations and simulations. This application note serves as the tutorial intended to emphasize the importance of understanding transmission line effects in the application of PCBs. It covers the following subjects: PCB traces as transmission lines, transmission line analysis methods, termination schemes, general notes concerning layout, and examples for loaded traces and

termination. Discussions of termination and examples are presented for exercise only and do not imply behavior of any Motorola devices.

Some techniques promoted in this document have been in practice over 20 years in ECL designs. The premier source for ECL designs is the *MECL Design Handbook* (see Reference 1). Since the techniques presented there are designed for ECL applications, they do not automatically work for all CMOS and TTL applications. CMOS and TTL outputs are different from ECL outputs in that ECL has similar output impedances for the low-to-high-driven and the high-to-low-driven cases; whereas, CMOS and TTL output impedances often vary by an order of magnitude from their low-to-high-driven and high-to-low-driven cases. Also, many CMOS and TTL outputs drive 5-V swings in less than 2 ns (some actually reach down into the 500-ps range for rise and fall times). ECL outputs drive a 1-V swing in roughly 1 ns. These differences require close examination of the basic, entrenched termination schemes for ECL before they are used with CMOS and TTL.

PCB TRACES

The following paragraphs discuss PCB traces as transmission lines, the four trace types, and device loading.

PCB Traces as Transmission Lines

The key factor in determining if a trace should be treated as a transmission line rather than a lumped load is the relationship between the driving device's rise or fall time and the propagation delay of the signal through the trace. Specifically, the trace should be analyzed as a transmission line if

$$2 \times T_{PD} \times \text{trace length} > T_R \text{ or } T_F \text{ (minimum of the two)} \quad (1)$$

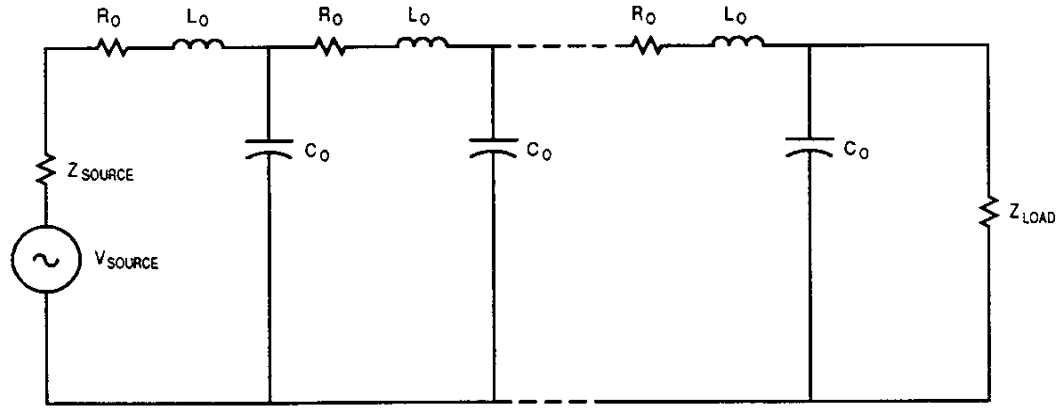
T_{PD} is the unit propagation delay of the signal, usually given in nanoseconds per unit length. T_R and T_F are the rise and fall times of the driving device. Note that the fastest of the rise and fall time values should be used. The high-level interpretation of Equation (1) is that, if the round-trip time for the switching waveform is greater than the rise or fall time of the driving device, the settling of the transmission line effects are not hidden during the rise and fall times of the driving device.

PCB traces have resistive, inductive, and capacitive effects distributed throughout them. These characteristics are used to develop transmission line models, and the basic means for approximating the distributed effects is a

lumped load model. Figure 2 shows a transmission line modeled in lumped, constant terms, using the intrinsic resistance, inductance, and capacitance of a trace. This representation is reduced to a transmission line circuit that uses the characteristic impedance (Z_O) and propagation delay (T_{PD}) values to describe the trace. Referring to Figure 2, the effects of the intrinsic resistance (R_O) on Z_O are negligible, leaving only the effects of L_O and C_O to be considered in the calculation of the characteristic impedance and propagation delay per unit length:

$$Z_O = \sqrt{(L_O/C_O)}\ \Omega \quad (2)$$

$$T_{PD} = \sqrt{(L_O \times C_O)}\ \text{ns/length} \quad (3)$$



NOTE:

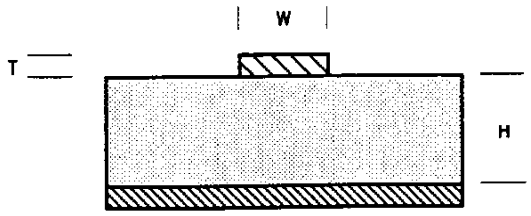
V_{SOURCE} = SWITCHING VOLTAGE SUPPLY
Z_{SOURCE} = OUTPUT IMPEDANCE OF VOLTAGE SUPPLY
R_O = INTRINSIC RESISTANCE OF TRANSMISSION LINE
L_O = INTRINSIC INDUCTANCE OF TRANSMISSION LINE
C_O = INTRINSIC CAPACITANCE OF TRANSMISSION LINE
Z_{LOAD} = LOAD IMPEDANCE

Figure 2. Lumped Transmission Line Approximation

If the intrinsic capacitance and inductance are known, they can be used in Equations (2) and (3). Usually, the propagation delay and the characteristic impedance are calculated from cross-section geometries and dielectric materials used in the PCB traces. The equations using the geometries and materials are based on Equations (2) and (3), but then require considerations that treat the traces as if they are operating in the transverse electromagnetic mode. If more information is desired for that derivation, see Reference 1. For this discussion, only multilayer board types (microstrip and stripline) are analyzed. For wire-wrapped applications, consult Reference 1.

PCB Trace Types

The two basic trace types are the microstrip and stripline. Each type can be modified to form derivatives such as the embedded microstrip and the dual stripline configurations. Cross-section diagrams of these trace types are shown in Figure 3.

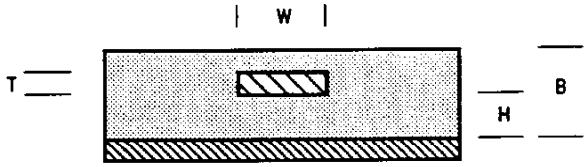


$$Z_O = \frac{87}{\sqrt{E_R + 1.41}} \ln\left\{\frac{5.98\ H}{0.8\ W + T}\right\}$$

$$T_{PD} = 1.017\sqrt{0.475\ E_R + 0.67}$$

WHERE:
E_R = DIELECTRIC CONSTANT
H = DIELECTRIC THICKNESS
T = TRACE THICKNESS
W = TRACE WIDTH

(a) Surface Microstrip



$$Z_O = \frac{K}{\sqrt{0.805\ E_R + 2}} \ln\left\{\frac{5.98\ H}{0.8\ W + T}\right\}$$

$$T_{PD} = 1.017\sqrt{0.475\ E_R + 0.67}$$

OR:

$$Z_O = \frac{87}{\sqrt{E_R' + 1.41}} \ln\left\{\frac{5.98\ H}{0.8\ W + T}\right\}$$

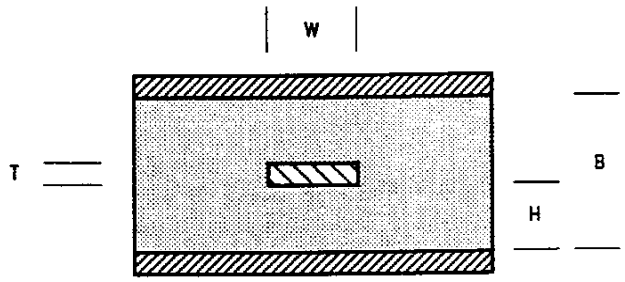
WHERE: $E_R' = E_R \left\{1 - e^{\left(\frac{-1.55\ B}{H}\right)}\right\}$

$$T_{PD} = 1.017\sqrt{0.475\ E_R + 0.67}$$

WHERE: $60 \le K \le 65$
E_R = DIELECTRIC CONSTANT
H = DIELECTRIC THICKNESS BETWEEN TRACE AND POWER/GROUND PLANE
B = OVERALL DIELECTRIC THICKNESS
T = TRACE THICKNESS
W = TRACE WIDTH

(b) Embedded Microstrip

Figure 3. PCB Trace Types (Sheet 1 of 3)



$$Z_O = \frac{60}{\sqrt{E_R}} \ln\left\{\frac{4B}{0.67\pi W\left(0.8 + \frac{T}{W}\right)}\right\}$$

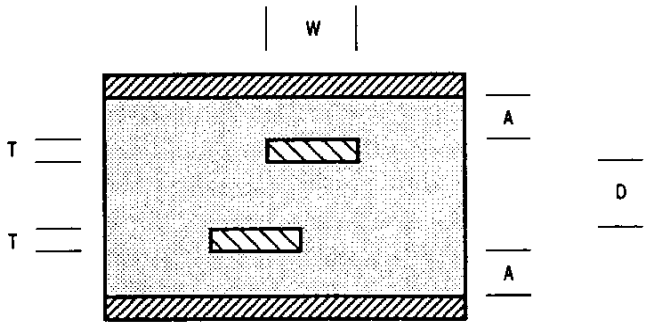
$$T_{PD} = 1.017 \times \sqrt{E_R}$$

WHERE:
E_R = DIELECTRIC CONSTANT
H = DIELECTRIC THICKNESS BETWEEN TRACE AND POWER/GROUND PLANE
B = OVERALL DIELECTRIC THICKNESS
T = TRACE THICKNESS
W = TRACE WIDTH

VALID FOR $\frac{W}{(B-T)} < 0.35$ AND $\frac{T}{B} < 0.25$

(c) Stripline

Figure 3. PCB Trace Types (Sheet 2 of 3)



$$Z_O = \frac{2YZ}{Y+Z} \qquad \text{WHERE } Y = \frac{60}{\sqrt{E_R}} \ln\left\{\frac{8A}{0.67\pi W\left(0.8+\frac{T}{W}\right)}\right\}$$

$$\text{WHERE } Z = \frac{60}{\sqrt{E_R}} \ln\left\{\frac{8(A+D)}{0.67\pi W\left(0.8+\frac{T}{W}\right)}\right\}$$

$$T_{PD} = 1.017 \times \sqrt{E_R}$$

WHERE:
E_R = DIELECTRIC CONSTANT
H = DIELECTRIC THICKNESS BETWEEN TRACE AND POWER/GROUND PLANE
B = OVERALL DIELECTRIC THICKNESS
T = DIELECTRIC THICKNESS BETWEEN TRACES
W = TRACE WIDTH

OR:

$$Z_O = \frac{80\left[1-\left(\frac{A}{4(A+D+T)}\right)\right]}{\sqrt{E_R}} \ln\left\{\frac{1.9(2A+T)}{0.8W+T}\right\}$$

$$T_{PD} = 1.017 \times \sqrt{E_R}$$

WHERE:
E_R = DIELECTRIC CONSTANT
A = DIELECTRIC THICKNESS BETWEEN TRACE AND POWER/GROUND PLANE
B = DIELECTRIC THICKNESS BETWEEN TRACES
T = TRACE THICKNESS
W = TRACE WIDTH

LEGEND:

DIELECTRIC

TRACE

GROUND OR POWER PLANE

(d) Dual Stripline

Figure 3. PCB Trace Types (Sheet 3 of 3)

The most frequently used types of dielectrics are glass-epoxy (G-10) and one of its derivatives (FR-4). The dielectric constants (or more specifically in relation to its derivation, relative permittivity) for G-10 can be characterized generally as 4.5 to 5.0, and the dielectric constant for FR-4 can be characterized as 4.5 to 5.2, although PCB manufacturers have seen values as low as 4.0 for both constants. The dielectric constant varies with frequency; Reference 2 provides a discussion on this. Trace dimensions can vary greatly depending on their applications. For multilayer boards with overall board thicknesses of 0.062 in, dielectric thicknesses of layers range from 0.005–0.016 in. Controlled impedance boards, in which all traces on the board have characteristic impedances within a specified range of several ohms, usually have the controlled characteristic impedance in the range of 55–75 ohms due to constraints on manufacturing PCB traces, such as maximum dielectric thicknesses and minimum trace widths.

Device Loading

When a trace is loaded with devices, inductance and capacitance from the devices add to the trace's inductance and capacitance. Figure 4 illustrates the loading down the line. This loading alters propagation delay and characteristic impedance values as shown in Equations (4) and (5):

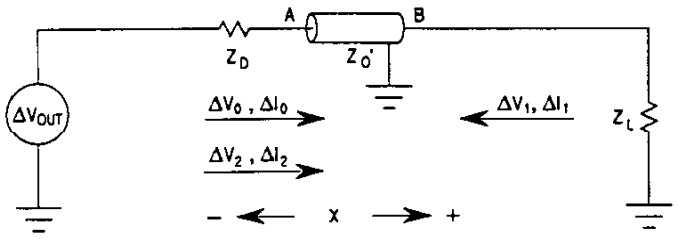
$$T_{PD}' = T_{PD} \times \sqrt{1+(C_D / C_O)} \text{ ns/length} \quad (4)$$

$$Z_O' = Z_O / \sqrt{1+(C_D / C_O)}\ \Omega \quad (5)$$

where C_D is the distributed capacitance of the receiving devices (i.e., total load capacitance/trace length) and C_O is intrinsic capacitance of the trace. Sockets and vias also add to the distributed capacitance (sockets ≈ 2 pF and vias ≈ 0.3–0.8 pF). Since $T_{PD} = \sqrt{L_O \times C_O}$ and $Z_O = \sqrt{L_O / C_O}$, C_O can be calculated as follows:

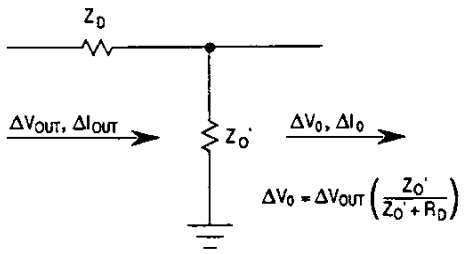
$$C_O = 1000 \times (T_{PD} / Z_O) \text{ pF/length} \quad (6)$$

This loaded propagation delay value must be used when deciding whether a trace should be considered a transmission line ($2 \times T_{PD}' \times$ trace length $> T_R$ or T_F).

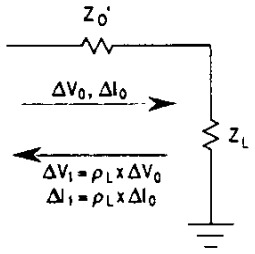


ΔV_{OUT} = VOLTAGE SOURCE, V_{OH} AND V_{OL}
Z_D = OUTPUT IMPEDANCE OF DRIVING DEVICE
Z_L = LOAD IMPEDANCE
ΔV_0 = INCIDENT VOLTAGE
ΔI_0 = INCIDENT CURRENT
A = DRIVING END OF TRACE
B = RECEIVING END OF TRACE
Z_O' = LOADED CHARACTERISTIC IMPEDANCE
ΔV_1 = REFLECTED VOLTAGE AT LOAD
ΔV_2 = REFLECTED VOLTAGE AT DRIVING DEVICE
ΔI_1 = REFLECTED CURRENT AT LOAD
ΔI_2 = REFLECTED CURRENT AT DRIVING DEVICE

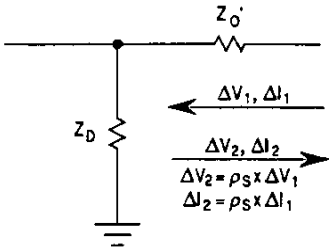
(a) Transmission Line Representation with Z_O' and Load Resistance



(b) Voltage Divider and Incident Wave at Driving Device



(c) Incident Wave and Reflected Wave at Receiving Device



(d) Reflected Wave at Source

NOTE: These are simplified, intermediate representations of the transmission line model.

Figure 4. Simplified Transmission Line Representation

The results of these equations are not as straightforward as they seem. C_D, the distributed capacitance per length of the trace, depends on the capacitive load of the receiving devices, sockets, and vias. To mask transmission line effects, slower rise and fall times are recommended. A heavily loaded trace slows the rise and fall times of the devices due to the increased RC time constant associated with the increased distributed capacitance and the filtering of high-frequency components out of the switching signal. Heavily loaded traces seem advantageous until the loaded trace condition is examined. A high C_D raises the loaded propagation delay and lowers the loaded characteristic impedance. The higher loaded propagation delay value increases the likelihood that transmission line effects will not be masked during the rise and fall times, and a lower loaded characteristic impedance often exaggerates impedance mismatches between the driving device and the PCB trace. Thus, the apparent benefits of a heavily loaded trace are not realized unless the driving device is designed to drive large capacitive loads.

A higher intrinsic capacitance (C_O) reduces the effects of the distributed capacitance (C_D). A higher C_O correlates to a higher unloaded propagation delay. The higher C_O counteracts the higher C_D values, but often the unloaded propagation delay is too high for transmission line effects to be avoided. Examples 1 and 2 in **APPENDIX A TRANSMISSION LINE EXAMPLES** illustrate these considerations. Calculations are performed on microstrip and stripline PCB configurations to demonstrate how loading affects each configuration. The microstrip has lower unloaded propagation delay and intrinsic capacitance values than the stripline. These examples show that the microstrip may be faster than the stripline, but it is affected by loading more than the stripline, which is the consequence of having a lower intrinsic capacitance. In each of these configurations, the best way to limit transmission line effects is to keep PCB traces as short as possible, which lowers the round-trip time of the signal, increasing the likelihood that transmission line effects will be masked during the rise and fall times of the signal.

Loading also alters the characteristic impedance of the trace. As with the loaded propagation delay, a high ratio between the distributed capacitance and the intrinsic capacitance exaggerates the effects of loading on the characteristic impedance. Because $Z_O = \sqrt{L_O / C_O}$ and the load adds capacitance, the loading factor ($\sqrt{1 + C_D / C_O}$) divides in Z_O, and the characteristic impedance is lowered when the trace is loaded. Reflections on a loaded PCB trace, which cause ringing and stair-stepped switching delays are more extreme when the loaded characteristic impedance differs substantially from the driving device's output impedance and the receiving device's input impedance. A complete discussion of these reflections is presented in **LATTICE DIAGRAM**.

TRANSMISSION LINE ANALYSIS TECHNIQUES

After the loaded characteristic impedance and the loaded propagation delay values of the PCB traces are calculated, the interaction between the devices and the trace can be defined. The two basic occurrences are ringing and stair-stepping delays (see Figure 1). Ringing causes unwanted crossings of logic thresholds, which can be detected by receiving devices with inputs that recognize very fast switching events. In cases with severe ringing, undershoot is produced, which can cripple receiving devices by violating the minimum voltage level allowed at their inputs. Delays caused by stair-stepped voltages limit the overall switching speed of an interconnection. Transmission line analysis methods, from hand-analysis methods to sophisticated computer programs, must be able to predict this behavior.

Lattice diagram and Bergeron plot methods are recommended for hand analysis of transmission line effects. The lattice diagram method requires several calculations to derive reflection coefficients, which are then used to determine the amplitude of reflections at points of unequal impedance throughout a transmission line. This method applies well to computer programs. References 1 and 3 provide a complete derivation of this method. The Bergeron plot is a graphic approach requiring little calculation. It uses the current versus voltage curves of the devices tied to the trace as well as the loaded characteristic impedance of the trace to determine voltages at the driving and receiving devices. References 4, 5, and 6 give basic descriptions of this method. These methods provide information necessary to compile voltage versus time plots, which show the severity and occurrence of transmission line effects.

Lattice Diagram

The following explanation of the lattice diagram method is derived from the finite-length transmission line with a resistive load representation (see Figure 4(a)). The first event in this derivation is that a voltage wave (ΔV_{out}) is sent down the line in the positive-X direction (toward the load). At the output of the driving device, the voltage is split in proportion to the ratio of the output impedance of the driving device and the loaded characteristic impedance (see Figure 4(b)). A new voltage (ΔV_0), called the incident voltage, now travels down the transmission line.

Throughout the transmission line portion of this circuit, the voltage-to-current ratio equals the loaded characteristic impedance ($\Delta V_0/\Delta I_0 = Z_O'$). At the load, the voltage-to-current ratio equals the load impedance ($V_L/I_L = Z_L$). At the junction of the transmission line and the load, to satisfy Kirchoff's circuit equations, a new reflected voltage wave traveling in the negative-X direction (toward the driving device) is introduced; the voltage-to-current ratio as it travels down the

transmission line equals the loaded characteristic impedance ($\Delta V_1/\Delta I_1 = Z_O'$). The incident voltages and currents add with the reflected voltages and currents to equal the voltage and current at the load ($V_L = \Delta V_1 + \Delta V_0$ and $I_L = \Delta I_1 + \Delta I_0$). This concept is depicted in Figure 4(c).

The identical situation of accounting for Kirchoff's circuit equations by adding new, reflected voltages and currents occurs at the driving device's output. The voltage and current equations at the driving device's output are derived identically as those at the load, which require that a new voltage and current (ΔV_2 and ΔI_2) be introduced, using the Kirchoff circuit equations to derive voltage and current at the driving device ($V_D/I_D = Z_D$, $V_D = \Delta V_1 + \Delta V_2$, and $I_D = \Delta I_1 + \Delta I_2$). Figure 4(d) is a representation of this concept.

The ratio of the reflected voltage to that of the incident voltage at the load is defined as the load reflection coefficient, ρ_L; the ratio of the reflected voltage and its subsequent reflected voltage at the source is defined as the source reflection coefficient, ρ_S. They are described as follows:

$$\rho_L = \frac{Z_L - Z_o'}{Z_L + Z_O'} \quad (7)$$

$$\rho_S = \frac{Z_D - Z_O'}{Z_D + Z_O'} \quad (8)$$

where Z_L is the impedance at the receiving device's input, Z_D is the impedance at the driving device's output, and Z_O' is the loaded characteristic impedance.

Once computed, the reflection coefficients are used to determine the voltage and current reflected at each discontinuity by multiplying the incoming voltage and current by the reflection coefficients. The voltages and currents traveling into and out of each discontinuity sum to equal the voltages and currents at the discontinuity. If Z_L or $Z_D >> Z_O'$, then the reflected wave is positive; if Z_L or $Z_D << Z_O'$, then the reflected wave is negative. See Figure 5(a) for this representation of the lattice diagram.

The two basic types of transmission line effects are ringing and stair-stepped switching events. When CMOS and TTL devices are the receiving devices because they have large input impedances ($\rho_L \approx 1$), indicating that the full incident wave from the driving device is reflected back to the driving device. The ringing or stair-stepping events depend on ρ_S which is calculated from the driving device's output impedance and the trace's loaded characteristic impedance. Specifically, when $\rho_L \approx 1$, ringing is caused when the loaded characteristic impedance is greater than the driving device's output impedance, resulting in a negative source reflection coefficient and a large initial voltage step; stair-

stepping is present when the loaded characteristic impedance is less than the driving device's output impedance, resulting in a positive source reflection coefficient and a small initial voltage step. Some CMOS or TTL devices have grossly different output impedances for the low-to-high-driven and high-to-low-driven states, which produce ringing in high-to-low switching and stair-stepping delays in low-to-high switching. Termination often reduces ringing while increasing the stair-stepping, requiring the designer to choose which effect is worse and to terminate appropriately. Examples 3–5 in **APPENDIX A TRANSMISSION LINE EXAMPLES** illustrate the effects of loading and termination for transmission line effects.

This derivation of the lattice diagram method illustrates several details concerning transmission line effects. If the load impedance matches the loaded characteristic impedance, there are no reflections after the incident wave arrives at the load, which is the goal of most termination schemes. Also, this derivation uses a single transmission line with discontinuities at the load and driving device only. Often, a loaded trace connected to several devices is approximated in this manner rather than using a separate discontinuity for each device input. This approximate transmission line representation is accurate if the stubs off the main trace are very short (< 1 in) or if the trace is laid out using a daisy-chain format. If the designer is not afraid of a lattice diagram that looks like random molecules bouncing off various surfaces, then the nonapproximate method is straightforward, because the derivation for reflection coefficients at each discontinuity is identical to the derivation of the reflection coefficients at the driving device and receiving device. An example of this multiple discontinuity situation is shown on page 222 of Reference 1. Reference 2 provides an explanation of different layout and loading configurations.

The detailed mathematical representation of the lattice diagram is described as follows:

$$V(t) = \Delta V_0(t) \times \{ U(t - T_{PD}) + \rho_L \times U[t - T_{PD}(2l - X)] + \rho_L \times \rho_S \times U[t - T_{PD}(2l + X)] + \rho_L^2 \times \rho_S \times U[t - T_{PD}(4l - X)] + \rho_L^2 \times \rho_S^2 \times U[t - T_{PD}(4l + X)] + ...\} + V_{INITIAL} \quad (9)$$

where:

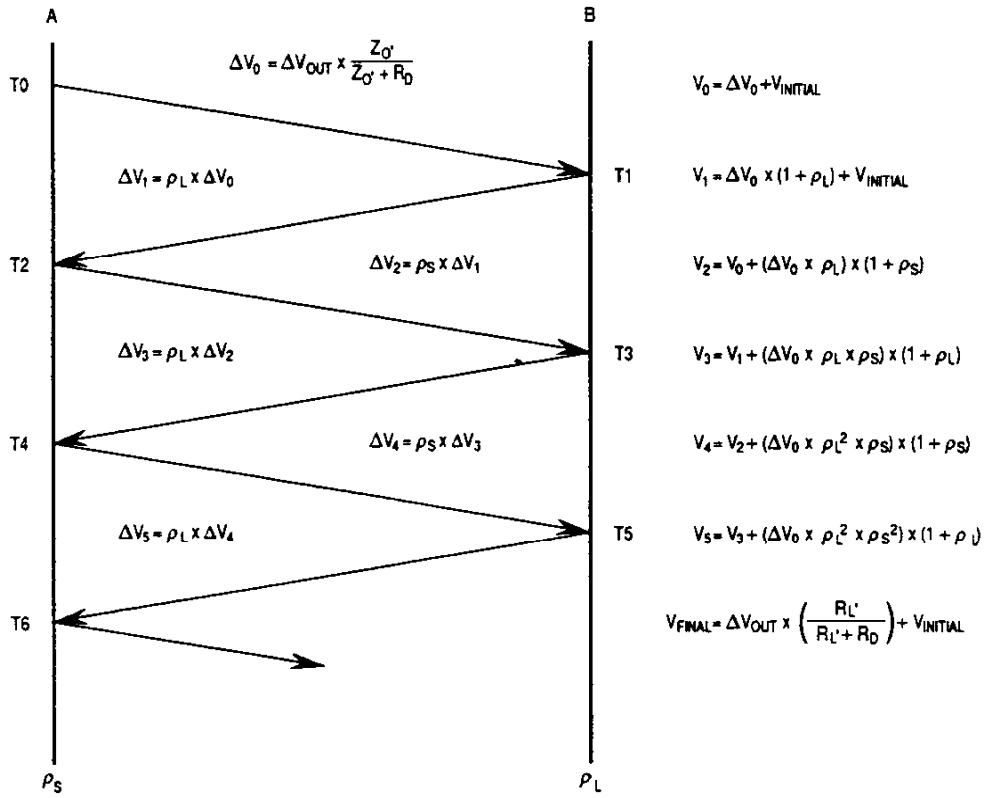
$\Delta V_0(t)$ = voltage at driving device from the voltage divider equation

$$\Delta V_0(t) = \Delta V_{OUT} \times [Z_O' / (Z_O' + Z_D)]$$

where ΔV_{OUT} is the voltage output swing of the driving device, Z_D is the output impedance of the driving device, and Z_O' is the loaded characteristic impedance of the PCB trace.

T_{PD}	= propagation delay of the line
U(t)	= unit step function
l	= length of trace
X	= any point along the trace
ρ_L	= load reflection coefficient
ρ_S	= source reflection coefficient
$V_{INITIAL}$	= quiescent voltage throughout the trace prior to switching

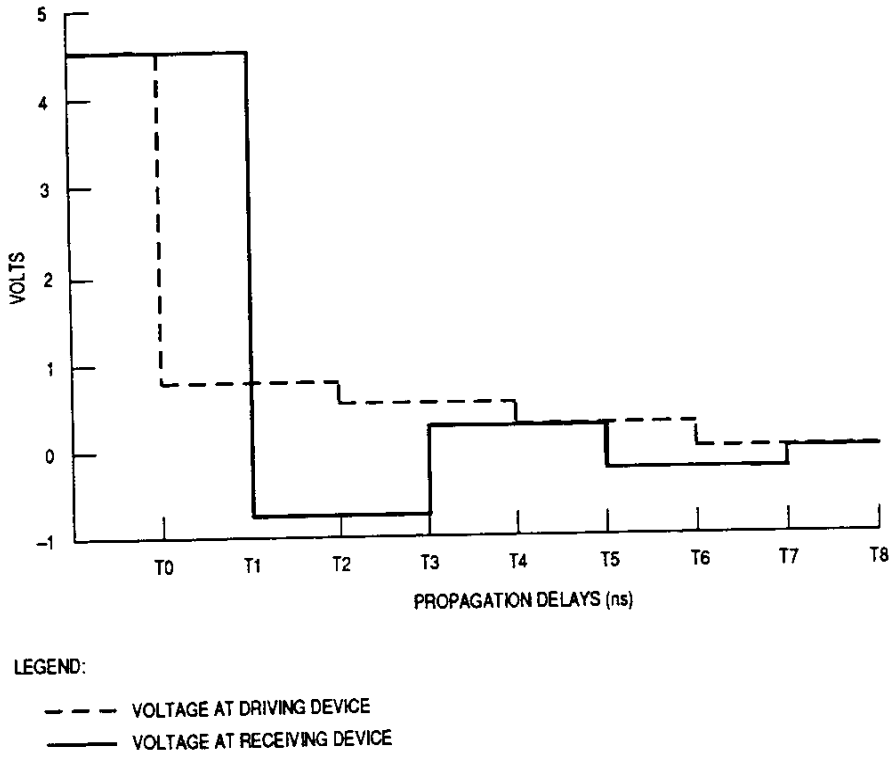
The derivation of this representation is found on page 123 of Reference 1. The simplified representation, complete with equations, is given in Figure 5(a), which shows how to compute the voltages at the driving and receiving ends of a transmission line using reflection coefficients. The vertical line on the left represents the starting position (X = 0) of the incident wave (driving device); whereas, the vertical line on the right represents the end position (X = L) of the incident wave and the point of the first reflected wave (receiving device). The voltages and currents at each endpoint are equal to the voltages and currents flowing into and out of them. The time required to travel the length of the transmission line (PCB trace) is equal to T_{PD}', which are the units of the vertical scale. Units of length are used for the horizontal scale.



NOTE: ρ_L and ρ_S are reflection coefficients and $V_{INITIAL}$ is the steady-state voltage prior to the switching of the gate. Each TD is a propagation delay($T_{PD'}$) in duration. A and B indicate the driving and receiving ends of the trace, respectively.

(a) Lattice Diagram

Figure 5. Lattice Diagram Representation (Sheet 1 of 2)



(b) Voltage Versus Time Plot

Figure 5. Lattice Diagram Representations (Sheet 2 of 2)

The lattice diagram method does make an important assumption in that unless the Z_D and Z_L are specifically given by a data sheet, they have to be calculated over the particular voltage of interest. Not all devices behave linearly over the range of interest. For instance, if a high-to-low transition is to be analyzed, V_{OL}/I_{OL} is used to calculate Z_D for the driving device; for a low-to-high transition, V_{OH}/I_{OH} is used. Frequently, these voltage and current values are given as test conditions or worst-case numbers in a device's specification and do not represent the typical or best-case performance of the device. It is also difficult to find input voltage and current curves, but they are usually approximated by using Schottky diode clamps for CMOS and TTL devices. If the device does not respond linearly and the V_{OUT}/I_{OUT} curves for the driving device and if the V_{IN}/I_{IN} curves for the receiving device are available, then the Bergeron plot method is advised.

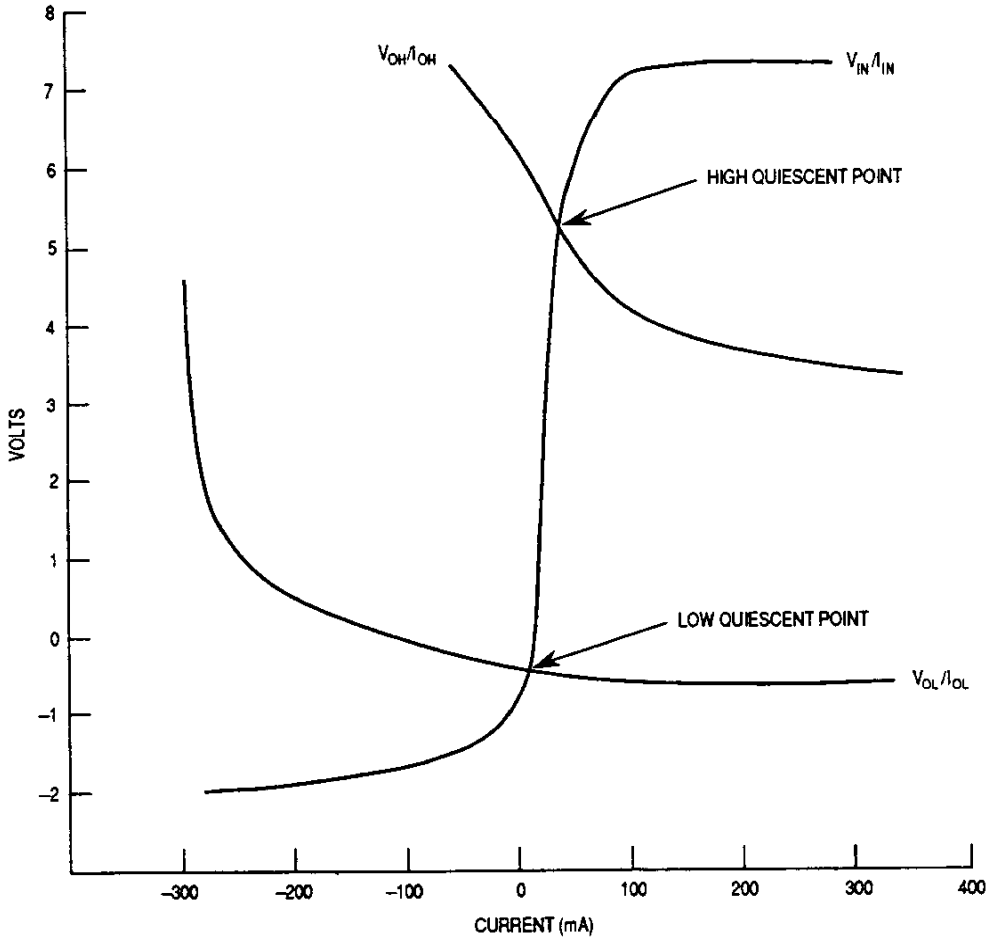
The lattice diagram is translated into a voltage versus time plot to show the response at each end of the transmission line (see Figure 5(b)). The time required for each voltage wave to travel through the trace is T_{PD}'; therefore, each

voltage level is plotted versus T_{PD}' directly from the lattice diagram. In general, the voltage changes at the driving device at time $2n \times T_{PD}'$; the voltage changes at the receiving device at time $(2n + 1) \times T_{PD}'$.

Bergeron Plot

The Bergeron plot provides the same basic information as the lattice diagram (voltage and current versus time) but with fewer calculations. It relies on a graphic means of describing the reflections on the trace.

The current versus voltage curves for the devices connected to the trace and the loaded characteristic impedance of the trace itself are required for this method. The axes are the voltage and current ranges for the driving device and receiving device. The curves plotted on the graph are the V_{OH}/I_{OH} and V_{OL}/I_{OL} of the driving device and the V_{IN}/I_{IN} of the receiving device. See Figure 6 for a basic representation.



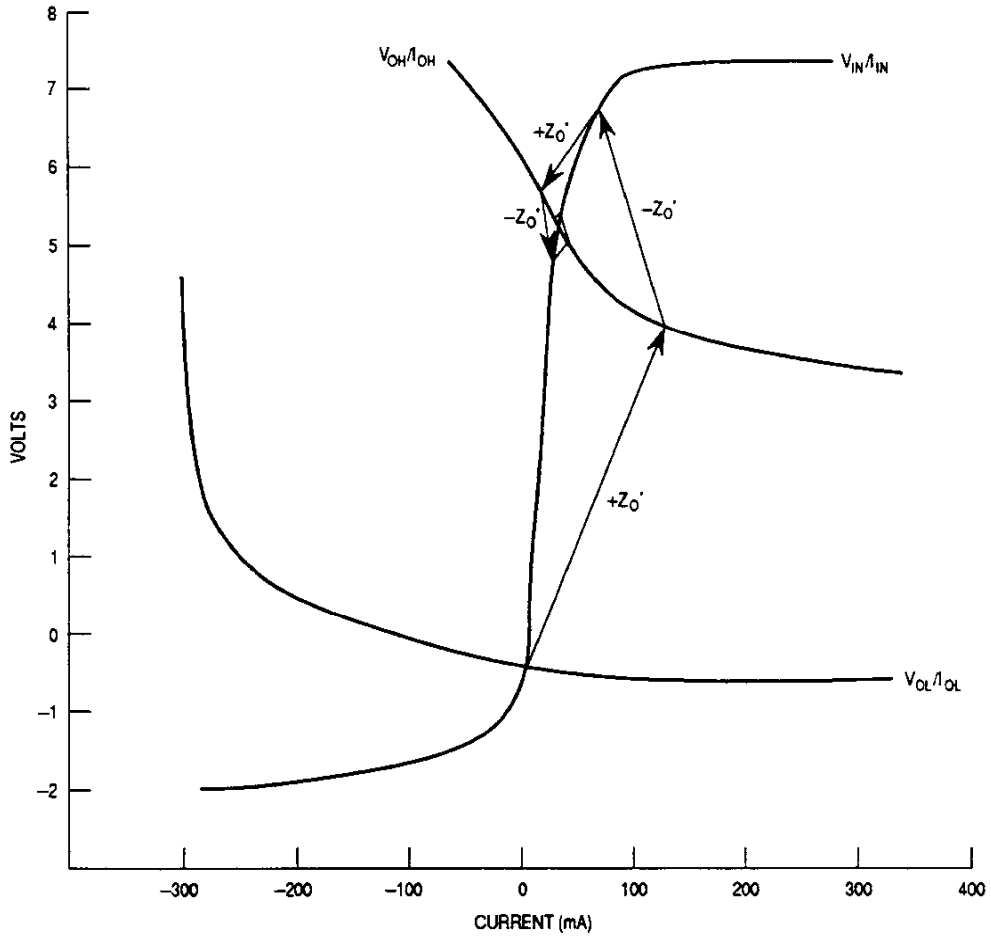
NOTE: V_{OL}/I_{OL} and V_{OH}/I_{OH} are output curves for the driving device; V_{IN}/I_{IN} is the input curve for the receiving device.

Figure 6. Bergeron Plot

The starting point for a transition depends on the quiescent values of the circuit, which are determined by the intersections of the output curves of the driving device with the input curves of the receiving device. These points are the voltage and current values to which the circuit settles in a stable high or low state prior to the transition. In tracking either a high-to-low or a low-to-high transition, a line of slope $\pm Z_O'$ is drawn between the curves. The means for calculating Z_O' is presented in Equation (5).

For the low-to-high transition, the first line is drawn starting at the logic low quiescent point (intersection of V_{OL}/I_{OL} and V_{IN}/I_{IN}) and has a slope of $+Z_O'$ (see Figure 7). The line ends at the V_{OH}/I_{OH} line, with the intersection indicating the

voltage and current values at the output of the driving device and the input of the transmission line.



NOTE: V_{OL}/I_{OL} and V_{OH}/I_{OH} are output curves for the driving device; V_{IN}/I_{IN} is the input curve for the receiving device; and Z_O' is the loaded characteristic impedance of the trace.

Figure 7. Bergeron Plot with Transitions

The second line drawn has a $-Z_O'$ slope from this second intersection point to the V_{IN}/I_{IN} line. This point indicates the current and voltage at the input of the receiving device and the end of the transmission line after one propagation delay since the signal has traveled one trace length.

The third line is drawn from this point to the V_{OH}/I_{OH} line at a slope of $+Z_O'$. This point is the voltage and current at the driving device after two propagation delays since the signal is reflected back to the driving device from the receiving device.

The fourth line on the plot has a slope of $-Z_O'$ and ends at the V_{IN}/I_{IN}. This procedure continues until the logic-high quiescent point is reached.

The high-to-low transition is handled similarly. The starting point is at the logic-high quiescent point. The first line has a $-Z_O'$ slope drawn to the V_{OL}/I_{OL} line. The second line has a $+Z_O'$ slope drawn from the intersection to the V_{IN}/I_{IN} line. In either case, intersection points that lie on a V_{OH}/I_{OH} or V_{OL}/I_{OL} line are values at the driving device; those on the V_{IN}/I_{IN} line are values at the receiving device.

The Bergeron plot results are easily transferred to a voltage versus time plot . The first intersection in the plot gives voltage at time T_0, which is the instant that the driving device switches. The second intersection marks the voltage and current at the receiving device, which occurs at time T_1 (T_{PD}' after T_0). The next change at the driving device occurs at $2T_{PD}'$. In general, the voltage switches at the driving device at time $2n \times T_{PD}'$; whereas, the voltage switches at the receiving device at time $(2n + 1) \times T_{PD}'$. The two graphs can be superimposed if desired. See Figure 5(b) from the lattice diagram illustration.

Basic Bergeron plot exercises are shown in Examples 6 and 7 (see **APPENDIX A TRANSMISSION LINE EXAMPLES**). Examples 8–10 (see **APPENDIX A TRANSMISSION LINE EXAMPLES)** step through series and parallel termination results for various values.

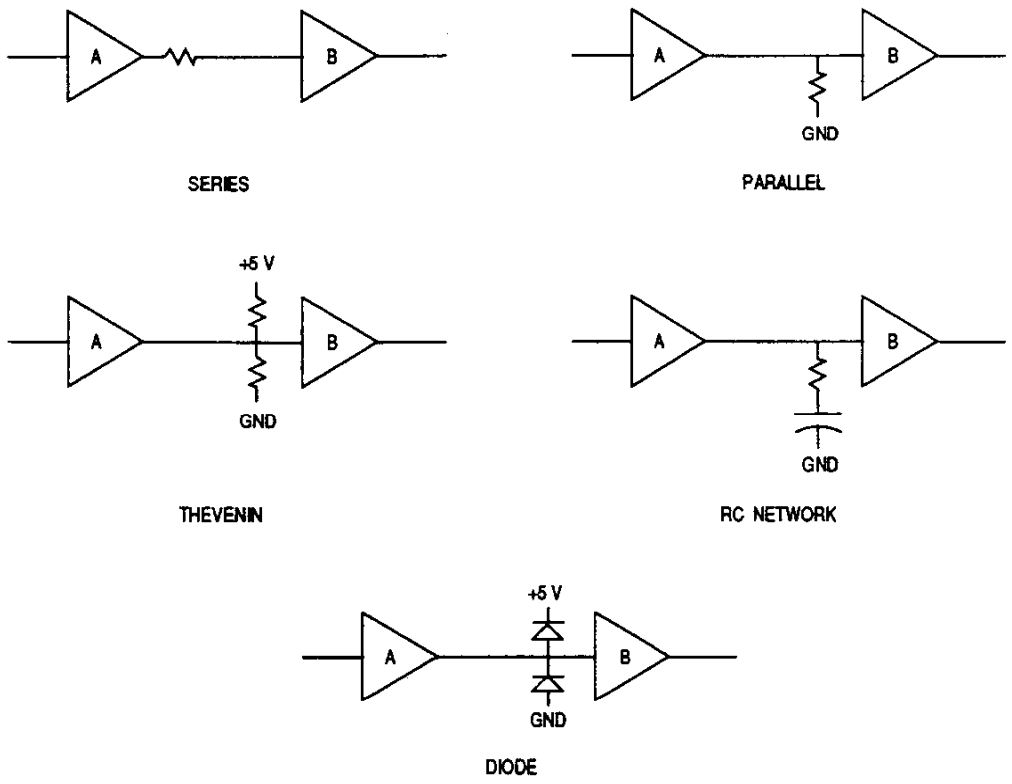
TERMINATIONS

To dissipate the undesired effects of unmatched traces and loads, termination of traces may be utilized. No standard termination works universally due to the complexities of layout geometries, power considerations, component count, and other factors that are discussed in the following paragraphs. In some cases, a combination of these schemes works best. In cases in which a driving device is overloaded, termination adds to the loading of the circuit, further degrading the performance. When the effects of transmission lines rather than overloaded driving devices are dominant, termination may improve performance.

Five of the most frequently used terminations are as follows:

1. Series Termination Resistor
2. Parallel Termination Resistor
3. Thevenin Network
4. RC Network
5. Diode Network

Figure 8 and Table 1 provide a synopsis of these implementations.



NOTES:

1. A – driving device; B- receiving device.
2. Termination near A should be at the driving device's output, and those near B should be the receiving device's input.

Figure 8. Termination Types

Table 1. Termination Types and Their Properties

Termination Type	Added Parts	Delay Added	Power Required	Parts Values	Comments
Series	1	Yes	Low	$R_S = Z_O' - R_D$	Good dc Noise Margin
Parallel	1	Small	High	$R = Z_O'$	Power Consumption Is a Problem
Thevenin	2	Small	High	$R = 2 \times Z_O'$	High Power for CMOS
RC Network	2	Small	Medium	$R = Z_O'$ $C = 300$ pF	Check Bandwidth and Added Capacitance
Diode	2	Small	Low	—	Limits Undershoot; Some Ringing at Diodes

The series termination resistor is preferred when the load is lumped at the end of the trace, when the driving device's output impedance (Z_D) is less than the loaded characteristic impedance of the trace (Z_O'), or when a minimum number of components is required. It is placed near the driving device, and its value is equal to ($Z_O' - Z_D$). When the series resistance and output impedance equal Z_O', as prescribed, the voltage wave is split evenly, causing half of the voltage to be transmitted to the receiving device. A receiving device with a very high input impedance sees the full waveform immediately (due to the reflection at its end of the trace), but the driving device does not see the full waveform until $2 \times T_{PD}'$ (see Example 4). Because devices often have different output impedance values for their high and low cases, choosing a series resistance value is not always straightforward.

Parallel Termination Resistor

The parallel termination resistor utilizes a single resistor whose value equals Z_O' tied to ground, V_{CC}, or +3 V. It adds some delay because the RC time-constant effects of the trace are increased when the termination resistance is included. Its major disadvantage is that it dissipates much dc power since its value is small (50–150 ohms). Examples 5 and 8 illustrate these considerations concerning parallel termination.

Thevenin Network

The Thevenin network connects one resistor to ground and a second resistor to V_{CC}. To avoid settling of the voltage at a point between the high and low logic levels that causes reduced noise margins, careful consideration of the ratio of resistors is required. This technique works well with TTL families, but care is required when using CMOS devices because the switching voltage is at 50% of the waveform. A balanced level near the threshold causes greater power dissipation and potential crossings of the threshold, resulting in unreliable output states. Because this method serves as a pullup and a pulldown termination scheme, it works well for clock signals.

RC Network

The RC network performs well in CMOS and TTL systems. The resistor serves to match the impedance of the trace; the capacitor holds the dc signal component, allowing the ac current to flow to the ground during the switching of logic states. Some delay is presented, but the power dissipation is much less than the parallel scheme. The resistor equals Z_O', and the capacitor is very small (200–600 pF). Their RC time constant must be greater than twice the loaded line propagation delay. This scheme is highly recommended for buses that have similar layouts for all lines (and similar Z_Os) because RC termination networks are available in single-in-line packages (SIPs), which require much less space than a two-discrete-component solution.

Diode Network

The diode termination network is used frequently for termination on differential networks. It limits overshoot to approximately 1 V and has low power dissipation, but the diodes' response at the switching frequency needs to be verified. An important observation is that the energy is not absorbed in this method. Overshoot is limited at each receiver that has these diodes at their inputs, but the overall energy is not absorbed as it is in the resistive terminations; thus, reflections occur throughout the trace.

MISCELLANEOUS FACTORS

Supply voltage, temperature, processes, crosstalk, and layout are factors affecting PCBs. The following paragraphs describe the factors involved.

Supply Voltage

The supply voltage to the devices affects their rise and fall times. Specifically, a higher supply voltage creates faster rise and fall times because the output transistors are being driven by a higher-than-nominal voltage.

Temperature

Temperature alters the performance of the output devices. A higher temperature adds to CMOS devices' propagation delay times, slowing the rise and fall times.

Process

The best-case and worst-case processes can have a large effect on the devices. Generally, best-case factors speed up the switching, and worst-case factors delay the switching. Since devices with best-case processes have faster rise and fall times, they may cause more transmission line situations than typical devices and become the worst-case devices for system designers.

Crosstalk

To reduce transmission line effects, the most compact layout with short traces is advised. However, traces that run close to each other for several inches are suspect to crosstalk problems. To avoid this problem, increased spacing or shielding between traces must be implemented. Increasing space between traces is difficult in dense layouts, which causes crosstalk to be another complicated issue. References 1, 7, 8, and 9 discuss this subject in detail.

Layout

The following general comments relate to PCB layout and components:

1. Evenly distributed devices along a trace are preferred to lumped loads because there are fewer large discontinuities in impedances.

2. Avoid stubs and T's in layout for critical signals, which cause impedance discontinuities. A daisy-chain method is preferred.

3. Sockets and vias add small amounts of capacitance (less than 2 pF and 0.5 pF, respectively). This amount can be added into calculations for distributed capacitance, if desired.

4. One package type of the future is tape-automated bonding (TAB). The pin orientation and package size require less interconnect area, potentially reducing trace lengths and transmission line effects. Another method used for layout is the multichip module, which mounts several devices together on silicon substrates to reduce interconnect area.

5. Although exotic materials are available, they are not normally used in digital PCB construction. Generally, they have lower dielectric constants, meaning their traces have smaller propagation delays. Reference 10 provides a list of these materials.

6. Controlled-impedance PCBs give a predictable environment for transmission line behavior. They can be expensive, but they are recommended for high-performance or prototype applications.

7. Bidirectional signals often use parallel, RC, or Thevenin terminations at both ends of the PCB trace.

8. Multiwire configurations for PCBs have applications in this high-speed world of digital designs. They have lower dielectric constants, providing faster unloaded propagation delay times.

9. A detailed means of accounting for all types of signal integrity issues is described in Reference 11. It focuses on noise budgets that examine powerdrops and tolerances throughout a system

TIME-DOMAIN REFLECTOMETER

Reference 1 promotes a means of lab verification using a time-domain reflectometer (TDR), which is basically a step generator that stimulates a PCB trace for an oscilloscope display to monitor. The TDR is recommended for designers who desire to observe transmission lines on a PCB. Because it has a 1-V swing and uses an unpopulated PCB, some expertise is necessary to translate the results to the CMOS and TTL world.

CONCLUSION

PCB layout is not trivial. A poor layout can prevent a well-simulated conventional design from working properly. With devices achieving faster rise and fall times and PCB materials not improving, the transmission line effects must be resolved, usually by using terminations. This solution involves more components and more power consumed by the printed circuit assembly, but it provides improved performance and greater reliability.

The discussions presented in this document are designed to give a background into transmission line effects. To fully understand these effects, predicted results, whether from hand analysis or computer-aided programs, need to be correlated with actual hardware. This complete investigation reduces the unpredictability associated with transmission line effects.

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11. Tummala and Kymaszewski, *Microelectronics Packaging Handbook*, NY, NY: Van Nostrand Reinhold, 1989.

ADDITIONAL READING

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APPENDIX A
TRANSMISSION LINE EXAMPLES

EXAMPLE 1: LOADED MICROSTRIP

An MC68030 with 3-ns rise and fall times drives a unidirectional 4-in surface microstrip trace with six devices (e.g., FAST family) distributed along the trace. Is termination necessary for transmission line effects?

Microstrip Geometry

Given as W = 0.010 in, T = 0.002 in, H = 0.012 in, and E_R = 4.7.

Calculate Characteristic Impedance and Propagation Delay:

Using the surface microstrip equations in Figure 3(a):

$$Z_O = \frac{87}{\sqrt{E_R + 1.41}} \times \ln\left\{\frac{5.98 \times H}{0.8xW + T}\right\} = \frac{87}{\sqrt{4.7 + 1.41}} \times \ln\left\{\frac{5.98 \times 12}{0.8 \times 10 + 2}\right\} =$$

69.4 Ω

$$T_{PD} = 1.017 \times \sqrt{.475 \times E_R + 0.67} = 1.73 \text{ ns/ft} = 0.144 \text{ ns/in.}$$

Consider Loading

C_D is the distributed capacitance per length of the load, which is the total input capacitance of the receiving devices divided by the length of the trace. The loading of each device is given in its specifications For this case, each C_L = 7 pF. Since there are six devices distributed along the 4-in trace, C_D = 6 x C_L/Trace Length = 42 pF/4 in = 10.5 pF/in.

C_O is the intrinsic capacitance of the trace. $C_O = T_{PD}/Z_O$ = 0.0250 nF/ft =

25.0 pF/ft = 2.08 pF/in.

$T_{PD}' = T_{PD} \times \sqrt{1 + 10.5/2.08}$ = 4.26 ns/ft. This is the new one-way propagation time for the signal from the MC68030.

Transmission Line Effects

If 2 x T_{PD}' x Trace Length ≤ T_R or T_F, then the ringing and other transmission line effects are masked during the rise and fall times, and no termination will be needed.

2 x T_{PD}' x Trace Length = 2 x 4.25 ns/ft x 1/3 ft = 2.83 ns.

T_R and T_F = 3 ns; since 2.83 ≤ 3, no termination is required, but this is a marginal case. Note that, if the guideline promoted by some device manufacturers of 3 x T_{PD}' x Trace Length is used, then termination would be required.

For comparison, if a 69-Ω stripline was used instead of a 69-Ω microstrip, would termination be required?

$T_{PD} = 1.017 \times \sqrt{E_R} = 2.20$ ns/ft.

$C_O = T_{PD}/Z_O = 35$ pF/ft = 2.91 pF/in.

C_D is same as above (= 10.5 pF/in).

$T_{PD}' = T_{PD} \times \sqrt{1 + C_D/C_O} = 4.72$ ns/ft.

2 x T_{PD}' x Trace Length = 2 x 4.72 ns/ft x 1/3 ft = 3.14 ns.

The rise and fall times are 3 ns. Since 3.14 > 3 ns, termination is needed for the 69-Ω stripline case.

In comparison, note that C_O is greater for the stripline, which tends to lessen the effect of loading in the T_{PD}' equation. However, the unloaded T_{PD} is substantially greater for the stripline than the microstrip, and this factor prevents the transmission line effects from being masked during the rise and fall times, according to these equations. Notice that the unloaded propagation delay calculations depend only on E_R, the dielectric constant, and not on the trace geometries.

EXAMPLE 2: LOADED STRIPLINE

An MC88100 with rise and fall times of 2 ns drives four MC88200s distributed over an 8-in stripline trace.

Stripline Geometry

Assume a stripline with B = 0.020 in, W = 0.006 in, T = 0.0014 in, and E_r = 4.6.

From Figure 3(c), the equations for Z_O and T_{PD} for a stripline are:

$$Z_O = \frac{60}{\sqrt{E_R}} \times \ln\left\{\frac{4 \times B}{0.67\pi W \times (0.8 + T/W)}\right\}$$

$$= \frac{60}{\sqrt{4.6}} \times \ln\left\{\frac{4 \times 20}{0.67\pi \times 6 \times (0.8 + 1.4/6)}\right\} = 50.7\ \Omega$$

$$T_{PD} = 1.017 \times \sqrt{E_R} = 2.18 \text{ ns/ft} = 0.182 \text{ ns/in.}$$

Calculate the intrinsic capacitance of the trace:

$$C_O = T_{PD}/Z_O = 0.043 \text{ nF/ft} = 43.0 \text{ pF/ft} = 3.58 \text{ pF/in.}$$

Consider Loading

Each MC88200 has a capacitive load of 15 pF. The total load is 60 pF for the four MC88200s. C_D is the distributed load per length for the trace: C_D = 60 pF/ 8 in = 7.5 pF/in.

$$T_{PD}' = T_{PD} \times \sqrt{1 + C_D/C_O} = 2.18 \times \sqrt{1 + 7.50/3.58} = 3.84 \text{ ns/ft.}$$

Transmission Line Effects

2 x T_{PD}' x Trace Length < T_R or T_F is the condition of interest.

2 x 3.84 ns/ft x 2/3 ft = 5.10 ns. Since this is not less than T_R or T_F (2 ns), termination is recommended to absorb transmission lines effects.

Look at a 50.7-Ω microstrip line loaded similarly.

$$T_{PD} = 1.017 \times \sqrt{0.475E_R + 0.67} = 1.72 \text{ ns/ft.}$$

$C_O = T_{PD}/Z_O = 2.83$ pF/in.

$T_{PD}' = T_{PD} \times \sqrt{1 + C_D/C_O} = 3.29$ ns/ft.

Is this a transmission line? 2 x T_{PD}' x Trace Length = 2 x 3.29 ns/ft x 2/3 ft = 4.38 ns. Since this is greater than T_R or T_F, termination is recommended.

For a trace this long, the rise and fall times are too fast to handle without termination. Trace length does not directly figure into the calculations for T_{PD} or Z_O, but it is an important factor in the relationship that determines if a trace is a transmission line.

EXAMPLE 3: LATTICE DIAGRAM

Chip A is driving an 8-in 90-Ω stripline trace on a glass-epoxy PCB (Er = 4.7) loaded with four devices (chip B) of 15-pF load capacitance each. Chip A has an output low impedance of 20 Ω and an output high impedance of 120 Ω. Chip B has a very large input impedance (100 kΩ). Examine voltages at each end of the trace by using a lattice diagram.

Calculate Z_O' and T_{PD}'

$$Z_O' = Z_O / \sqrt{1 + C_D/C_O}$$

$$T_{PD} = T_{PD} \times \sqrt{1 + C_D/C_O}$$

C_D = (4 devices x (15 pF/device)) / 8 in of trace = 7.5 pF/in.

To calculate C_O, first calculate T_{PD} for a stripline of E_R = 4.7 using the equations in Figure 3(c). T_{PD} = 2.20 ns/ft.

Calculate intrinsic capacitance: $C_O = T_{PD}/Z_O$ = 2.04 pF/in.

Inserting the C_O and C_D values yields: Z_O' = 41.6 Ω and T_{PD}' = 4.76 ns/ft.

The following procedure is outlined in **LATTICE DIAGRAM** (see Figure 5(a)).

Switching Levels

V_{OH} = 4.75 V, V_{OL} = 0.25 V.

Output High to Output Low

$\Delta V_{OUt} = V_{FINAL} - V_{INITIAL} = V_{OL} - V_{OH}$ = -4.50 V.

Use Z_D = 20 Ω because the final value is the driven low case.

The voltage divider at the driving end of the trace for Z_D = 20 Ω and Z_O' = 41.6 Ω gives: $\Delta V_0 = \Delta V_{OUT} \times \frac{Z_O'}{Z_O' + Z_D}$ = -3.04 V.

Calculate Reflection Coefficients

$$\rho_S = \frac{Z_D - Z_O'}{Z_D + Z_O'} = \frac{20 - 41.6}{20 + 41.6} = -0.351$$

$$\rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} = \frac{100k - 41.6}{100k + 41.6} \approx 1 \ (=0.999)$$

The voltages and currents down the trace are modified proportionally with the reflection coefficients. $V_{INITIAL} = V_{OH} = 4.75$ V.

$V_0 = \Delta V_0 + V_{INITIAL} = 1.71$ V.

$V_1 = \Delta V_0 \times (1 + \rho_L) + V_{INITIAL} = -1.33$ V.

$V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = -0.261$ V.

$V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 0.803$ V.

$V_4 = \Delta V_0 \times \rho_L^2 \times \rho_S \times (1 + \rho_S) + V_2 = 0.430$ V.

$V_5 = \Delta V_0 \times \rho_L^2 \times \rho_S^2 \times (1 + \rho_L) + V_3 = 0.058$ V.

$V_6 = \Delta V_0 \times \rho_L^3 \times \rho_S^2 \times (1 + \rho_S) + V_4 = 0.188$ V.

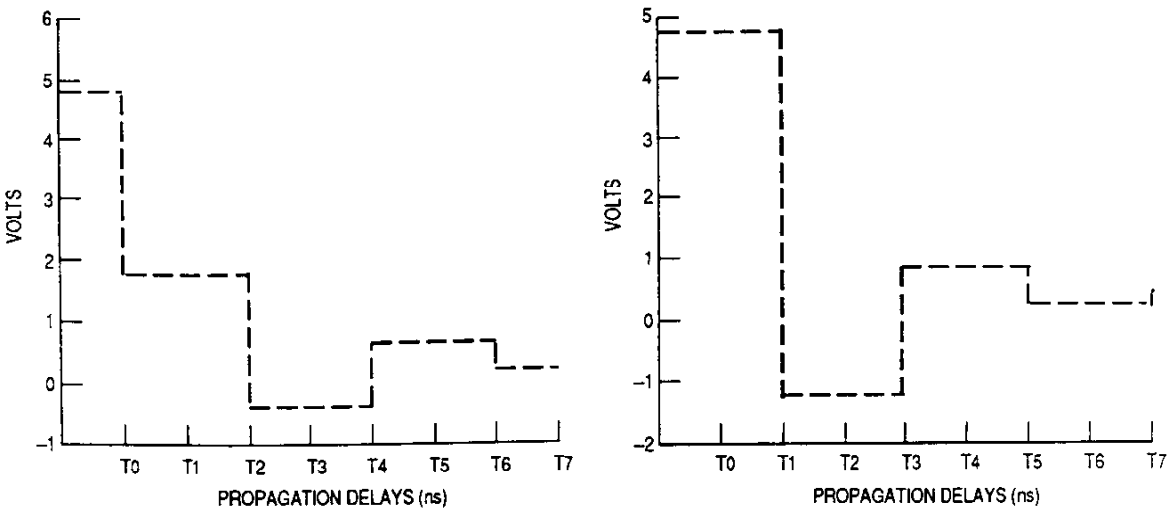
$V_7 = \Delta V_0 \times \rho_L^3 \times \rho_S^3 \times (1 + \rho_L) + V_5 = 0.319$ V.

From Figure 5(a), V_{FINAL} is calculated:

$$V_{FINAL} = \Delta V_{OUT} \times \frac{Z_L}{Z_L + Z_D} + V_{INITIAL} = -4.5 \times \frac{100k}{100k + 20} + 4.75 = 0.251 \text{ V}.$$

Notice that the voltages are settling towards 0.251 V, which is the final value in this transition.

The voltage versus time plots are shown in Figure A-1:



(a) Driving Device (b) Receiving Device

Figure A-1. Example 3 Unterminated High-to-Low Switching Results

Output Low to Output High

$$\Delta V_{OUT} = V_{FINAL} - V_{INITIAL} = V_{OH} - V_{OL} = 4.50 \text{ V}.$$

For this case, $Z_D = 120\ \Omega$, since the final state is the high-driving state.

The voltage divider at the driving end of the trace for $Z_D = 120\ \Omega$ and $Z_O' = 41.6\ \Omega$ gives: $\Delta V_0 = \Delta V_{OUT} \times \frac{Z_O'}{Z_O' + Z_D} = 1.16$ V.

Calculate Reflection Coefficients

$$\rho_S = \frac{Z_D - Z_O'}{Z_D + Z_O'} = \frac{120 - 41.6}{120 + 41.6} = 0.485$$

$$\rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} = \frac{100k - 41.6}{100k + 41.6} \approx 1 \ (=0.999)$$

The voltages and currents down the trace are modified proportionally with the reflection coefficients. The initial voltage is the logic-low state = 0.25 V.

$V_0 = \Delta V_0 + V_{INITIAL} = 1.41$ V.

$V_1 = \Delta V_0 \times (1 + \rho_L) + V_{INITIAL} = 2.57$ V.

$V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = 3.13$ V.

$V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 3.69$ V.

$V_4 = \Delta V_0 \times \rho_L^2 \times \rho_S \times (1 + \rho_S) + V_2 = 3.96$ V.

$V_5 = \Delta V_0 \times \rho_L^2 \times \rho_S^2 \times (1 + \rho_L) + V_3 = 4.23$ V.

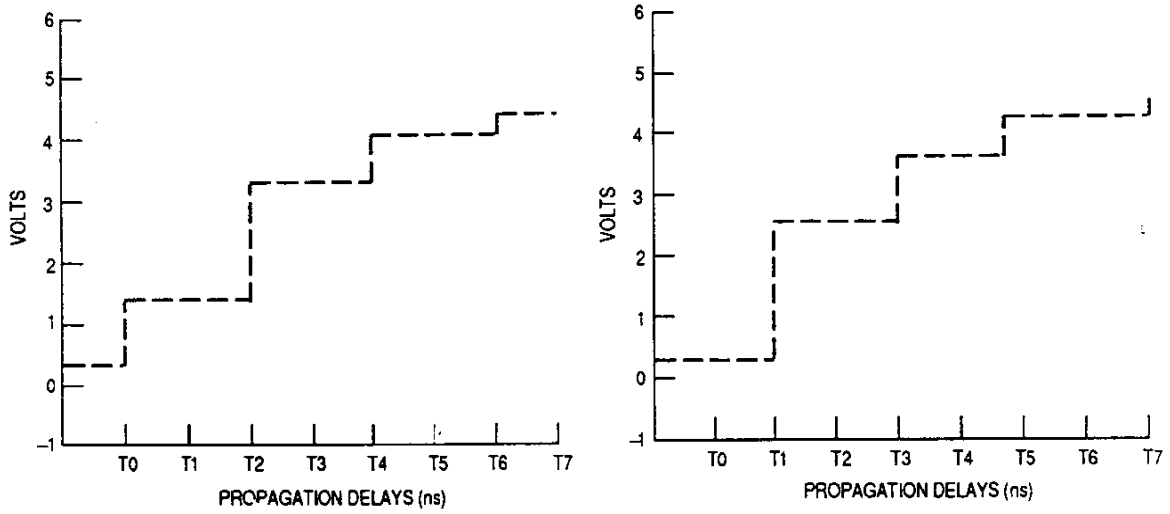
$V_6 = \Delta V_0 \times \rho_L^3 \times \rho_S^2 \times (1 + \rho_S) + V_4 = 4.36$ V.

$V_7 = \Delta V_0 \times \rho_L^3 \times \rho_S^3 \times (1 + \rho_L) + V_5 = 4.50$ V.

$$V_{FINAL} = \Delta V_{OUT} \times \frac{Z_L'}{Z_L' + Z_D} + V_{INITIAL} = 4.5 \times \frac{100k}{100k + 20} + 0.25 = 4.75 \text{ V.}$$

In this case, the voltage creeps up toward the final value of 4.75 V. The ringing effects are not as severe as the high-to-low case, but the high-voltage value is not reached until several propagation delays have transpired. The stair-stepping occurs because the loaded characteristic impedance is lower than the output impedance of the driving device. In the first case, ringing occurs because the output impedance of the driving device is lower than the loaded characteristic impedance of the trace.

The voltage versus time plots are shown in Figure A-2:



(a) Driving Device (b) Receiving Device

Figure A-2. Example 3 Unterminated Low-to-High Switching Results

EXAMPLE 4: LATTICE DIAGRAM WITH SERIES TERMINATION

The conditions are the same as Example 3. A series termination resistor of 25 Ω is inserted to reduce ringing in the high-to-low switching state. The lattice diagram analysis for both states is performed to show the series termination tradeoffs in this situation.

Series Termination

For series termination, a resistor is placed in series at the driving device's output, altering the output impedance value used in the calculations.

$Z_D' = Z_D + R_S$, where R_S is the series resistor and Z_D' is the new output impedance value used in calculations.

Output-High to Output-Low Switching

Choose $R_S = 25\ \Omega$. Now $Z_D' = Z_D + R_S = 25 + 20 = 45\ \Omega$.

Z_O' remains the same (41.6 Ω).

Recalculate ρ_s

$$\rho_S = \frac{Z_D - Z_D'}{Z_D + Z_O'} = \frac{45 - 41.6}{45 + 41.6} = 0.0393$$

$$\rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} = \frac{100k - 41.6}{100k + 41.6} \approx 1\ (=0.999)$$

Calculate Voltages

Output voltage levels are $V_{OH} = 4.75$ V, $V_{OL} = 0.25$ V.

For the high-to-low case, $\Delta V_{OUT} = V_{FINAL} - V_{INITIAL} = V_{OL} - V_{OH} = -4.5$ V.

The voltage divider at the driving end of the trace yields:

$$\Delta V_0 = \Delta V_{OUT} \times \frac{Z_O'}{Z_O' + Z_D} = -2.16\ \text{V}.$$

The voltages and currents down the trace are modified proportionally with the reflection coefficients. Use initial voltage of high case (= 4.75 V).

$V_0 = \Delta V_0 + V_{INITIAL} = 2.59$ V.

$V_1 = \Delta V_0 \times (1 + \rho_L) + V_{INITIAL} = 0.429$ V.

$V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = 0344$ V.

$V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 0.259$ V.

$V_4 = \Delta V_0 \times \rho_L^2 \times \rho_S \times (1 + \rho_S) + V_2 = 0.256$ V.

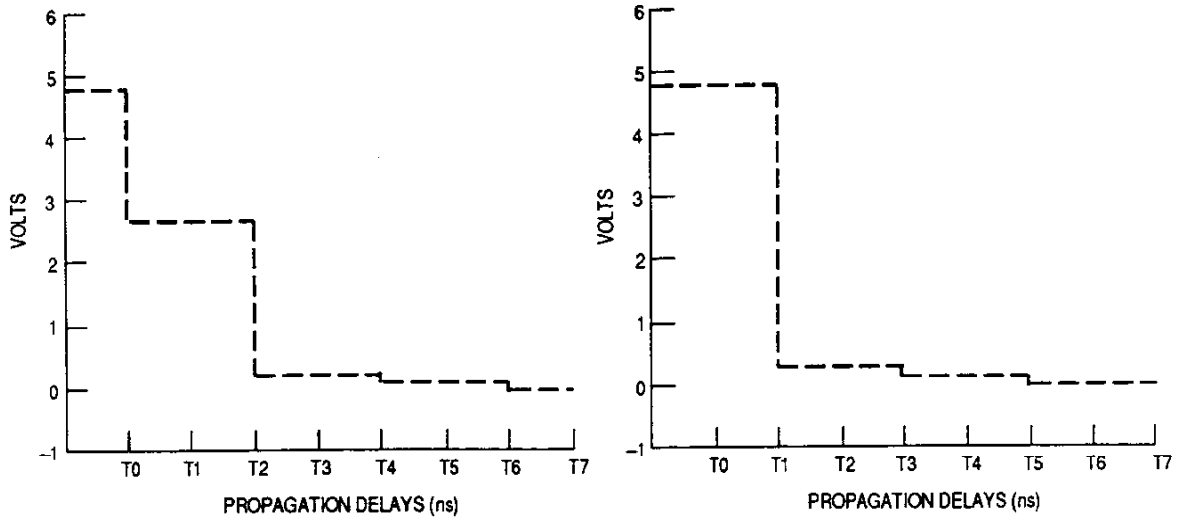
$V_5 = \Delta V_0 \times \rho_L^2 \times \rho_S^2 \times (1 + \rho_L) + V_3 = 0.252$ V.

$V_6 = \Delta V_0 \times \rho_L^3 \times \rho_S^2 \times (1 + \rho_S) + V_4 = 0.252$ V.

$V_7 = \Delta V_0 \times \rho_L^3 \times \rho_S^3 \times (1 + \rho_L) + V_5 = 0.252$ V.

The termination reduces the ringing as the voltage settles to its final voltage level of 0.252 V. It is important to note that the first waveform (V_0) is a half-voltage waveform. This places the output in the region between logic levels in which noise on the trace may cause receiving devices to switch unpredictably, but only for a short time (2 x T_{PD}'). Also, the devices at the receiving end of trace see the full waveform after one propagation delay; whereas, the driving device (and devices near it) see it after two propagation delays.

The voltage versus time plots are shown in Figure A-3:



(a) Driving Device (b) Receiving Device

Figure A-3. Example 4 Series Terminated High-to-Low Switching Results

This is a good fix for the ringing in the high-to-low switching event. To get a complete idea of the impact of the series resistor, the low-to-high event must be examined.

Output-Low to Output-High Switching

$\Delta V_{OUT} = V_{FINAL} - V_{INITIAL} = V_{OH} - V_{OL} = 4.5$ V.

For this case, $Z_D' = Z_D + R_S = 120\ \Omega + 25\ \Omega = 145\ \Omega$, since the final state is the high-driving state and $Z_{OH} = 120\ \Omega$.

The voltage divider at the driving end of the trace for $Z_D' = 145\ \Omega$ and $Z_O' = 41.6\ \Omega$ yields: $\Delta V_0 = \Delta V_{OUT} \times \frac{Z_O'}{Z_O' + Z_D} = 1.00$ V.

Calculate Reflection Coefficients

$$\rho_S = \frac{Z_D - Z_O'}{Z_D + Z_O'} = \frac{145 - 41.6}{145 + 41.6} = 0.554$$

$$\rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} = \frac{100k - 41.6}{100k + 41.6} \approx 1\ (=0.999)$$

The voltages and currents down the trace are modified proportionally with the reflection coefficients. The initial voltage is the logic-low state = 0.25 V.

$V_0 = \Delta V_0 + V_{INITIAL} = 1.25$ V.

$V_1 = \Delta V_0 \times (1 + \rho_L) + V_{INITIAL} = 2.25$ V.

$V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = 2.81$ V.

$V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 3.37$ V.

$V_4 = \Delta V_0 \times \rho_L^2 \times \rho_S \times (1 + \rho_S) + V_2 = 3.67$ V.

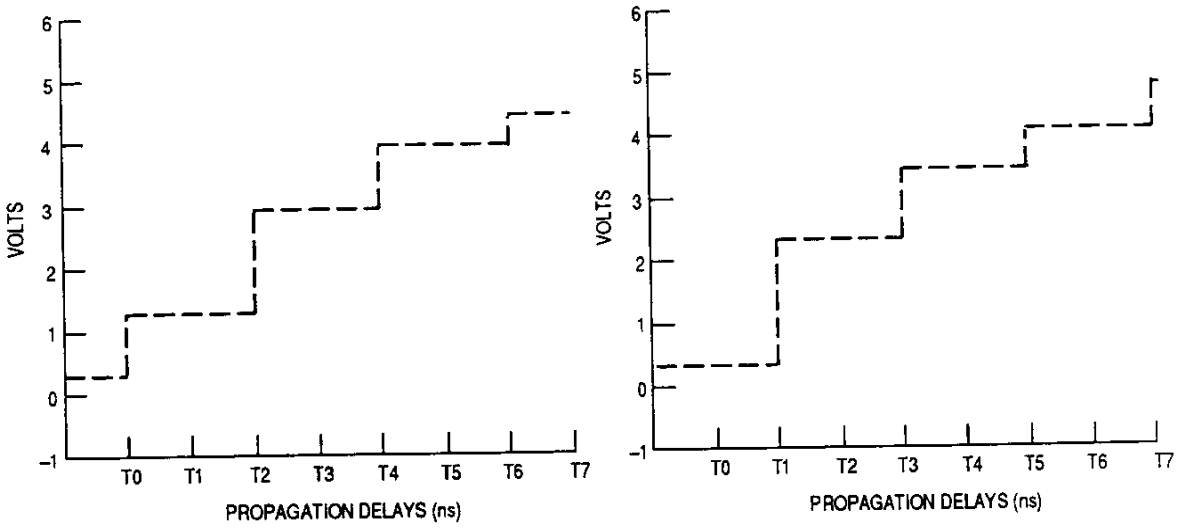
$V_5 = \Delta V_0 \times \rho_L^2 \times \rho_S^2 \times (1 + \rho_L) + V_3 = 3.98$ V.

$V_6 = \Delta V_0 \times \rho_L^3 \times \rho_S^2 \times (1 + \rho_S) + V_4 = 4.15$ V.

$$V_{FINAL} = \Delta V_{OUT} \times \frac{Z_L'}{Z_L' + Z_D} + V_{INITIAL} = 4.5 \times \frac{100k}{100k + 145} + 0.25 = 4.74 \text{ V.}$$

The series termination exaggerates the low-to-high stair-stepping from the unterminated state because the output impedance of the driving device is larger than the unterminated state ($Z_D' = 145\ \Omega$; $Z_D = 120\ \Omega$), which is exaggerated when the termination is added. This illustrates one of the sequences involved in terminating lines—one undesirable effect is reduced while another is exaggerated.

The voltage versus time plots are shown in Figure A-4:



(a) Driving Device

(b) Receiving Device

Figure A-4. Example 4 Series Terminated Low-to-High Switching Results

EXAMPLE 5: LATTICE DIAGRAM WITH PARALLEL TERMINATION

The trace characteristics are identical to the previous two examples. Now a parallel resistor is placed at the end of the trace to absorb the energy of the switching wave. This implementation also represents the ac switching events that occur when a RC network is not changed when the voltage initially switches.

In the parallel termination scheme, a resistor of value Z_O' is placed at the receiving device's end of the trace. Since $Z_O' = 41.6\ \Omega$, choose $Z_L' = 40\ \Omega$.

Output High to Output Low

$Z_D = 20\ \Omega$ in the low-driving case. $Z_O' = 41.6\ \Omega$.

Recalculate Reflection Coefficients

$$\rho_S = \frac{Z_D - Z_O'}{Z_D + Z_O'} = \frac{20 - 41.6}{20 + 41.6} = -0.351$$

$$\rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} = \frac{40 - 41.6}{40 + 41.6} = 0.0196$$

This is the same source reflection coefficient as the unterminated case. The change in reflection coefficients due to the parallel termination is seen in ρ_L:

Calculate Voltages

$$\Delta V_{OUT} = V_{FINAL} - V_{INITIAL} = V_{OL} - V_{OH} = -4.5\ V.$$

The voltage divider at the driving end of the trace gives:

$$\Delta V_0 = \Delta V_{OUT} \times \frac{Z_O'}{Z_O' + Z_D} = -4.5 \times \frac{41.6}{41.6 + 20} = -3.04\ V.$$

Using $V_{INITIAL} = 4.75\ V$, the voltages are:

$$V_0 = \Delta V_0 + V_{INITIAL} = 1.71\ V.$$

$$V_1 = \Delta V_0 \times (1 + \rho_L) + V_{INITIAL} = 1.65\ V.$$

$$V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = 1.67\ V.$$

$$V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 1.67 \text{ V}.$$

The effect of driving the line low is not achieved because of the relationship between Z_D and Z_L'. The final value depends on the voltage divider at the load where Z_L' is the value of the parallel impedance of the termination resistor and the load impedance. Since the termination resistor (R_T) is much smaller than the load impedance (R_T = 40 Ω, Z_L = 100 kΩ), it is effectively the parallel impedance value. (Recall calculations for parallel resistance from circuit theory:

$$Z_L' = \frac{R_T \times Z_L}{R_T + Z_L} \approx 40\Omega).$$

$$V_{FINAL} = \Delta V_{OUT} \times \frac{Z_L'}{Z_L' + Z_D} + V_{INITIAL} = -4.5 \times \frac{40}{40 + 20} + 4.75 = 1.75 \text{ V}.$$

Most driving devices can drive to the low-logic state because the output impedance of the driving device changes as additional current is pumped into the circuit. With the nondynamic impedances used in the lattice diagram method, the final output low value is not reached, which is a limitation of this hand-analysis method.

For illustration of the parallel method, choose a larger Z_L' that allows the final output low value to be reached. For this case, choose Z_L' = 300 Ω. Check final voltage: $V_{FINAL} = \Delta V_{OUT} \times \frac{Z_L'}{Z_L' + Z_D} + V_{INITIAL} = -4.5 \times \frac{300}{300 + 20} + 4.75 =$ 0.531 V. This is an acceptable final voltage because it is less than the maximum input logic-low level (0.8 V).

Recalculate Reflection Coefficients

$$\rho_S = \frac{Z_D - Z_O'}{Z_D + Z_O'} = \frac{20 - 41.6}{20 + 41.6} = -0.351$$

$$\rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} = \frac{300 - 41.6}{300 + 41.6} = 0.756.$$

The voltage divider at the driving end of the trace yields:

$$\Delta V_0 = \Delta V_{OUT} \times \frac{Z_O'}{Z_O' + Z_D} = -3.04 \text{ V}.$$

Using $V_{INITIAL}$ = 4.75 V, the voltages at each end are:

$$V_0 = \Delta V_0 + V_{INITIAL} = 1.71 \text{ V}.$$

$V_1 = \Delta V_0 \times (1 + \rho_L) + V_{INITIAL} = -0.588$ V.

$V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = 0.218$ V.

$V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 0.828$ V.

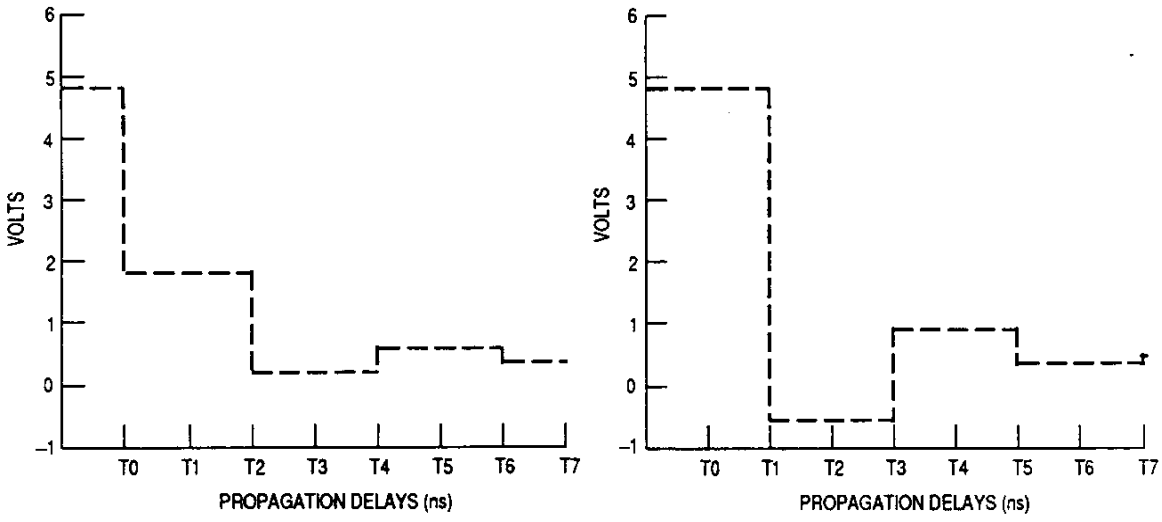
$V_4 = \Delta V_0 \times \rho_L^2 \times \rho_S \times (1 + \rho_S) + V_2 = 0.614$ V.

$V_5 = \Delta V_0 \times \rho_L^2 \times \rho_S^2 \times (1 + \rho_L) + V_3 = 0.453$ V.

$V_6 = \Delta V_0 \times \rho_L^3 \times \rho_S^2 \times (1 + \rho_S) + V_4 = 0.509$ V.

$V_7 = \Delta V_0 \times \rho_L^3 \times \rho_S^3 \times (1 + \rho_L) + V_5 = 0.552$ V.

The voltage versus time plots are shown in Figure A-5:



(a) Driving Device

(b) Receiving Device

Figure A-5. Example 5 Parallel Terminated High-to-Low Switching Results

As shown earlier, the final voltage is 0.531. In this case, notice that the first voltage (V_0 = 1.71 V) at the driving device falls in the intermediate zone between logic states because Z_O' and Z_D are close in value (41.6 and 20.0 Ω's, respectively), similarly to the unterminated case. The ringing is reduced at the

load but still exists. As with the series termination, this reduces the ringing in the high-to-low-switching event. The low-to-high-switching event must be examined, too.

Output-Low to Output-High Switching

$$\Delta V_{OUT} = V_{FINAL} - V_{INITIAL} = V_{OH} - V_{OL} = 4.5 \text{ V}.$$

For this case, $Z_D = 120\ \Omega$, since the final state is the high-driving state. The voltage divider at the driving end of the trace for $Z_D = 120\ \Omega$ and $Z_O' = 41.6\ \Omega$:

$$\Delta V_0 = \Delta V_{OUT} \times \frac{Z_O'}{Z_O' + Z_D} = 1.16 \text{ V}.$$

Calculate Reflection Coefficients

$$\rho_S = \frac{Z_D - Z_O'}{Z_D + Z_O'} = \frac{120 - 41.6}{120 + 41.6} = 0.485$$

$$\rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} = \frac{300 - 41.6}{300 + 41.6} = 0.756$$

The initial voltage is the logic-low state = 0.25 V.

$$V_0 = \Delta V_0 + V_{INITIAL} = 1.41 \text{ V}.$$

$$V_1 = \Delta V_0 \times (1 + \rho_L) + V_{INITIAL} = 2.29 \text{ V}.$$

$$V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = 2.71 \text{ V}.$$

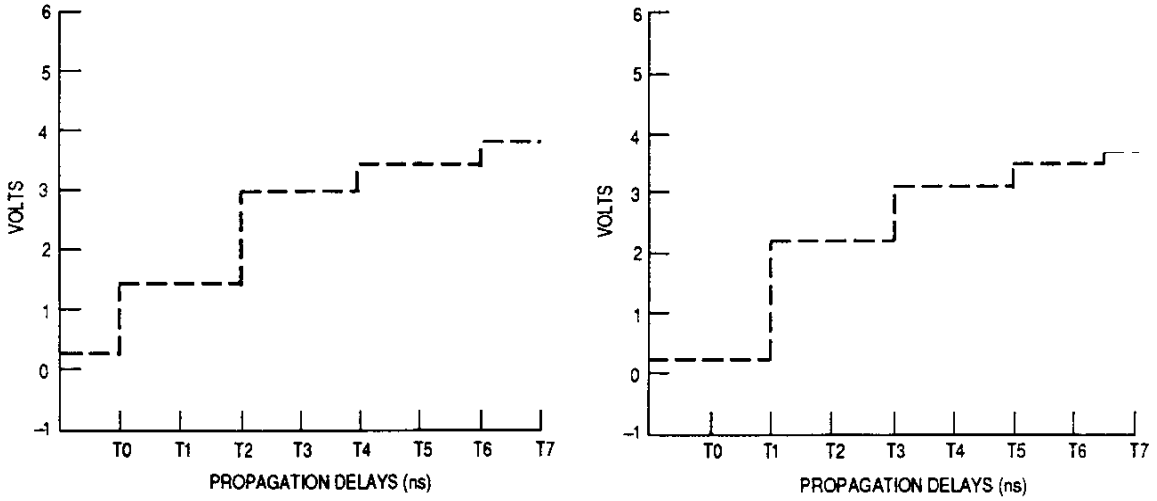
$$V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 3.04 \text{ V}.$$

$$V_4 = \Delta V_0 \times \rho_L^2 \times \rho_S \times (1 + \rho_S) + V_2 = 3.19 \text{ V}.$$

$$V_5 = \Delta V_0 \times \rho_L^2 \times \rho_S^2 \times (1 + \rho_L) + V_3 = 3.31 \text{ V}.$$

$$V_{FINAL} = \Delta V_{OUT} \times \frac{Z_L'}{Z_L' + Z_D} + V_{INITIAL} = 4.5 \times \frac{300}{300 + 120} + 0.25 = 3.46 \text{ V}.$$

The voltage versus time plots are shown in Figure A-6:



(a) Driving Device (b) Receiving Device

Figure A-6. Example 5 Parallel Terminated Low-to-High Switching Results

The final voltage predicted (3.46 V) is not the final output high voltage desired (4.75 V), but it is the new quiescent value, assuming the driving device does not supply additional current. Since the output impedance of the driving device is greater than the loaded characteristic impedance, stair-stepping occurs during the switching. Any additional load exaggerates the stair-stepping, which is the case when either parallel or series termination is added.

The major drawback with the parallel method of termination is the current consumed. The dc current for the high state would be:

$$I_{FINAL} = \frac{\Delta V_{OUT}}{Z_L' \times Z_D} + I_{INITIAL} = \frac{4.5}{320} + 14.9\ mA = 28.9\ mA$$

This dc current requirement violates the drive capability of many devices.

To solve this dc current drive issue, the RC termination scheme is recommended. In the first switching events of the circuit, the capacitor is not charged thus it acts identically as the parallel resistor tied to ground. After the voltage settles, the capacitor charges to the final voltage level and no dc current flows. The capacitor's value ranges between 200-600 pF, and the resistor's value is near Z_O'. The RC time constant must be less than twice the loaded propagation delay; otherwise, the RC network adds to the ringing.

For this case, use $Z_L' = 300\ \Omega$ and C = 300 pF. Since the time constant is 90 ns, this scheme should be satisfactory. The voltage and current levels during switching follow those given in the parallel termination resistor calculations for $R_T = 300\ \Omega$.

For designers who would like to experiment with various trace configurations and termination schemes, a spreadsheet of the formulas provides quick comparisons of the trade-offs involved in transmission line effects. Sample spreadsheets for Examples 1–3 are as follows:

Calculations of Surface Microstrip PCB Traits (Example 1 Configuration)

E_R (Dielectric Constant)	4.700	4.700
H (Dielectric Thickness)	12.000 in/1000	12.000 in/1000
T (Trace Thickness)	2.000 in/1000	2.000 in/1000
W (Trace Width)	10.000 in/1000	10.000 in/1000
Z_O (Characteristic Impedance)	69.363 Ω	69.363 Ω
T_{PD} (Unit Propagation Delay)	1.733 ns/ft	1.7.33 ns/ft
C_O (Intrinsic Capacitance)	2.082 pF/in	2.082 pF/in
L(Length of Trace)	4.000 in	6.000 in
n (Number of Devices on Trace)	6.000	4.000
C_l (Load Capacitance of Each Device)	7.000 pF	7.000 pF
C_D (Distributed Capacitance)	10.500 pF/in	4.667 pF/in
Z_O' (Loaded Characteristic Impedance)	28.214 Ω	38.524 Ω
T_{PD}' (Loaded Propagation Delay)	4.260 ns/ft	3.120 ns/ft
T_R or T_F (Lesser of Rise and Fall Times)	3.000 ns	3.000 ns
Round-Trip Time ($2*T_{PD}'*l$)	2.840 ns	3.120 ns
Need Termination? ($2*T_{PD}'* \le T_R$ or T_F)	0.160 ns	-0.120 ns
If results from previous line < 0, then further investigation is needed.		

Calculations of Surface Microstrip PCB Traits (Example 2 Configuration)

E_R (Dielectric Constant)	4.600	4.600
B (Overall Dielectric Thickness)	20.000 in/1000	20.000 in/1000
T (Trace Thickness)	1.400 in/1000	1.400 in/1000
W (Trace Width)	6.000 in/1000	6.000 in/1000
Z_O (Characteristic Impedance)	50.725 Ω	50.725 Ω
Z_O Formula Valid for W/(B-T)<0.35 and T/B<0.25	0.323 0.070	0.323 0.070
T_{PD} (Unit Propagation Delay)	2.181 ns.ft	2.181 ns/ft
C_O (Intrinsic Capacitance)	3.583 pF/in	3.583 pF/in
L (Length of Trace)	8.000 in	4.000 in
n (Number of Devices on Trace)	4.000	2.000
C_I (Load Capacitance of Each Device)	15.000 pF	15.000 pF
C_D (Distributed Capacitance)	7.500 pF/in	7.500 pF/in
Z_O' (Loaded Characteristic Impedance)	28.843 Ω	28.843 Ω
T_{PD}'(Loaded Propagation Delay)	3.836 ns/ft	3.836 ns/ft
T_R or T_F (Lesser of Rise and Fall Times)	3.000 ns	3.000 ns
Round-Trip Time ($2*T_{PD}'*l$)	5.115 ns	2.557 ns
Need Termination? ($2*T_{PD}'* \le T_R$ or T_F)	-2.115 ns	0.443 ns
If results from previous line < 0, then further investigation is needed.		

Lattice Diagram Worksheet
(Example 3: High-to-low Case)

Z_O (Characteristic Impedance)	90.000 Ω
T_{PD} (Propagation Delay)	2.200 ns/ft
C_O (Intrinsic Capacitance)	2.037 pF/in
L(Length of Trace)	8.000 in
n (Number of Devices on Trace)	4.000
C_I (Load Capacitance of Each Device)	15.000 pF
C_D (Distributed Capacitance)	7.500 pF/in
Z_O' (Loaded Characteristic Impedance)	41.594 Ω
T_{PD}' (Loaded Propagation Delay)	4.760 ns/ft
V_{OH} (Output High Voltage)	4.750 V
V_{OL} (Output Low Voltage)	0.250 V
Z_D (Output Impedance of Driving Device)	20.000 Ω
Z_I (Input Impedance of Driving Device)	100000.000 Ω
$V_{INITIAL} = V_{OH}$	4.750 V
$\Delta V_{OUT} = V_{OL} - V_{OH}$	-4.500 V
$\Delta V_0 = \Delta V_{OUT} * (Z_O'/(Z_O' + Z_D))$	-3.039 V
$V_{FINAL} = \Delta V_{OUT} * (Z_I'/(Z_I' + Z_D)) + V_{INITIAL}$	0.251 V
$\rho_S = (Z_D - Z_O')/(Z_D + Z_O')$	-0.351
$\rho_L = (Z_I - Z_O')/(Z_I + Z_O')$	0.999

Voltages	Source Voltage	Receiver Voltage	Time
$V_{INITIAL}$	4.750	4.750	T_I
V_0	1.711	4.750	T_0
V_1	1.711	-1.325	T_1
V_2	-0.261	-1.325	T_2
V_3	-0.261	0.803	T_3
V_4	0.430	0.803	T_4
V_5	0.430	0.803	T_5
V_6	0.188	0.058	T_6
V_7	0.188	0.319	T_7
Final Voltages	0.251	0.251	

Lattice Diagram Worksheet
(Example 3: Low-to-High Case)

Z_O (Characteristic Impedance)	90.000 Ω
T_{PD} (Propagation Delay)	2.200 ns/ft
C_O (Intrinsic Capacitance)	2.037 pF/in
l (Length of Trace)	8.000 in
n (Number of Devices on Trace)	4.000
C_I (Load Capacitance of Each Device)	15.000 pF
C_D (Distributed Capacitance)	7.500 pF/in
Z_O' (Loaded Characteristic Impedance)	41.594 Ω
T_{PD}' (Loaded Propagation Delay)	4.760 ns/ft
V_{OH} (Output High Voltage)	4.750 V
V_{OL} (Output Low Voltage)	0.250 V
Z_D (Output Impedance of Driving Device)	120.000 Ω
Z_I (Input Impedance of Driving Device)	100000.000 Ω
$V_{INITIAL} = V_{OH}$	0.250 V
$\Delta V_{OUT} = V_{OL}-V_{OH}$	4.500 V
$\Delta V_0 = \Delta V_{OUT} * (Z_O'/(Z_O' + Z_D))$	1.158 V
$V_{FINAL} = \Delta V_{OUT} * (Z_I'/(Z_I' + Z_D)) + V_{INITIAL}$	4.745 V
$\rho_S = (Z_D - Z_O')/(Z_D + Z_O')$	0.485
$\rho_L = (Z_I - Z_O')/(Z_I + Z_O')$	0.999

Voltages	Source Voltage	Receiver Voltage	Time
$V_{INITIAL}$	0.250	0.250	T_I
V_0	1.408	0.250	T_0
V_1	1.408	2.566	T_1
V_2	3.127	2.566	T_2
V_3	3.127	3.688	T_3
V_4	3.960	3.688	T_4
V_5	3.960	4.232	T_5
V_6	4.364	4.232	T_6
V_7	4.364	4.496	T_7
Final Voltages	4.745	4.745	

EXAMPLE 6: BERGERON PLOT

A Motorola FACT device drives two MC88200s over an unterminated 5-in surface microstrip laid out in a daisy-chain configuration with a characteristic impedance of 70 Ω and a dielectric constant of 4.7.

The Bergeron plot method will be used as outlined in Reference 6 (page 2-3). The V_{IN} versus I_{IN} curve for the MC88200s is given in this example. These are hand-drawn approximations, not simulated or measured values (i.e., these are for exercise only).

Calculate Z_O'

$$Z_O' = \frac{Z_O}{\sqrt{1 + C_D/C_O}}$$

Find the intrinsic and distributed capacitance values:

$C_O = T_{PD} / Z_O = 1.017 \times \sqrt{0.475E_R + 0.67} / Z_O = 1.73$ ns/ft / 70 Ω = 2.06 pF/in.

$C_D = 2 \times 15$ pF/ 5 in = 6 pF/in.

$$Z_O' = \frac{70}{\sqrt{1 + 6.00/2.06}} = 35.4\ \Omega.$$ For simplicity, use 35 Ω.

This value of 35 Ω is used as a slope throughout the Bergeron plot analysis. To graph it, select voltages and currents whose differences provide an impedance of 35 Ω. For example, to get a 35-Ω slope, choose one voltage and current point at the 0-V and 0-mA point. The second point should be 3.5 V and 100 mA for a positive 35-Ω slope or 3.5 V and -100 mA for a negative 35-Ω slope (Z_O' = V/I). Lines drawn parallel to this are used throughout the plot.

Bergeron Plot Method

1. Start at a quiescent point (intersection of V_{OL}/I_{OL} or V_{OH}/I_{OH} and V_{IN}/I_{IN}). For the high-to-low transition, start at the high quiescent point; for the low-to-high transition, start at the low quiescent point.

2. Draw line with slope of $+Z_O'$ for a low-to-high transition or $-Z_O'$ for a high-to-low transition. This intersects with a V_{OL}/I_{OL} or V_{OH}/I_{OH} line, indicating the voltage and current seen at the discontinuity between the output driving device and the trace.

3. Draw a line of slope ± Z_O' whose sign is opposite to that of the first line drawn. This line intersects with the V_{IN}/I_{IN} line, which provides the voltage and current seen at the receiving device's input from the trace.

4. Repeat steps 2 and 3 until the Z_O' lines converge on the new quiescent point.

5. Take the voltage values at the intersections and plot these with respect to time. Intersection points on the V_{OL}/I_{OL} or V_{OH}/I_{OH} curves are voltages at the driving device; whereas, points on the V_{IN}/I_{IN} curves are voltages at the receiving device.

Each voltage step from a V_{OL}/I_{OL} or V_{OH}/I_{OH} line to a V_{IN}/I_{IN} line occurs in time T_{PD}'.

Comments

In the low-to-high case, the receiving devices experience voltages as high as 6.4 V; in the high-to-low case, they experience voltages as low as -1 V.

The Bergeron method (see Figure A-7) requires much less calculation than the lattice diagram method. It also does not assume a linear value for Z_O of the driving device. One drawback for the Bergeron plot is the availability of V/I curves. If the devices used have these curves available, then this is the preferred method of hand analysis. Also, these V/I curves vary over temperature, process, and supply voltage. To account for these factors in a worst-case manner may not always be straightforward. It is important to note this as a limitation.

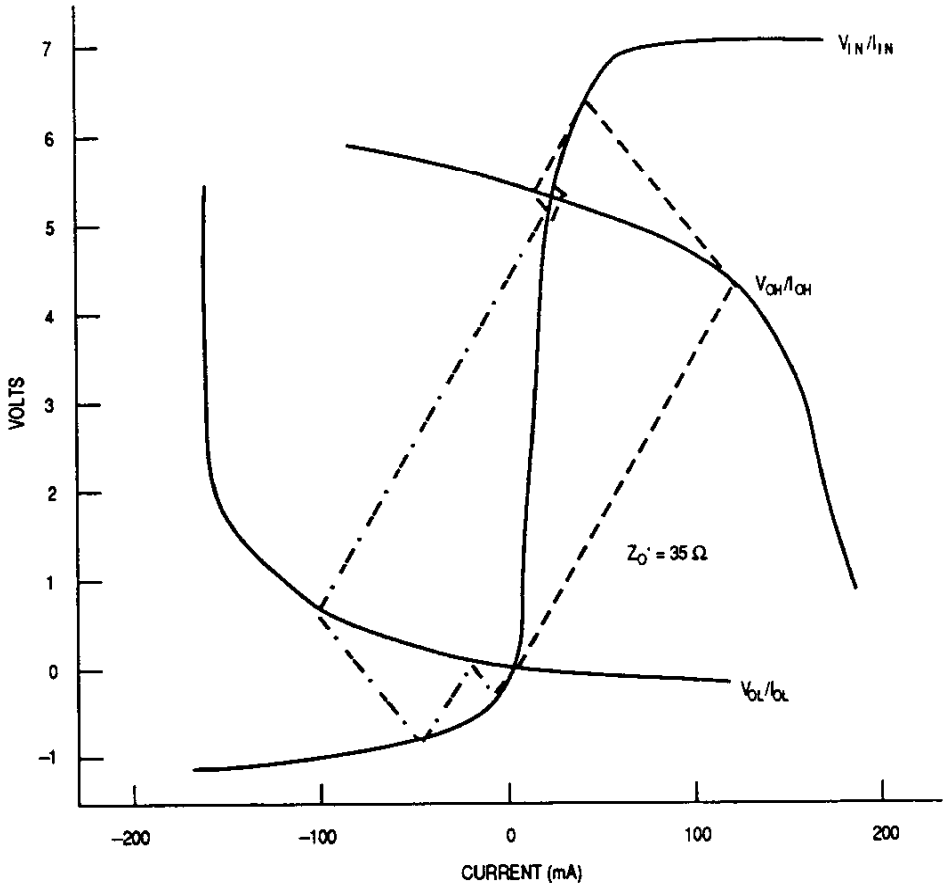
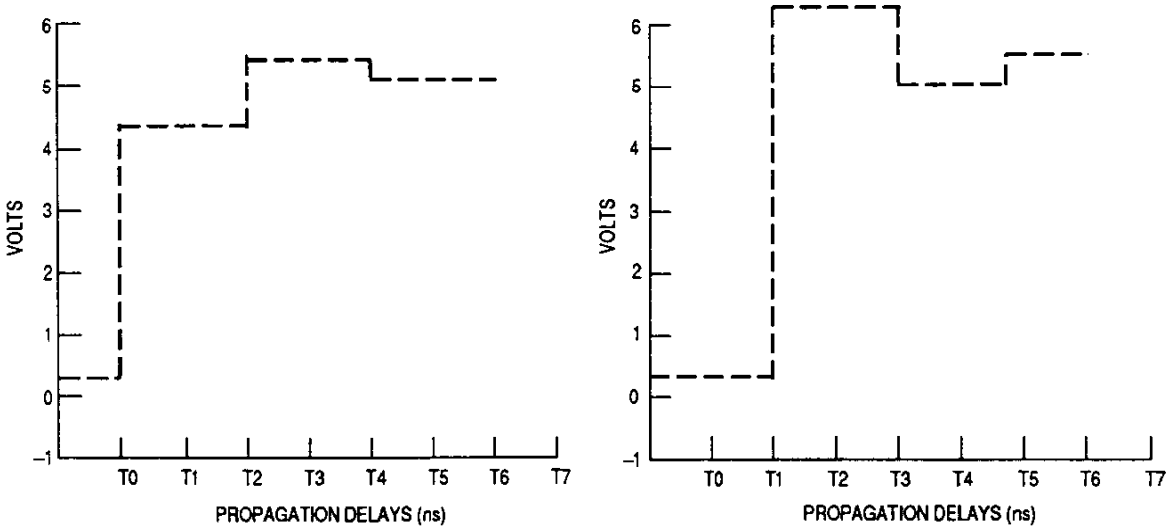


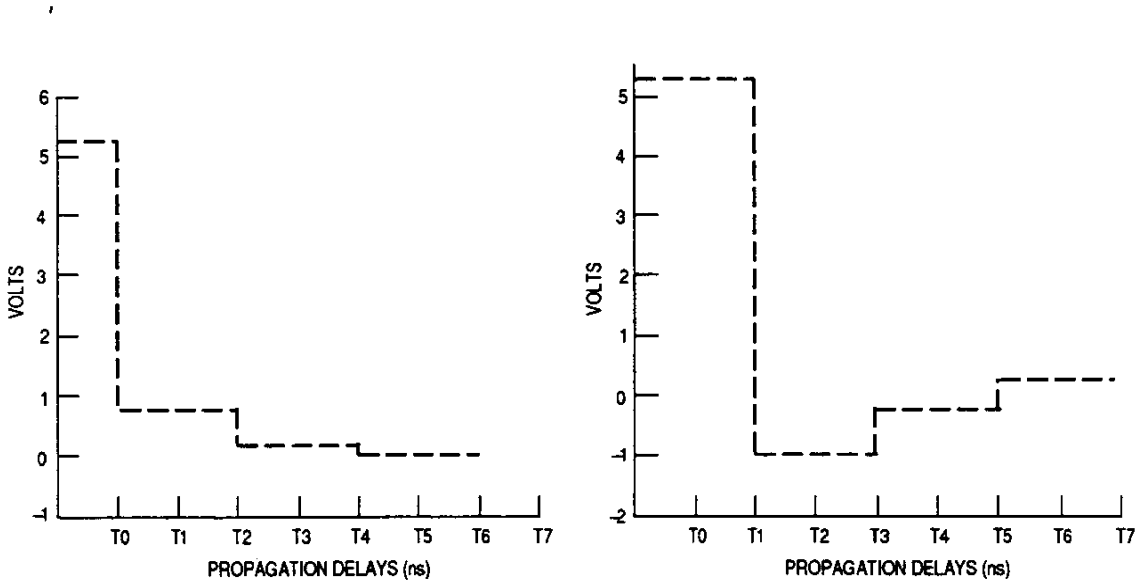
Figure A-7. Bergeron Plot

The voltage versus time plots are shown in Figures A-8 and A-9:



(a) Driving Device (b) Receiving Device

Figure A-8. Example 6 Unterminated Low-to-High Switching Results



(a) Driving Device (b) Receiving Device

Figure A-9. Example 6 Unterminated High-to-Low Switching Results

EXAMPLE 7: BERGERON PLOT FOR DEVICES WITH HIGH-DRIVE CAPABILITIES

Determine the transmission line effects when a device designed to drive a heavy load is connected to four devices with a load capacitance of 15 pF each over an 8-in stripline trace that is laid out in daisy-chain configuration.

Trace Characteristics

B = 0.016 in, W = 0.006 in,T= 0.0014 in, and E_R = 4.5.

From stripline equations in Figure 3(c), Z_O = 45 Ω and T_{PD} = 2.16 ns/ft = 0.180 ns/in.

Calculate Effects of Load

C_D = 4 devices x 15 pF/device/8 in = 7.5 pF/in.

$C_O = T_{PD} / Z_O$ = 2.16 ns/ft/45 Ω x 1000 pF/1 nF x 1 ft/12 in = 4 pF/in.

$$Z_O' = \frac{Z_O}{\sqrt{1 + C_D/C_O}} = 26.5\ \Omega \approx 25\ \Omega.$$

The Bergeron plot for Z_O' = 25 Ω is shown in Figure A-10.

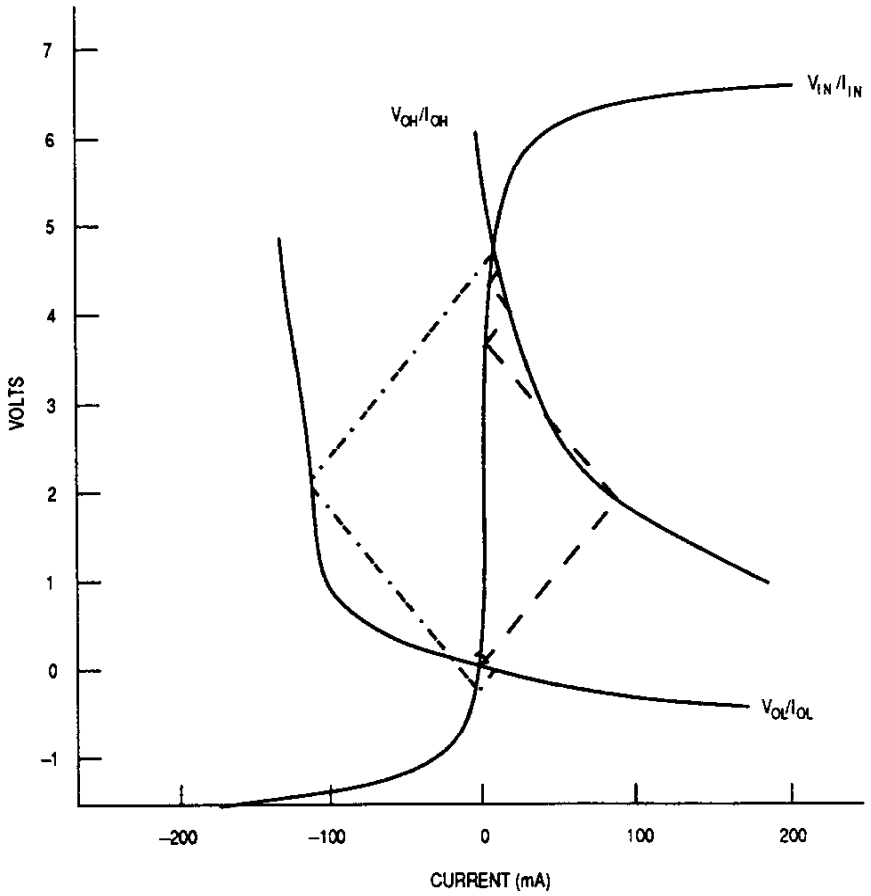
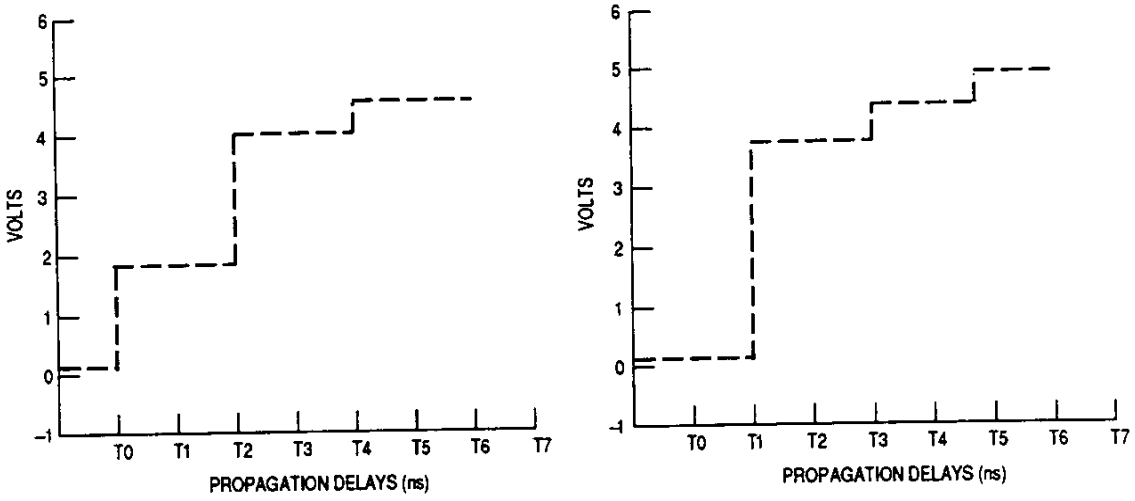


Figure A-10. Bergeron Plot for $Z_O' = 25\ \Omega$

The voltage versus time plots are shown in Figures A-11 and A-12:

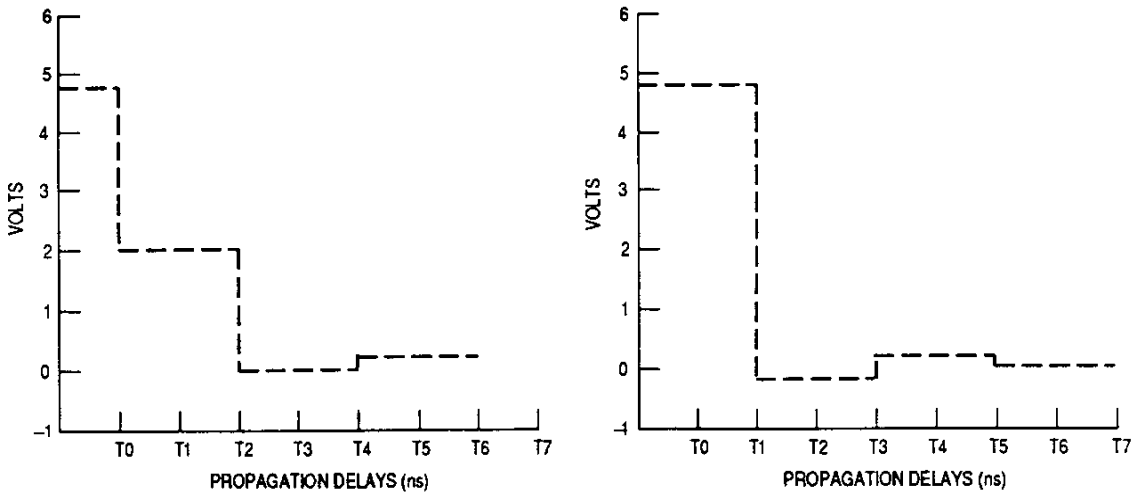


(a) Driving Device

(b) Receiving Device

NOTE: The load matches the drive capability of the driving device fairly well; there is some stairstepping in the low-to-high case but little undershoot in the high-to-low case.

Figure A-11. Unterminated Low-to-High Switching Results



(a) Driving Device

(b) Receiving Device

NOTE: The load matches the drive capability of the driving device fairly well; there is some stairstepping in the low-to-high case but little undershoot in the high-to-low case.

Figure A-12. Unterminated High-to-Low Switching Results

EXAMPLE 8: BERGERON PLOT WITH PARALLEL TERMINATION

The device and trace configuration is identical to Example 7. The parallel form of termination is examined to demonstrate how the V/I curves are altered when it is used.

For parallel terminations, the V_{IN}/I_{IN} curve is modified such that its slope matches the value of the termination. Several different values are shown in Figure A-13.

Notice that the clamping effect from the diodes is applied, but the linear region follows the value of the termination.

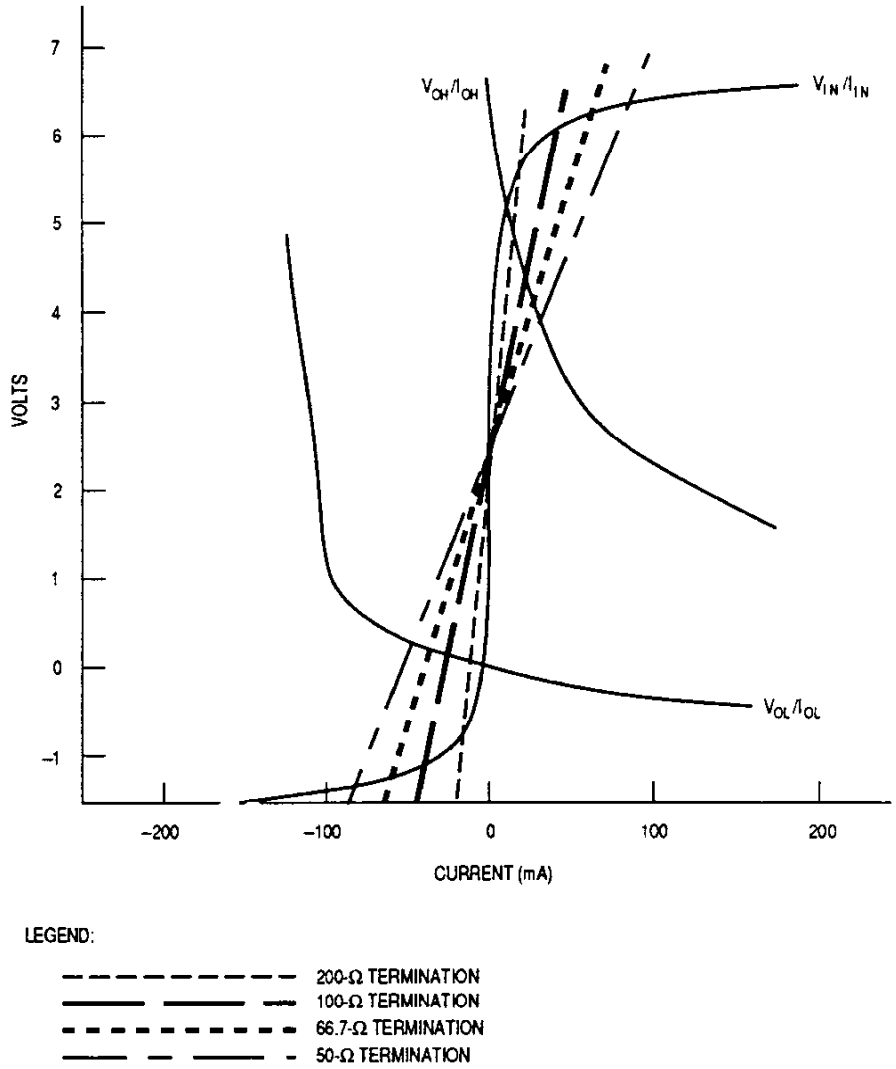


Figure A-13. Bergeron Plot with Assorted Parallel or RC Terminations

To terminate the trace used in Example 7, use a 66.7-Ω resistor tied to ground. The V_{in}/I_{in} curve is altered by changing the linear region of the curve to follow the slope of the parallel resistor (66.7 Ω). This can be implemented as the RC, Thevenin, or parallel method.

Although the ringing is reduced, there is not much difference from the unterminated state because this particular driving device handles the heavily loaded trace well.

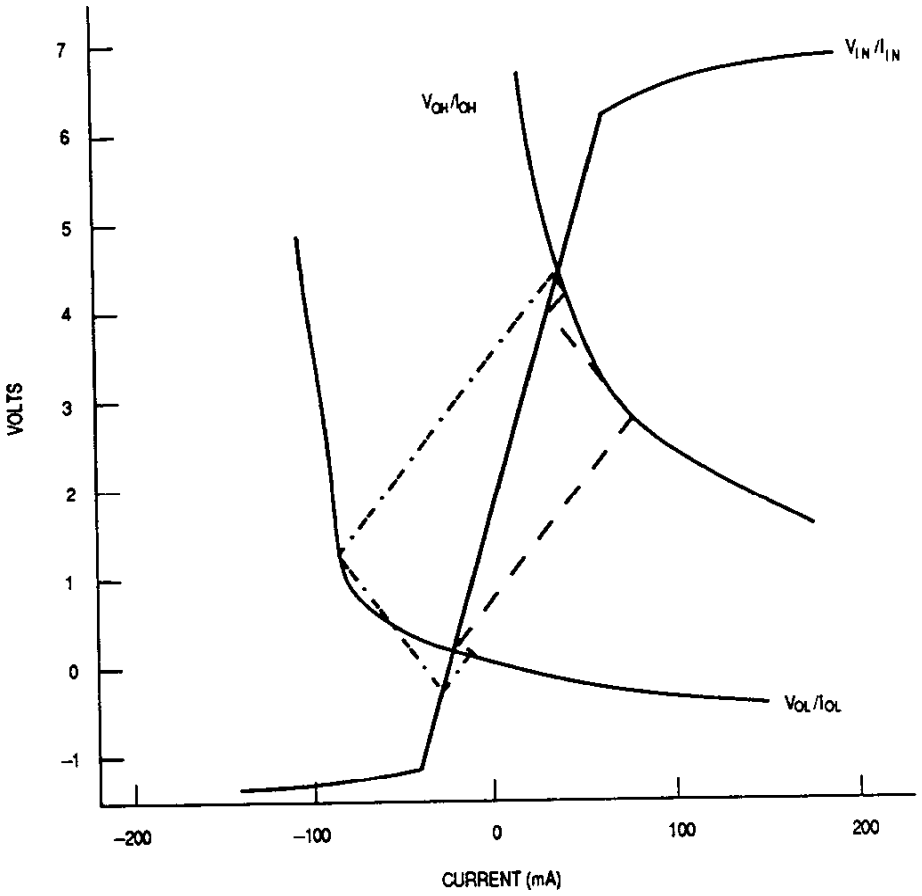


Figure A-14. Bergeron Plot for $Z_O' = 24\ \Omega$ with 66.7-Ω Parallel or RC Termination

EXAMPLE 9: BERGERON PLOT FOR A HEFTY OUTPUT DRIVING DEVICE CONNECTED TO A LIGHTLY LOADED TRACE

The same driving and receiving curves are used as in Examples 7 and 8, but a different characteristic impedance is used to illustrate what happens when a driving device that handles the heavily loaded trace (see Figure A-15) well is loaded lightly. Notice that the undershoot is greater and the ringing is substantial in the high-to-low switching case. There is less stair-stepping than in the case with $Z_O' = 25\ \Omega$. The characteristic of this output buffer shown in Examples 7–9 is, if the trace is heavily loaded to match the high-to-low drive capabilities, then stair-stepping occurs in the low-to-high drive case; if the trace is lightly loaded to match the low-to-high drive capabilities, then ringing occurs in the high-to-low drive case. The designer must understand which case is worse for the design and account for it accordingly.

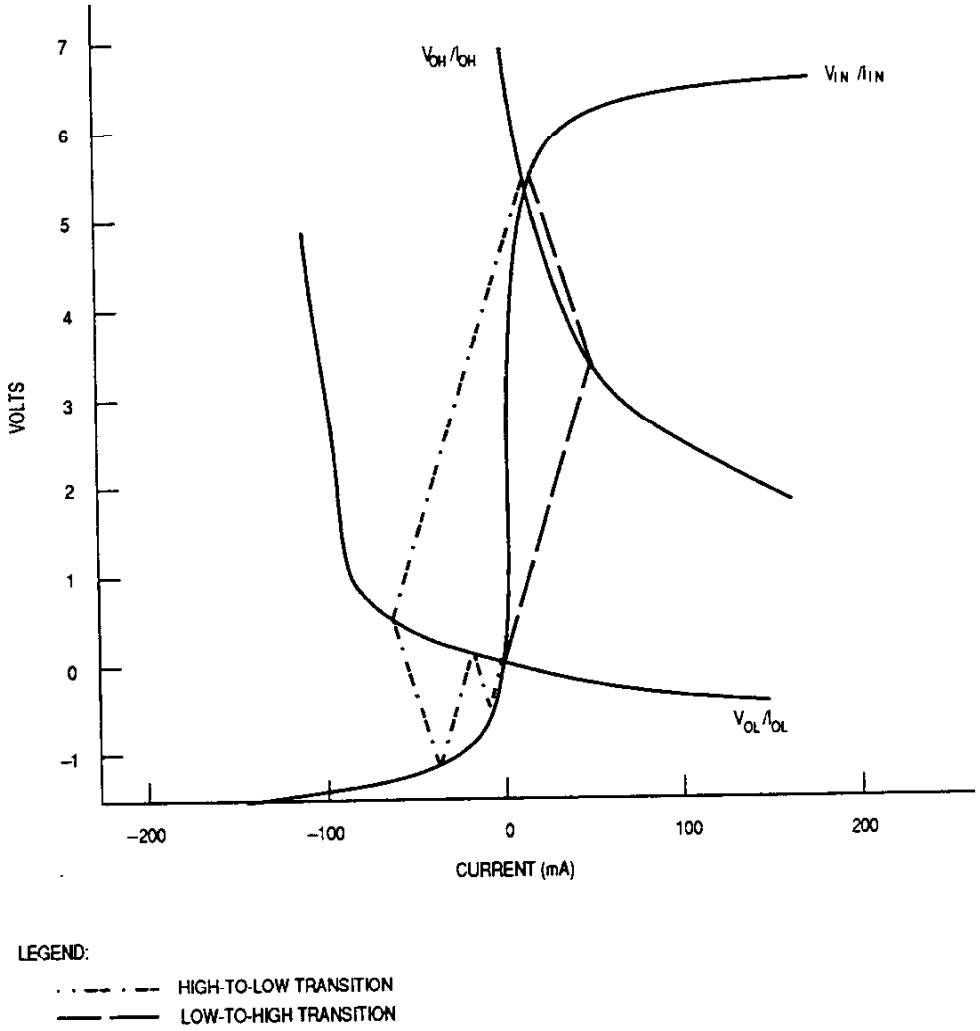


Figure A-15. Bergeron Plot with $Z_O' = 70\ \Omega$

To alleviate the ringing from the lightly loaded condition shown previously, terminate using a 100-Ω resistor implemented in parallel or RC fashion. The V_{IN}/I_{IN} curve is modified by using the slope of the parallel termination (100 Ω) for the linear region (see Figure A-16). This absorbs the ringing and overshoot well.

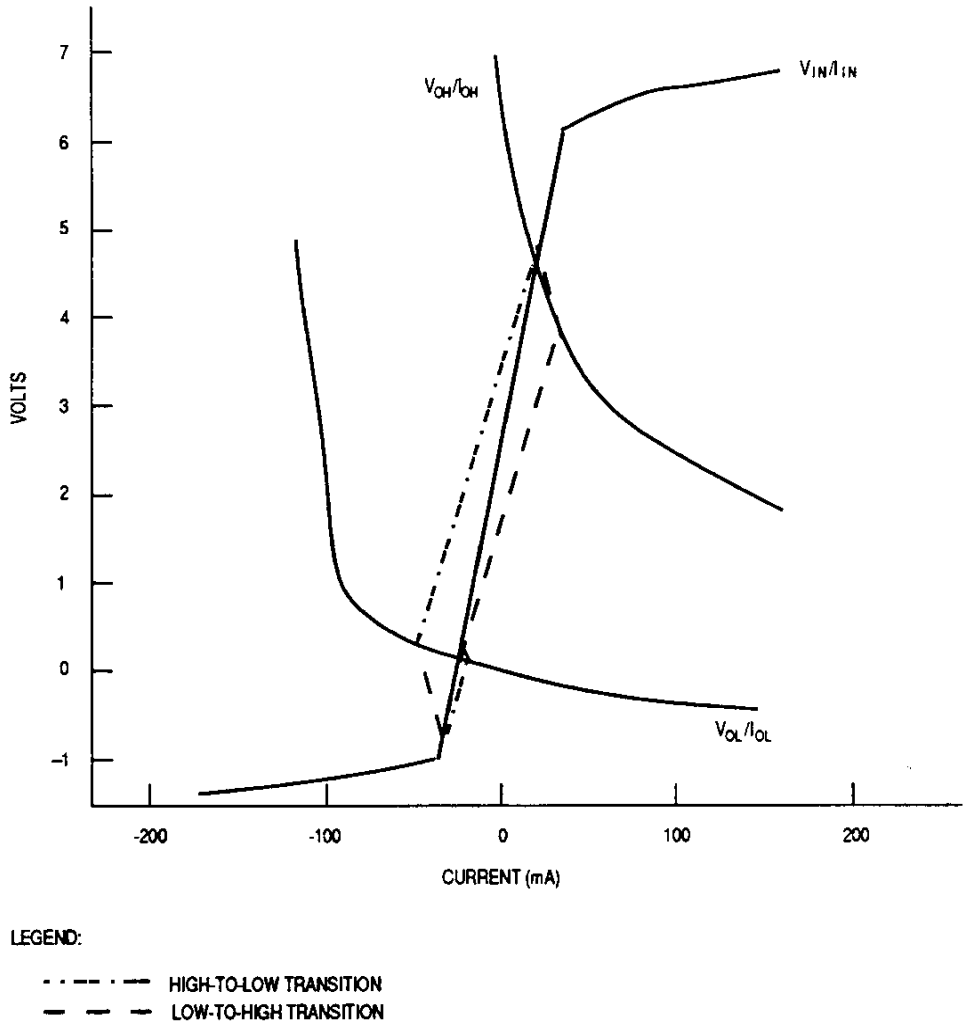


Figure A-16. Bergeron Plot with Z_O' = 70 Ω and 100 Ω Parallel or RC Termination

EXAMPLE 10: BERGERON PLOT FOR SERIES TERMINATION

For demonstration, use a trace with a loaded characteristic impedance of 50 Ω and devices with voltage versus current curves similar to the devices used in Examples 7, 8, and 9. The driving devices have similar output impedances for the high-to-low and low-to-high cases.

If a series resistor method is chosen for termination, the output curves of the driving device are modified. Z_D, the output impedance of the driving device, adds to R_S, the series resistor, to give the new output impedance, $Z_D' = 25\ \Omega$. This is the slope of the output curves for the driving device at both the high and low quiescent points.

An example of a 25-Ω series termination is shown in Figure A-17. The total output impedance is shown in the high and low states as a line with slope of 25. In this case, overshoot and undershoot occur. The stair-stepping is no longer evident, and the ringing is minimal.

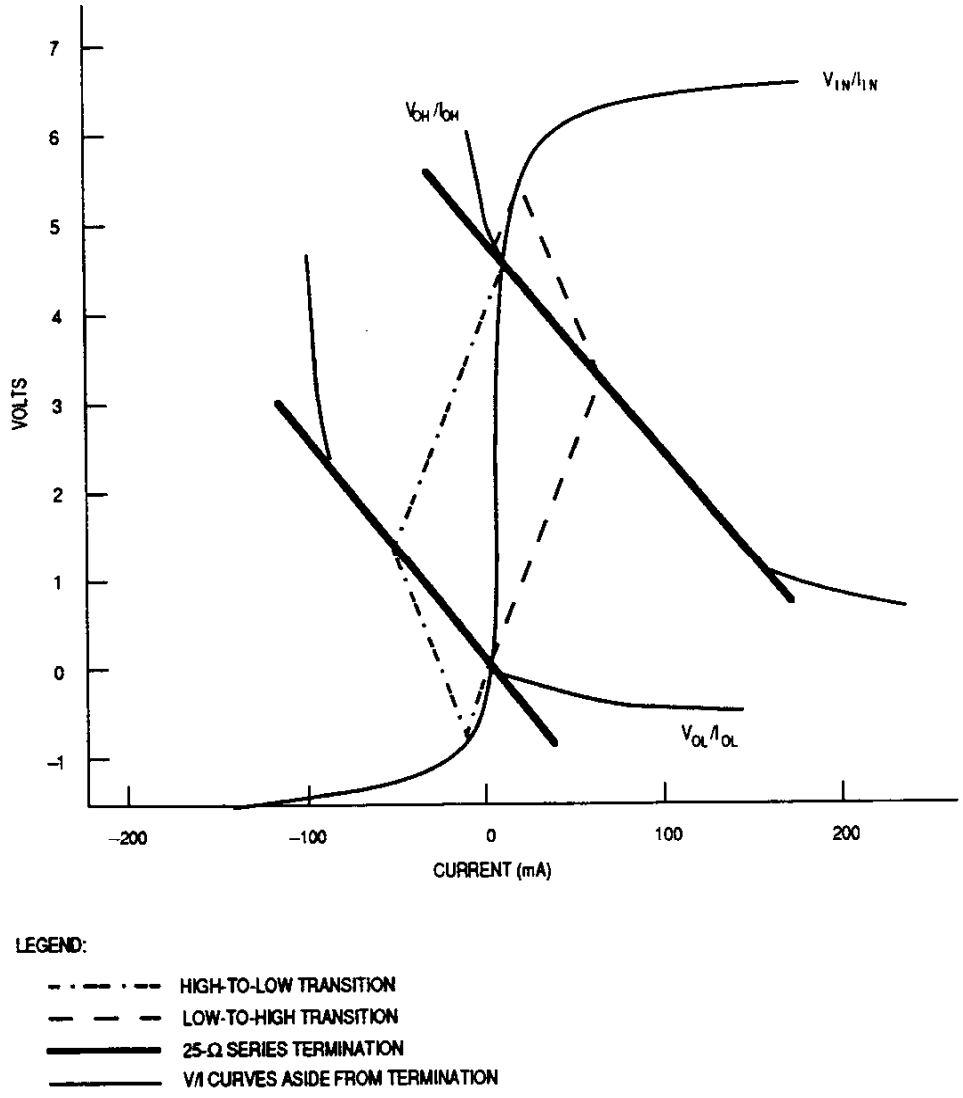


Figure A-17. Bergeron Plot for Z_O' = 50 Ω with 25-Ω Series Termination

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