SERVICE MANUAL

HP 8340A SYNTHESIZED SWEEPER

10 MHz to 26.5 GHz

HEWLETT PACKARD

VOLUME 3 CONTENTS

TABLES

SAFETY CONSIDERATIONS

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation. This product has been designed and tested in accordance with international standards.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual (refer to Table of Contents).

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND

This is a Safety Class I product (provided with a protective earthing terminal). An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an autotransformer, make sure the common terminal is connected to the neutral (grounded) side of mains supply.

SERVICING

WARNING

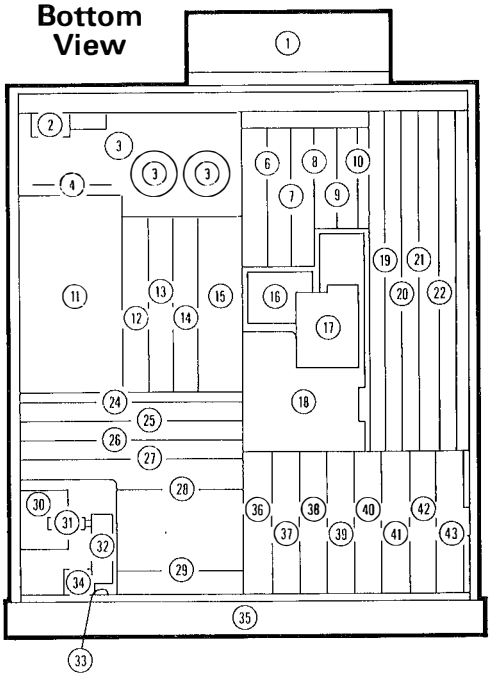
Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

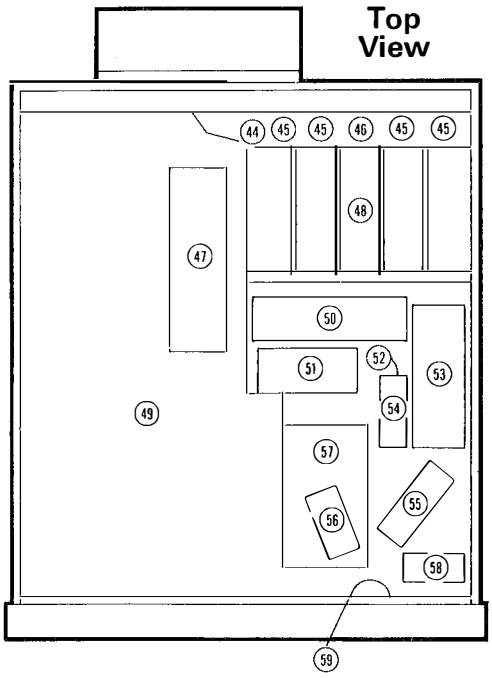
Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 3					Volume 4		
			Ref.-M/N Loops	20-30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	33					●			
A2	Display Driver	33					●			
A3	Display Processor	33					●			
A4	Not Assigned	-								
A5	Keyboard	35					●			
A6	Keyboard Interface	35					●			
A7	Lower Keyboard	35					●			
A8	3.7 GHz Oscillator	57						●		
A9	Band 0 Pulse Modulator	56						●		
A10	Directional Coupler	32						●		
A11	Band 1-4 Detector	31						●		
A12	Band 0 Splitter/Detector	34						●		
A13	SYTM (Switched YIG Tuned Multiplier)	30						●		
A14	Band 1-4 Power Amplifier	53						●		
A15	Band 0 Low Pass Filter	52						●		
A16	Band 1-4 Modulator/Splitter	51						●		
A17	Band 0 Mixer	54						●		
A18	Band 0 Power Amplifier	55						●		
		60						●		
A19	Capacitor Assembly	48								●
A20	RF Section Filter	50						●		
A21	Pulse Modulator Driver	29						●		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRO Bias	28						●		
A25	ALC Detector	27						●		
A26	Linear Modulator	26						●		
A27	Level Control	25						●		
A28	SYTM Driver	24						●		
A29	Reference Phase Detector	12	●							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	●							
A31	M/N Phase Detector	14	●							
A32	M/N VCO (Voltage Controlled Osc.)	15	●							
A33	M/N Output	15	●							
A34	Reference-M/N Motherboard	5	●							
A35	Rectifier	4								●
A36	PLL1 VCO (Voltage Controlled Osc.)	36		●						
A37	PLL1 Divider	37		●						
A38	PLL1 IF	38		●						
A39	PLL3 Upconverter	39		●						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		●						
A41	PLL2 Phase Detector	41		●						
A42	PLL2 Divider	42		●						
A43	PLL2 Discriminator	43		●						
A44	YIG Oscillator (YO)	18			●					
A45	Directional Coupler	18			●					
A46	7 GHz Low Pass Filter	18			●					
A47	Sense Resistor Assembly (YO circuit)	47			●					
	(SYTM circuit)	47						●		
A48	YO Loop Sampler	18			●					
A49	YO Loop Phase/Detector	18			●					
A50	YO Loop Interconnect	17			●					
A51	Reference Oscillator	16	●							
A52	Positive Regulator	6								●
A53	Negative Regulator	7								●
A54	YO Pretune/Delay Compensation	8			●					
A55	YO Driver	9			●					
A56	−15V Regulator	10								●
A57	Marker/Bandcross	19					●			
A58	Sweep Generator	20			●					
A59	Digital Interface	21					●			
A60	Processor	22					●			
A61	Not Assigned	23					●			
A62	Motherboard	49				●				
A63	90 dB RF Attenuator	59						●		
AT1	Peripheral Mode Isolator	58						●		
AT2	15 dB Attenuator	18			●					
B1	Fan Assembly	1								●
A62C1-3	Power Supply Filter Capacitors	3								●
FL1	AC Line Module	2								●
A62Q1-4	Power Supply Regulating Transistors	45								●
A62S1	Power Supply Thermal Switch	44								●
T1	Power Supply Transformer	11								●
A62U1	Power Supply Regulator	46								●

SERVICE INTRODUCTION

This Service Introduction provides the troubleshooter with a structured procedure by which an instrument fault may be localized to the appropriate **functional group** (see below). The functional group provides the information required to troubleshoot to the component level. This section contains an "OVERALL THEORY OF OPERATION" and simplified block diagram. These are used in conjunction with the "OVERALL INSTRUMENT TROUBLESHOOTING," and "TROUBLESHOOTING AIDS" to determine the cause of the instrument failure. Information on safety and repair procedures is also included in this Service Introduction. Refer to the "SERVICE SECTION FORMAT" description, below.

The HP 8340A Service Section is divided into eight sub-sections called functional groups. Four of these are listed on the front of each Service section tab along with a chart that shows which individual assemblies they contain and where these assemblies are located.

The tab for each of the eight functional groups provides an outline of the functional group's contents. Typically this includes an introduction, overall theory of operation, simplified block diagram, and a troubleshooting block diagram.

This is followed by a description of each assembly in the functional group. Each assembly description contains an overall theory of operation, simplified block diagram, component layout, pin I/O table and schematic diagram.

A Major Assembly and Component Locations diagram is provided at the end of each volume.

ATTENTION

In order to avoid unnecessary troubleshooting, verify the instruments internally stored calibration constants. If these constants have been incorrectly modified, the instrument may activate an error annunciator. To do this, first remove the hard copy of the calibration constants from the metal bracket inside the instrument on the left hand side panel (as viewed from the front). Compare these to the constants stored in memory per the instructions in the "CALIBRATION CONSTANTS" section, "Instrument User Access," step 1.

SERVICE SECTION FORMAT

INTRODUCTION

The HP 8340A Service Section is structured to minimize the time it takes to troubleshoot a problem. The following text describes the format of the Service Section and provides important information concerning its use.

SECTION FORMAT

General Information

The beginning of Section VIII contains general information concerning safety, required tools, and the location of instrument interconnects and mnemonics.

Overall Theory of Operation

An Overall Instrument Theory of Operation is supplied that includes an overall block diagram of the instrument. A description of the instrument's stored Calibration Constants is also provided.

Troubleshooting Aids

This part of Section VIII contains descriptions of the troubleshooting aids that are built into the instrument. These aids are: the instrument Self-Test, Digital Signature Analysis (DSA), Direct I/O Addressing, and front panel Diagnostics.

Overall Instrument Troubleshooting

This is the single most important part of the Service Section. This troubleshooting guide will allow the repair person to begin troubleshooting with a symptom and lead him or her to one of the eight major functional areas of the instrument (see below). In many cases this guide leads the troubleshooter directly to the faulty assembly.

Repair

This section contains warnings and cautions concerning the repair of the HP 8340A. It is extremely important that these precautions are implemented when repairing the instrument. A description of the microcircuit field exchange program and after-service safety checks is also included.

Major Functional Group Service Sections

A functional group is a group of assemblies that work in conjunction with one another to perform a certain task. There are eight such groups in the HP 8340A. These are:

- Reference Loop - M/N Loop
- 20-30 Loops
- Sweep Generator - YO Loop
- Motherboard - Wiring List
- Controller Section
- Front Panel - Rear Panel
- RF Section (Power Level Control)
- Power Supplies - Fan

These sections are further divided into overall troubleshooting guides, one for each of the above functional groups. Each of these guides contains the theory of operation and block diagrams for the functional group as a whole. This is followed by a service guide for each asssembly that makes up that functional group. These assembly level service guides contain; theory of operation, troubleshooting information, block diagrams, a component location diagram, a pin I/O table, and a schematic diagram.

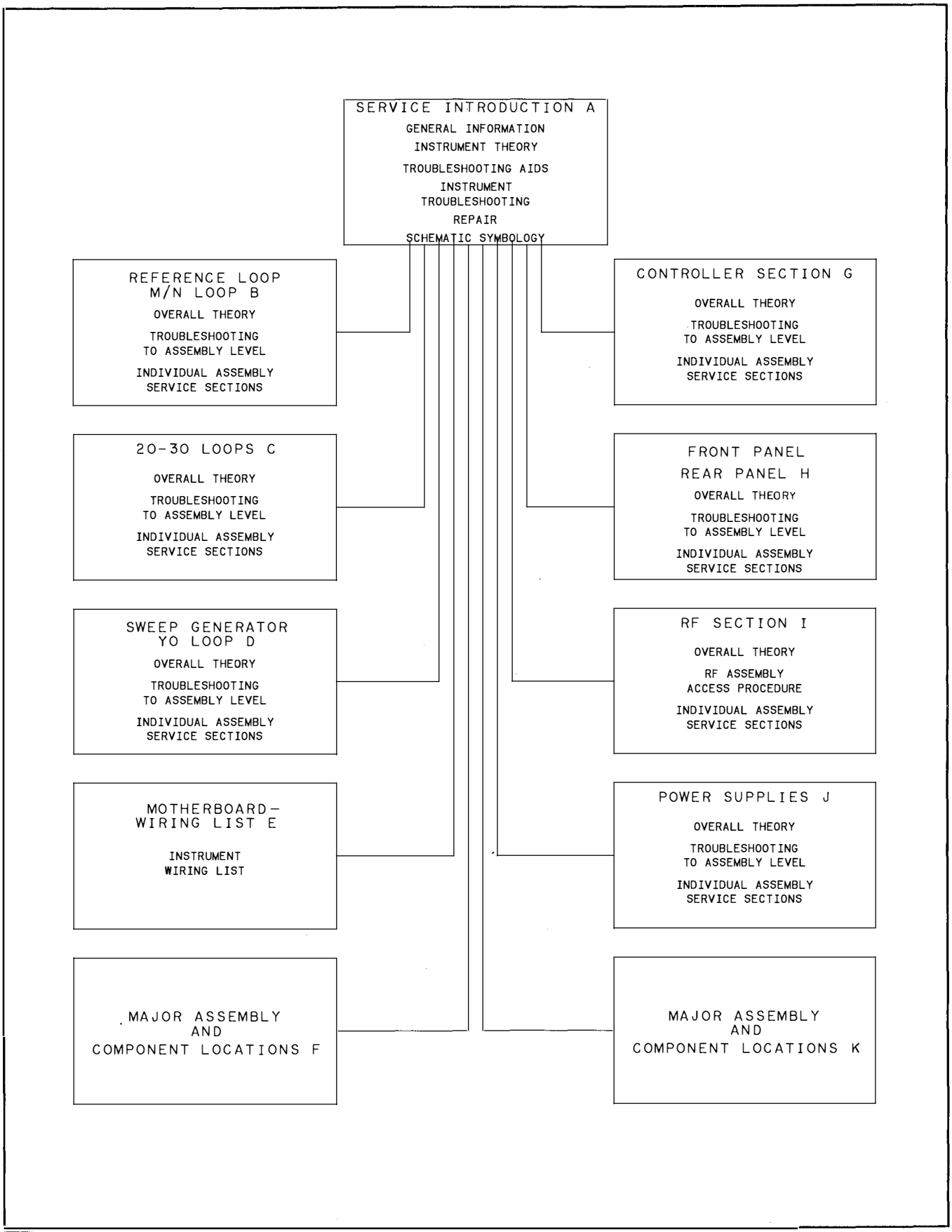


Figure 8A-1. Service Section Format

WARNING

When connected to ac mains, there are voltages at points inside the instrument that can cause personal injury or even death. Any servicing of this instrument with protective covers removed should be performed only by trained personnel who are aware of the hazard involved.

If the A19 POWER-ON SAFETY INDICATOR LED is on, there are voltages present inside the instrument (the A62 Motherboard, the A35 and A19 Rectifier Assemblies, line filter module/transformer wiring, etc.) that can cause injury or even death.

Whenever the instrument is connected to ac mains, the A19 and A35 rectifiers, as well as the A35 +22V REGULATOR, are fully operational. All filter capacitors are charged to full potential. This is true regardless of the position of the POWER switch. Only the A52, A53, and A56 regulators are turned off when the POWER switch is set to STANDBY.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from ac mains. The A19 POWER-ON SAFETY INDICATOR indicates that the filter capacitors on the A19 assembly are sufficiently charged to constitute a shock hazard. Wait until this LED is out before touching any internal components. The filter capacitors on the A35 RECTIFIER assembly bleed-off faster than the A19 capacitors. Therefore, by the time the A19 POWER-ON SAFETY INDICATOR LED is dark, (and the A35 assembly is connected to all of its normal loads) the A35 capacitors have had time to discharge.

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury or even death. (Grounding one conductor of a two conductor outlet is not sufficient protection). Whenever it is likely that this protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

If this instrument is to be energized via an autotransformer, make sure the common terminal is connected to the earth terminal of ac mains.

For continued protection against fire hazards, replace the LINE fuse only with 250V normal blow fuses with the proper current rating. Do not use repaired fuses or short circuited fuseholders.

CAUTION

Never short a capacitor with a screwdriver or similar direct short. Instead, either wait for the capacitor to bleed off via normal instrument loads or, if this is not convenient, provide a discharge path by applying a 0.5 watt, 100 ohm resistor (via shielded clip leads) across the capacitor terminals.

GENERAL INFORMATION

TOOLS REQUIRED

As mentioned above, a soldering station equipped with a grounded tip as well as a low static solder removal tool are required. The Ungar HOT VAC or equivalent is recommended for removing motherboard connectors. Other than these items, no special equipment is needed that isn't provided in the Service Kit (HP Part Number 08340-60134). Table 8A-1 is a list of the tools included in this kit:

Table 8A-1. Tools Supplied in Service Kit

Item	Description	HP Part Number
Adapters	APC-3.5 Female to Female APC-3.5 Female to Type N Male	5061-5311 1250-1744
Adapter Tee	SMB Male-Male-Male	1250-0670
PC Board Extenders	24-pin 30-pin 36-pin 44-pin 48-pin 62-pin 110-pin	08340-60095 08505-60041 08505-60042 08350-60031 08340-60050 08340-60096 08340-60033
IC Test Clip	16-pin 20-pin	1400-0734 1400-0979
Adjustment Tool	Fits adjustment slot on components	8830-0024
Service Cables	BNC (Male) to SMB (Female) (2 required) 61 mm (2 ft), 0.85 in., semi-rigid, SMA Male to SMA Male (2 required) 30 mm (12 in) SMB (Female) to SMB (Female)	85680-60093 08340-20124 5061-1022
Nut Driver	9/16 inch, to replace front panel BNC nuts	08340-20099
Wrench	5/16-inch slotted box/open end	08555-20097

Table 8A-2. Equipment Not Supplied in Service Kit

Item	Description	HP Part Number
RMA Solder	Rosin Mildly Activated	8090-0587
EDSYN SILVERSTAT	Low static solder removal tool	8690-0227
Replacement Tip	For low-static solder removal tool	8690-0253
Wrist Strap	Anti-static wrist strap, 4 ft cord and alligator clip	9300-0791

INTERCONNECT CABLES AND MNEMONICS

All interconnect cables and their associated connectors are listed in Table 8E-1, located within the A62 Motherboard Functional Group.

Table 8E-1 alphabetically lists and defines all HP 8340A signal mnemonics, references the point-to-point distribution of each signal to and from the PC board sockets and the cable connectors on the A62 Motherboard assembly, and identifies the signal source. This table is located in the A62 Motherboard Functional Group.

HP 8340A OVERALL INSTRUMENT THEORY

INTRODUCTION

Refer to Figure 8A-2, HP 8340A Block Diagram.

The HP Model 8340A is a synthesized sweeper that covers the frequency range from 10 MHz to 26.5 GHz in five bands. These bands are:

- Band 0 (10 MHz to 2.3 GHz)
- Band 1 (2.3 to 7.0 GHz)
- Band 2 (7.0 to 13.5 GHz)
- Band 3 (13.5 to 20.0 GHz)
- Band 4 (20.0 to 26.5 GHz)

Internal to the HP 8340A are 7 phase-lock loops, 16 high frequency microcircuits, and a 16 bit microprocessor. these provide the capability of broadband sweeps and the frequency accuracy of a high-performance synthesizer.

REFERENCE LOOPS

The HP 8340A's frequency accuracy and stability are tied to either the 10 MHz internal frequency standard or an external 10 MHz source. The Reference Loop uses this 10 MHz source to generate all of the translation and reference signals that are used by other phase-lock loops inside the instrument. These signals are:

- 400 MHz and 20 MHz signals used in the M/N Loop to produce the M/N output frequency.
- 10 MHz and 100 MHz signals used as reference signals in the 20-30 Loops.
- A separate, lower power 100 MHz output sent to the RF Section for phase locking the 3.7 GHz Oscillator to the 10 MHz Reference.

M/N LOOP

The M/N Loop produces an output between 177-197 MHz. This M/N output drives a Sampler in the YO Loop. The variables "M" and "N" are integers generated by the processor and control the output frequency of the M/N Loop. The output from the Sampler in the YO Loop must always be between 20-30 MHz for the instrument to phase-lock. With the YO at a specific frequency between 2.3 and 7.0 GHz there will be an M/N output frequency between 177 and 197 MHz. When a harmonic of this frequency is mixed with the YO frequency in the Sampler, an IF output between 20-30 Mhz will result. the Sampler output is then compared to the 20-30 Loop output by the YO Loop Phase/Frequency detector in the YO Loop.

20-30 LOOPS

The 20-30 Loops contain 3 phase-locked loops that are used in conjunction with one another to provide the HP 8340A YO Loop with 1 Hz CW resolution, and with analog sweep widths from 100 Hz to 5 MHz. For sweep widths $\leq$5 MHz the YO Loop remains phase-locked during the sweep, and the 20-30 Loop is swept the desired amount. For sweep widths $\geq$5 MHz, all phase-lock loops lock at the beginning of sweep, the 20-30 Loop remains fixed, and the YO is swept. This is called Lock and Roll and will be discussed later.

The 20-30 Loop generates an output between 20-30 MHz in CW mode and 15-30 MHz when the 20-30 Loop is swept. This loop has an output resolution of 1 Hz. Comparing and locking the down-converted YO frequency to the 20-30 output produces a 1 Hz resolution in the YO frequency.

YO LOOP

The YO Loop contains the YIG Oscillator (YO) that is the tunable local oscillator source for all frequency bands. When the HP 8340A is set to a specific CW frequency, the processor sets the frequency of the M/N and 20-30 Loops accordingly. It also sets the YO pretune voltage which tunes the YO to the approximate frequency.

The output of the YO is fed through the directional coupler to the RF Section. The directional coupler splits off part of the YO signal which goes to the Sampler. The M/N output frequency and its harmonics are mixed with the YO frequency in the Sampler to produce an IF signal between 20-30 MHz. The 20-30 MHz IF from the Sampler is compared to the 20-30 Loop output in the Phase/Frequency Detector. The error-induced voltage from the Phase/Frequency Detector is fed through a sample/hold and is summed with the pretune voltage that drives the YO tuning coils. The YO Frequency changes until the output voltage from the Phase/Frequency Detector goes to zero and phase-lock is achieved. For sweep widths greater than 5 MHz, the YO is phase-locked at the start of the sweep. The sample/hold is then set to hold, breaking the loop, and allowing the YO to sweep. The Sweep Generator initiates a Voltage-Sweep (VSWP) ramp that is summed with the YO pretune voltage. This voltage causes the YO to sweep to the STOP frequency. This action is referred to as Lock and Roll. During multi-band sweeps, the YO will again phase-lock at the start of each band before continuing on with the sweep, thus ensuring frequency accuracy across the full range of the HP 8340A.

CONTROLLER SECTION

The Controller Section performs all of the data transfer and coordinates the control signals that operate the HP 8340A. It contains a 16 bit microprocessor, a total of 34K x 16 ROM and 8K x 16 RAM. This section also contains interface circuitry for communicating with the rest of the instrument.

Digital information is exchanged between the microprocessor and other sections of the instrument on a bidirectional bus. In the power-on condition or at Instrument Preset, the controller runs through an instrument self-test. The microprocessor will also set the front panel controls to preset conditions if Instrument Preset was pressed.

The rear panel interface signals, such as the HP-IB bus, SWEEP OUTPUT, Z-AXIS, and others are also routed through or generated in the Controller functional group. The sweep control signal from the controller stops and starts the Sweep Generator. As previously mentioned, during bandcrossings, the sweep must be stopped to phased lock the YO before the sweep can continue. The controller monitors sweep events such as bandcrossings, end of sweep, and markers. It then executes specific instructions according to each type of sweep event.

FRONT PANEL

The front panel contains both the displays and the keyboard as well as some interface connectors. The display has a dedicated microprocessor that keeps the display refreshed and updated. When the instrument processor places display data into the display interface latch, it signals the display processor that some information is ready. The display processor immediately takes the data from the latch and stores it in internal memory. The data will be handled when the display processor has time. The keyboard communicates directly with the instrument processor. When a key is pressed, the instrument processor will either execute that key (if it is a single key operation), or wait for completion of the key sequence. Different key sequences not only allow the operator to set up the HP 8340A for normal operation but also allow access to internal registers, latches, D to A converters, and calibration constants for troubleshooting.

RF SECTION

The RF Section contains the microcircuits and control circuits that produce the 10 MHz to 26.5 GHz RF OUTPUT from the 2.3 to 7.0 GHz YO loop output.

RF output from the directional coupler in the YO loop is fed to the Modulator/Splitter (Mod/Splitter) in the RF Section. Band 0 (10 MHz to 2.3 GHz) is the heterodyne band and is produced by mixing a swept LO Drive from the Mod/Splitter with the phase-locked 3.7 GHz Oscillator output. The IF signal from the Band 0 Splitter/Detector is routed through the Switched-YIG-Tuned Multiplier (SYTM), the Band 1-4 Coupler, and the 90 dB Step Attenuator before reaching the RF OUTPUT connector. The SYTM and Band 1-4 Coupler perform no function in this band. Option 001 and 005 instruments do not have a Step Attenuator.

Band 1 (2.3 to 7.0 GHz) is the same as the YO frequency range. The RF from the Band 1-4 output on the Mod/Splitter is amplified by the Band 1-4 Power Amplifier and passes through the SYTM to the Band 1-4 Coupler. Here, part of the RF is coupled to the Band 1-4 Detector for leveling through the ALC Loop. After the coupler, the RF passes through the 90 dB Step Attenuator (on instruments so equipped) to the RF OUTPUT.

Bands 2-4 (7.0 to 26.5 GHz) are generated by multiplying the YO frequency in the SYTM. A Step Recovery Diode (SRD) in the SYTM, when biased properly, generates harmonics of the input signal. A YIG-Tuned filter tracks the desired harmonic allowing it to pass through to the Band 1-4 Coupler and Step Attenuator (if equipped with Step Attenuator) to the RF OUTPUT. The SYTM Driver provides the necessary circuitry so the YIG-Tuned filter in the SYTM can track the YO properly. Leveling in Bands 2-4 is the same as in Band 1.

Pulse modulation in the HP 8340A is produced by the Pulse Modulator Driver and two fast response time pulse modulators. The Band 0 Pulse Modulator, located just before the Band 0 Mixer, is used when the HP 8340A is operating below 2.3 GHz. Operation above 2.3 GHz uses the Band 1-4 Pulse Modulator inside the Mod/Splitter.

POWER SUPPLIES

The power supply in the HP 8340A produces eight regulated voltage levels, four positive supplies and four negative supplies. These voltages are +22, +20, +12, +5.2, −5.2, −10, −15, and −40 volts. The +22 volt supply powers the 10 MHz Reference Oscillator heater coil. This is the only supply that actually produces an output when the HP 8340A is switched to **STANDBY**. All supplies except for the +22 volt supply are referenced either directly or indirectly to the +20 volt supply. In **STANDBY** mode, the +20 volt supply shuts down. This in turn shuts down the regulators for all other supplies (except the +22 volt supply). However, it is important to note that even though these supplies are "shut down," all of the unregulated supply circuits are fully operational. Therefore, hazardous voltages exist in these sections of the instrument even when the front panel **POWER** switch is set to **STANDBY**. The +20, −15, −10, and −40 volt supplies deliver current to the low noise analog circuits and the microcircuits. The +12, +5.2, −5.2, and −15 volt supplies deliver power to the digital and non-critical analog circuits. Over temperature protection, current limit, and over voltage protection are built into each supply. The output voltage of each supply (excluding the +22 volt supply) is monitored. If any of these supplies drop out of regulation, the instrument microprocessor is flagged.

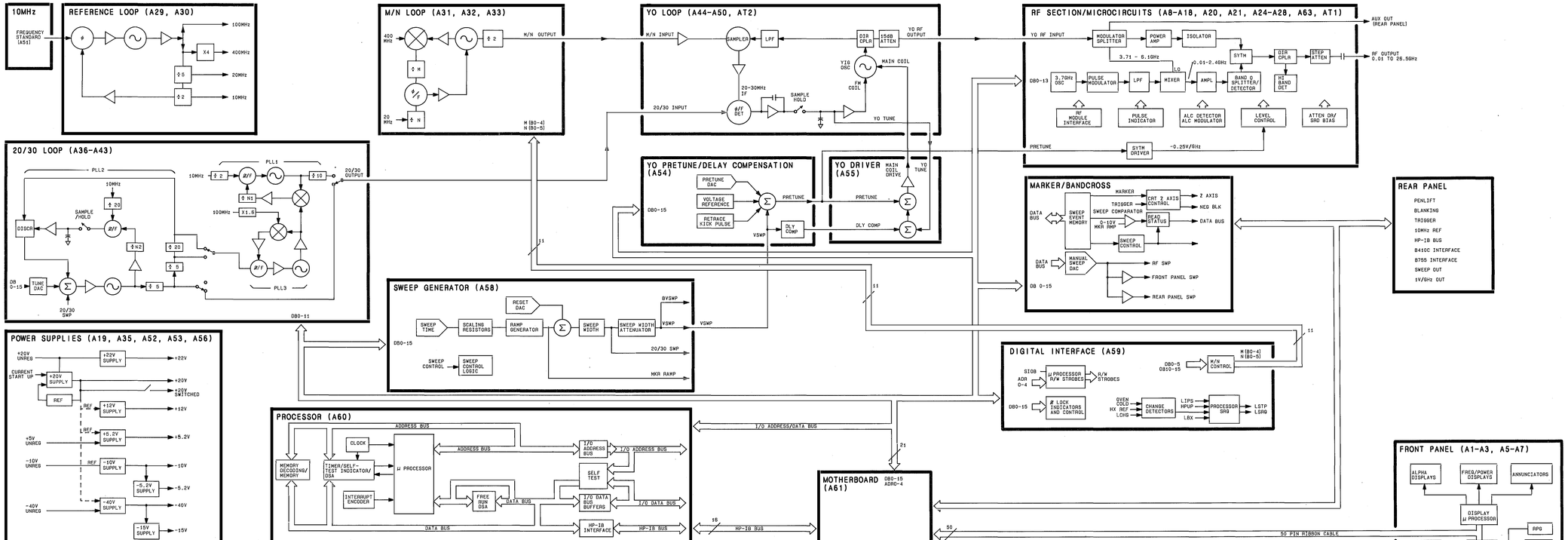


Figure 8A-2. Model 8340A Block Diagram

CALIBRATION CONSTANTS

Introduction

There are three sets of Calibration Constants maintained by the HP 8340A which contain the calibration data, serial number, option, HP-IB Address, and CHECKSUM information. The three sets of Calibration Constants are:

* Working Data
* Protected Data
* Default Data

Working Data contains the calibration information that is required for optimum performance of the HP 8340A. This is the only set of Calibration Constants that is accessed during normal operation of the HP 8340A. It is stored in RAM on the A60 Processor Assembly and maintained by battery A60BT1.

Protected Data contains calibration information which is accessed by the instrument if there is a problem with the Working Data or accessed by the user to update the data. The Protected Data is typically an exact duplicate of the Working Data and acts as a backup in the event an error occurs in the Working Data. Protected data is stored in EE-PROM on the A60 Processor Assembly.

Default Data differs from the Working and Protected Data in that its calibration data is the average calibration data of several HP 8340As. This is done to ensure that if any HP 8340A goes to Default Data, it will still be fairly close to its required calibration data for normal operation. This data is stored in UV-EPROM on the A60 Processor Assembly. The only instance where the instrument would select Default Data would be if a problem existed with both the Working and Protected Data.

Instrument and User Access

During normal operation, the HP 8340A will access the Working Data to obtain the calibration information required for optimum operation of the instrument. In addition to this, the HP 8340A will access the Working Data after an **[INSTR PRESET]** is initiated, and only to verify that the CHECKSUM (Cal Constant #99) is accurate (see Figure 8A-3, Instrument Preset Calibration Constant Verification Sequence).

When **[INSTR PRESET]** is pressed, the Working Data Cal Constants 1 through 98 are summed and then complemented. The result is then compared with the CHECKSUM. If the two numbers agree, the instrument continues normal operation. If not, the Protected Data is written into the Working Data's memory location and the CHECKSUM test is repeated. If the checksum test passes, the data that was in Protected Data is now stored as Working and Protected Data and displayed in the ENTRY DISPLAY will be "CALIBRATION RESTORED." If the CHECKSUMs do not agree, the Default Data is then written to the Working Data. The Working Data now contains the Default values, the FAULT light on the HP 8340A front panel is lit, and "CAL DEFAULTED" is displayed. Pressing **[SHIFT] [MANUAL]** will display the FAULT diagnostics in the ENTRY DISPLAY and the CAL light will be flashing. (Note that the Protected Data was not changed. For troubleshooting, this data may be written into the Working Data (per procedure #5 below) and viewed (per procedure #1 below)).

CAUTION

The following describes methods for intentionally changing the values of the Cal Constants. When a Cal Constant is changed, the CHECKSUM is automatically updated. If a CAL FAULT occurs and a Cal Constant is updated, on the next [INSTR PRESEST] (unless otherwise stated), the CAL FAULT indicator will turn off. This means that if only a few of the Cal Constants were updated, the balance will still be using Default Data.

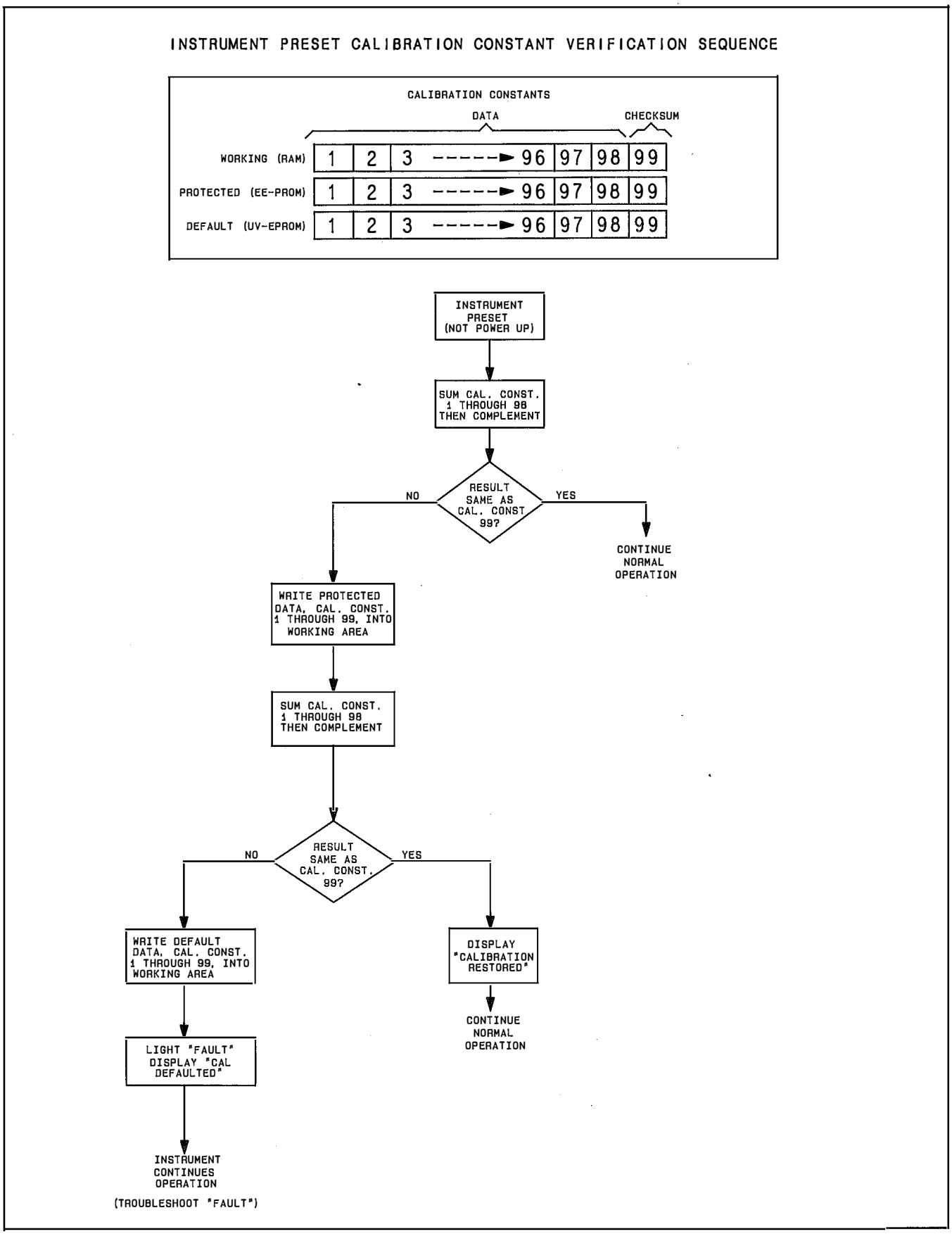


Figure 8A-3. Instrument Preset Calibration Constant Verification Sequence

A number of methods exist for user access of the Cal Constants. A description of each follows:

1. CALIBRATION CONSTANT ACCESS

   [SHIFT] [MHz] [1] [2] [Hz]
   (I/O SUBCHANNEL: 12 displayed in ENTRY DISPLAY)

   [SHIFT] [kHz] [2] [2] [Hz]
   (I/O WRITE: 22 displayed in ENTRY DISPLAY)

   Performing this key sequence allows the user direct access to the Working Data. At this point the data may either be viewed or changed. Immediately after entering the final [Hz], a Cal Constant number and value for that specific Cal Constant will be displayed on the HP 8340A ENTRY DISPLAY. Using the up and down [STEP] keys allows the rest of the Cal Constants to be viewed. For immediate access to a specific Cal Constant, press **[SHIFT] [GHz]** (I/O CHANNEL: XX displayed in ENTRY DISPLAY), enter the number of the desired Cal Constant, and then press **[Hz]** prior to beginning the above key sequence. To change a Cal Constant, use the **[STEP]** keys to move to the desired Cal Constant. Then use either the RPG or the ENTRY keyboard to enter a new value. After the desired value is reached, press **[Hz]**. At this point the Cal Constant value is changed and the CHECKSUM is updated. Note that using this method only changes the Working Data. To permanently change the Protected Data, the procedure described in #4 must be followed.

2. HP-IB ADDRESS ACCESS

   [SHIFT] [LOCAL]

   Performing this key sequency allows the HP-IB address to be viewed in the ENTRY DISPLAY. By rotating the RPG or by keyboard entry, the HP-IB address may be changed from 00 to 30. When the desired address is set, press the **[Hz]** key and the HP-IB address will be changed and the CHECKSUM updated (note that only the Working Data is updated). To prevent the HP-IB address from being changed in this manner, bit 5 of Cal Constant #57 may be set and this function is disallowed. The procedure for doing this is:

   a. Access the Working Data Cal Constant #57 as described in #1.
   b. Set bit 5 by adding 32 to the HP-IB address. Enter this value.
   c. Press **[Hz]**.

3. AUTOMATIC SYTM TO YTO TRACKING (POWER OPTIMIZATION)

   [SHIFT] [PEAK]

   Performing this key sequence causes an automatic SYTM Tracking to be performed. This function automatically adjusts and updates the YTM GAIN Cal Constants (#9 through #12 and #50 through #53) for peak RF output power and then updates the CHECKSUM. This function will also automatically turn off the CAL FAULT indicator without performing an **[INSTR PRESET]** as described in the above note.

4. WORKING DATA TO PROTECTED DATA TRANSFER

   [SHIFT] [MHz] [1] [4] [Hz]
   [SHIFT] [kHz] [5] [3] [4] [9] [Hz]

   Performing this key sequence causes the CHECKSUM of the Working Data to be recalculated and stored. The Working Data is then written over the Protected Data and stored as Protected Data. This is the only method for updating the Protected Data. If this transfer of data fails, the message "EEROM FAILURE, CAL NOT STORED" will be displayed in the ENTRY DISPLAY.

5. PROTECTED DATA TO WORKING DATA TRANSFER

   [SHIFT] [MHz] [1] [4] [Hz]
   [SHIFT] [kHz] [1] [9] [4] [6] [Hz]

   Performing this key sequence causes the HP 8340A to recall the Protected Data and store it in the Working Data memory location.

6. SAVE/RECALL REGISTER INITIALIZATION

   [SHIFT] [MHz] [1] [8]
   [SHIFT] [kHz] [0] [Hz]

   Performing this key sequence, switching the HP 8340A off then on, and then pressing **[INSTR PRESET]** forces the HP 8340A to reinitialize the Save/Recall Registers in RAM (this function does not effect the Cal Constants).

7. CAL CONSTANTS PASSWORD ENABLE

   [SHIFT] [GHz] [8] [2] [Hz]
   [SHIFT] [MHz] [1] [2] [Hz]
   [SHIFT] [kHz] [2] [2] [Hz]
   [−] [2] [3] [8] [7] [5] [Hz]

   The above key sequence accesses Cal Constant number 82 (LOCKWORD ENABLE) and sets it to −23,875. This enables the lockword function and sets Cal Constant number 81 (LOCKWORD) to 0. To change the LOCKWORD (password), access Cal Constant number 81 by pressing the down arrow STEP key. Enter a number between −32,768 and 32,767 via the ENTRY keyboard and terminate the entry with **[Hz]**. The number entered will be the password required to access the calibration constants. After this, remove number A59W1 on the A59 Digital Interface assembly. This is the final step in enabling the Cal Constants' lockword function. In the event that the password is forgotten, re-installing jumper A59W1 will disable the lockword function.

8. CALIBRATION CONSTANT ACCESS WHEN LOCKWORD FUNCTION IS ENABLED

   [SHIFT] [MHz] [2] [0] [Hz]

   This key sequence allows access to the location (sub-channel) where the password for access to the Cal Constants will need to be entered. After pressing the above key sequence, enter the password via the ENTRY keyboard and press **[Hz]**. Upon entry of the correct password, the Cal Constants may be accessed per procedure #1 described previously.

Description

A listing and description of the Cal Constants is given in Table 8A-3. The values that are given in the "Range" column represent the amount of adjustment that is possible with the Cal Constant. The numbers that are shown are the only ones that should be entered by the user. It is possible to enter values out of the given range, but they will not represent the value being used by the HP 8340A. The column labeled "Significance" gives the units associated with the Cal Constant. For example, the value entered for DWELL TIME represents the number of milliseconds that the HP 8340A will wait, after phase lock at the beginning of a sweep or at bandcross, before it will continue its sweep. Another example is the 9GZ SLOPE. For each count, a power compensation of 0.0025 dB/GHz will be added to the RF output. In other words, if 10 were entered for the Cal Constant, a 0.025 dB/GHz slopoe (10 times 0.0025 dB/GHz) would be added for a sweep within the 9 to 20 GHz range.

Five of the Cal Constants, PRESET OPTION (#56), HPIB ADDRESS (#57), RETRACE DWELL (#58), ATTEN CONFIG (#59), and CONFIGURATION (#60) use their bit configuration to store more than one piece of information for the HP 8340A. For example, the HPIB ADDRESS sets up the HP 8340A's HP-IB address and allows or disallows the **[SHIFT] [LOCAL]**, **[SHIFT] [SAVE]**, and **[SHIFT] [RECALL]** functions. If a user wished to set up an HP-IB address of 19, disallow the **[SHIFT] [LOCAL]** and **[RECALL]** functions, and allow the **[SHIFT] [SAVE]** function, the user would enter 179 for Cal Constant #57. The 179 was arrived at by adding 19 (HP-IB address), 32 (disallows **[SHIFT][LOCAL]**), 0 (allows **[SHIFT] [SAVE]**), and 128 (disallows **[SHIFT] [RECALL]**). The other four Cal Constants work in the same manner.

A hard copy of the HP 8340A's Protected Data is included in a plastic envelope with each instrument. It is stored in a bracket which is located underneath the top cover, on the side of the instrument. If the Working and Protected Data are ever lost, the information on this sheet should be used to restore the Cal Constants. Also, when the HP 8340A is recalibrated, the hard copy of the Protected Data should be updated and placed back into the instrument (remember to update the Protected Data). A sample of the hard copy that is included with the instrument is shown in Figure 8A-4.

8340A CALIBRATION CONSTANTS

SERIAL NUMBER; 9999 **8340AREV 08 JAN 85**

1.	DWELL TIME	50	34.	AT90 SLOPE	−12	67.	AT60 SLP 20GZ	10
2.	YTM BX DLY 2	112	35.	unused	0	68.	AT70 SLP 20GZ	13
3.	YTM BX DLY 3	131	36.	unused	0	69.	AT80 SLP 20GZ	13
4.	YTM BX DLY 4	125	37.	unused	0	70.	AT90 SLP 20GZ	18
5.	YTM DLY 1	89	38.	unused	0	71.	YTM OFFSET 1	1024
6.	YTM DLY 2	100	39.	ADC GAIN LO	−33	72.	YTM OFFSET 2	1024
7.	YTM DLY 3	117	40.	ADC GAIN HI	−28	73.	YTM OFFSET 3	1024
8.	YTM DLY 4	104	41.	MAX SWEEP RATE	600	74.	YTM OFFSET 4	1024
9.	YTM GAIN 1	755	42.	ADC OFFSET	−36	75.	YTM TC GAIN	25
10.	YTM GAIN 2	859	43.	AM OFFSET	0	76.	YTM TC OFFSET	1000
11.	YTM GAIN 3	772	44.	LVL DAC OFF; INT	33	77.	YTM TC BKP GAIN	175
12.	YTM GAIN 4	990	45.	LVL DAC OFF; EXT	2	78.	YTM TC BKP FREQ	50
13.	LO SLOPE	40	46.	LVL DAC GAIN; LO	8	79.	OI MODEL	1
14.	HI SLOPE	119	47.	LVL DAC GAIN; HI	3	80.	unused	0
15.	9GZ SLOPE	100	48.	LVL DAC GAIN; EXT	26	81.	LOCKWORD	0
16.	20GZ SLOPE	215	49.	PWR SWP GAIN	1	82.	LOCKWORD ENABLE	0
17.	AT10 OFFSET	−2	50.	YTM BX GAIN 1	890	83.	unused	0
18.	AT20 OFFSET	−5	51.	YTM BX GAIN 2	791	84.	unused	0
19.	AT30 OFFSET	−1	52.	YTM BX GAIN 3	1030	85.	unused	0
20.	AT40 OFFSET	−4	53.	YTM BX GAIN 4	990	86.	unused	0
21.	AT50 OFFSET	−7	54.	STOP LIMIT	20000	87.	unused	0
22.	AT60 OFFSET	−2	55.	START LIMIT	10	88.	unused	0
23.	AT70 OFFSET	−5	56.	PRESET OPTION	0	89.	unused	0
24.	AT80 OFFSET	−7	57.	HPIB ADDRESS	531	90.	unused	0
25.	AT90 OFFSET	−10	58.	RETRACE DWELL	0	91.	unused	0
26.	AT10 SLOPE	−2	59.	ATTEN CONFIG	20980	92.	unused	0
27.	AT20 SLOPE	−4	60.	CONFIGURATION	23	93.	unused	0
28.	AT30 SLOPE	−3	61.	SERIAL #	9999	94.	unused	0
29.	AT40 SLOPE	−5	62.	AT10 SLP 20GZ	4	95.	unused	0
30.	AT50 SLOPE	−7	63.	AT20 SLP 20GZ	5	96.	unused	0
31.	AT60 SLOPE	−60	64.	AT30 SLP 20GZ	5	97.	unused	0
32.	AT70 SLOPE	−8	65.	AT40 SLP 20GZ	8	98.	MODEL #	0
33.	AT80 SLOPE	−10	66.	AT50 SLP 20GZ	9	99.	CHECKSUM	9557

Procedure for manually entering calibration data into the HP 8340A:

1. Push the following sequence of KEYS:
   Instrument Preset SHIFT MHz 1 2 Hz SHIFT KHz 2 2 Hz
2. Note the Entry Display will indicate the Calibration Constant number and value.
3. Enter via the KEY BOARD or DATA KNOB the correct value for the first Calibration Constant indicated in the display.
   ≪ Terminate KEYBOARD entries with the Hz key ≫
4. Go to the next Calibration Constant by pushing the UP step key. The next constant can then be entered. Do not enter the "CHECKSUM" Constant. (This is computed automatically)
5. The Step Keys can be used to move from one Calibration Constant to another to either check them or to correct them.
6. After all entries have been made, check that all numbers are correct by using the step keys to review and verify them.
7. Allow instrument to warm up for 1/2 hour and make sure that nothing is connected to the Stop Sweep connector on the rear panel. Push SHIFT PEAK to perform an Automatic Tracking Calibration. This step may modify the "YTM GAIN n" & "YTM BX GAIN n" consts.
8. The CALIBRATION data should be permanently stored in the Non Volatile Protected Memory by pushing the following key sequence: SHIFT MHz 14 Hz SHIFT KHz 5349 Hz PRESET.

Figure 8A-4. Sample Calibration Constants Hard Copy (Found Inside Instrument)

Table 8A-3. Calibration Constants (1 of 7)

No.	Name	Function	Range (Counts)	Significance
1	DWELL TIME	Defines time to wait after phase lock at beginning of sweep and at bandcross.	0-500	0.2 ms/count
2	YTM BX DLY 2	Compensates for YTM Delay in Band 2 after bandcross from Band 1 to Band 2.	0-131	2.4 MHz/ms/count
3	YTM BX DLY 3	Compensates for YTM Delay in Band 3 after bandcross from Band 2 to Band 3.	0-131	2.4 MHz/ms/count
4	YTM BX DLY 4	Compensates for YTM Delay in Band 4 after bandcross from Band 3 to Band 4.	0-131	2.4 MHz/ms/count
5	YTM DLY 1	Compensates for YTM Delay in Band 1.	0-131	2.4 MHz/ms/count
6	YTM DLY 2	Compensates for YTM Delay in Band 2 for single band sweeps or multi-band sweeps that begin in Band 2.	0-131	2.4 MHz/ms/count
7	YTM DLY 3	Compensates for YTM Delay in Band 3 for single band sweeps or multi-band sweeps that begin in Band 3.	0-131	2.4 MHz/ms/count
8	YTM DLY 4	Compensates for YTM Delay in Band 4 for single band sweep.	0-131	2.4 MHz/ms/count
9	YTM GAIN 1	Adjusts Band 1 in YTM slow speed tracking.	0-2040	−4% - +4% of YTM Frequency
10	YTM GAIN 2	Adjusts Band 2 YTM slow speed tracking.	0-2040	−2% - +2% of YTM Frequency
11	YTM GAIN 3	Adjusts Band 3 YTM slow speed tracking.	0-2040	−1.33% - +1.33% of YTM Frequency
12	YTM GAIN 4	Adjusts Band 4 YTM slow speed tracking	0-2040	−1% - +1% of YTM Frequency
13	LO SLOPE	Slope compensation for RF power in Band 0.	0-255	0.005 dB/GHz/count
14	HI SLOPE	Slope compensation for RF power from 2.3 to 9.0 GHz.	0-255	0.005 dB/GHz/count
15	9 GZ SLOPE	Slope compensation for RF power from 9.0 to 20.0 GHz.	0-255	0.0025 dB/GHz/count
16	20 GZ SLOPE	Slope compensation for RF power from 20.0 to 26.5 GHz.	0-255	0.01 dB/GHz/count
17	AT10 OFFSET	Offset compensation for RF power at 10 dB attenuator setting from 0.01 to 26.5 GHz.	−200 - +200	0.05 dB/count

Table 8A-3. Calibration Constants (2 of 7)

No.	Name	Function	Range (Counts)	Significance
18	AT20 OFFSET	Offset compensation for RF power at 20 dB attenuator setting from 0.01 to 26.5 GHz.	−200 - +200	0.05 dB/count
19	AT30 OFFSET	Offset compensation for RF power at 30 dB attenuator setting from 0.01 to 26.5 GHz.	−200 - +200	0.05 dB/count
20	AT40 OFFSET	Offset compensation for RF power at 40 dB attenuator setting from 0.01 to 26.5 GHz.	−200 - +200	0.05 dB/count
21	AT50 OFFSET	Offset compensation for RF power at 50 dB attenuator setting from 0.01 to 26.5 GHz.	−200 - +200	0.05 dB/count
22	AT60 OFFSET	Offset compensation for RF power at 60 dB attenuator setting from 0.01 to 26.5 GHz.	−200 - +200	0.05 dB/count
23	AT70 OFFSET	Offset compensation for RF power at 70 dB attenuator setting from 0.01 to 26.5 GHz.	−200 - +200	0.05 dB/count
24	AT80 OFFSET	Offset compensation for RF power at 80 dB attenuator setting from 0.01 to 26.5 GHz.	−200 +200	0.05 dB/count
25	AT90 OFFSET	Offset compensation for RF power at 90 dB attenuator setting from 0.01 to 26.5 GHz.	−200 +200	0.05 dB/count
26	AT10 SLOPE	Slope compensation for RF power at 10 dB attenuator setting from 2.3 to 20.0 GHz.	−255 - +255	0.005 dB/GHz/count
27	AT20 SLOPE	Slope compensation for RF power at 20 dB attenuator setting from 2.3 to 20.0 GHz.	−255 - +255	0.005 dB/GHz/count
28	AT30 SLOPE	Slope compensation for RF power at 30 dB attenuator setting from 2.3 to 20.0 GHz.	−255 - +255	0.005 dB/GHz/count
29	AT40 SLOPE	Slope compensation for RF power at 40 dB attenuator setting from 2.3 to 20.0 GHz.	−255 - +255	0.005 dB/GHz/count
30	AT50 SLOPE	Slope compensation for RF POWER at 50 dB attenuator setting from 2.3 to 20.0 GHz.	−255 - +255	0.005 dB/GHz/count

Table 8A-3. Calibration Constants (3 of 7)

No.	Name	Function	Range (Counts)	Significance
31	AT60 SLOPE	Slope compensation for RF power at 60 dB attenuator setting from 2.3 to 20.0 GHz.	−255 - +255	0.005 dB/GHz/count
32	AT70 SLOPE	Slope compensation for RF power at 70 dB attenuator setting from 2.3 to 20.0 GHz.	−255 - +255	0.005 dB/GHz/count
33	AT80 SLOPE	Slope compensation for RF power at 80 dB attenuator setting from 2.3 to 20 GHz.	−255 - +255	0.005 dB/GHz/count
34	AT90 SLOPE	Slope compensation for RF power at 90 dB attenuator setting from 2.3 to 20 GHz.	−255 - +255	0.005 dB/GHz/count
35		UNUSED		
36		UNUSED		
37		UNUSED		
38		UNUSED		
39	ADC GAIN LO	Adjusts front panel dBm display accuracy from .01 to 2.3 GHz.	−100 - +100	−10% - +10%
40	ADC GAIN HI	Adjusts front panel dBm display accuracy from 2.3 to 26.5 GHz.	−100 - +100	−10% - +10%
41	MAX SWEEP RATE	Sets the maximum sweep rate in the AUTO sweeptime mode.	1-1000	1 MHz/ms/count
42	ADC OFFSET	Adjusts front panel dBm display.	−100 - +100	0.05 dB/count
43	AM OFFSET	Modulation level offset for output power accuracy in AM mode.	−100 - +100	0.05 dB/count
44	LVL DAC OFF; INT	Offsets level DAC A27U14 for internal leveling operation.	−100 - +100	0.05 dB/count
45	LVL DAC OFF; EXT	Offsets level DAC A27U14 for external leveling operation.	−100 - +100	0.05 dB/count
46	LVL DAC GAIN; LO	Adjusts gain of level DAC for internal leveling operation in Band 0.	−100 - +100	1% of ALC power (in dBm)/count
47	LVL DAC GAIN; HI	Adjust gain of level DAC for internal leveling operation in Bands 1-4.	−100 - +100	−10.0% - +10.0%

Table 8A-3. Calibration Constants (4 of 7)

No.	Name	Function	Range (Counts)	Significance
48	LVL DAC GAIN; EXT	Adjusts gain of level DAC for external leveling operation.	−100 - +100	−10.0% - +10.0%
49	PWR SWP	Adjust gain of power sweep DAC A27U24 during power sweep operation.	−100 - +100	−10.0% - +10.0%
50	YTM BX GAIN 1	Adjusts YTM slow speed tracking for sweeps which cross from Band 0 to Band 1.	0-2040	−4% - +4% YTM Frequency
51	YTM BX GAIN 2	Adjusts YTM slow speed tracking for sweeps which cross from Band 1 to Band 2.	0-2040	−2% - +2 of YTM Frequency
52	YTM BX GAIN 3	Adjusts YTM slow speed tracking for sweeps which cross from Band 2 to Band 3.	0-2040	−1.33% - +1.33% of YTM Frequency
53	YTM BX GAIN 4	Adjusts YTM slow speed tracking for sweeps which cross from Band 3 to Band 4.	0-2040	−1% - +1% of YTM Frequency
54	STOP LIMIT	Sets maximum allowable stop frequency.	11 - 26,000	1 MHz/count
55	START LIMIT	Sets minimum allowable start frequency.	10-(STOP LIMIT −1)	1 MHz/count
56	PRESET OPTION	Selects instrument's operating conditions.		
		Bits 0 through 7 - Selects power level after **[INSTR PRESET]**.	0-110	0 dBm - −110 dBm
		Bit 10 - PMI Network Analyzer retrace compatibility.	0/1024	Disabled/Enabled
		Bit 12 - CIIL compatibility (if option is installed)	0/4096	Disabled/Enabled
57	HBIB ADDRESS	Selects instrument's operating conditions.		
		Bits 0 through 4 - selects HP-IB address.	00 - 30	Instrument's HP-IB Address
		Bit 5 - allows or disallows the HP-IB address to be changed after entering a **[SHIFT] [LOCAL]**	0/32	Allowed/Disallowed
		Bit 6 - allows or disallows the **[SHIFT] [SAVE]** function.	0/64	Allowed/Disallowed
		Bit 7 - allows or disallows the **[SHIFT] [RECALL]** function.	0/128	Allowed/Disallowed

Table 8A-3. Calibration Constants (5 of 7)

No.	Name	Function	Range (Counts)	Significance
58	RETRACE DWELL	Required for Integra Filter operation.	0-20	10 ms/count
59	ATTEN CONFIG	Selects Attenuator operating conditions.		
		Bits 0 through 9 - selects attenuator switch threshold.	0-1020	0.05 dB/5 counts
		A 0 entry sets the attenuator switch threshold at −14.95 dBm (i.e., in coupled mode, the ALC will go as low as −14.95 dBm. At −15.0 dBm, the ALC is set to −5 dBm and the attenuator switches in 10 dB of attenuation). A 1020 entry sets the attenuator switch threshold at −4.75.		
		Bit 10 - Must be set to 1. This allows attenuator to be operated over 90 dB.	1024	90 dB operation
		Bit 12 - Selects attenuator Installed or not installed.	0/4096	Installed/ Not Installed
		Bit 13 - Must be set to zero.	0	—
		Bit 14 - Selects version of A26 Linear Modulator Assembly Installed. 0 selects P/N 08340-60021, 1 selects P/N 08340-60156.	0/16,384	08340-60021/ 08340-60156
		Bit 15 - Must be set to 0. This selects how attenuator is programmed.	0	Attenuator Programming
60	CONFIGURATION	Selects instrument options		
		Bit 0 - Must be set to zero	0	
		Bit 1 - Without or With Option 001 or 005 (No attenuator option).	0/2	Without/With
		Bit 2 - Without or With Option 004 or 005 (Rear panel option).	0/4	Without/With
		Bit 13 - Without or With C75 Special.	0/8192	Without/With
61	SERIAL #	Storage location for serial number of HP 8340A.	—	—
62	AT10 SLP 20GZ	Slope compensation for RF power at 10 dB attenuator setting from 20 to 26.5 GHz.	−255 - +255	0.01 dB/GHz/ count
63	AT20 SLP 20GZ	Slope compensation for RF power at 20 dB attenuator setting from 20.0 to 26.5 GHz.	−255 - +255	0.01 dB/GHz/ count

Table 8A-3. Calibration Constants (6 of 7)

No.	Name	Function	Range (Counts)	Significance
64	AT30 SLP 20GZ	Slope compensation for RF power at 30 dB attenuator setting from 20.0 to 26.5 GHz.	−255 - +255	0.01 dB/GHz/ count
65	AT40 SLP 20GZ	Slope compensation for RF power at 40 dB attenuator setting from 20.0 to 26.5 GHz.	−255 - +255	0.01 dB/GHz/ count
66	AT50 SLP 20GZ	Slope compensation for RF power at 50 dB attenuator setting from 20.0 to 26.5 GHz.	−255 - +255	0.01 dB/GHz/ count
67	AT60 SLP 20GZ	Slope compensation for RF power at 60 dB attenuator setting from 20.0 to 26.5 GHz.	−255 - +255	0.01 dB/GHz/ count
68	AT70 SLP 20GZ	Slope compensation for RF power at 70 dB attenuator setting from 20.0 to 26.5 GHz.	−255 +255	0.01 dB/GHz/ count
69	AT80 SLP 20GZ	Slope compensation for RF power at 80 dB attenuator setting from 20.0 to 26.5 GHz.	−255 - +255	0.01 dB/GHz/ count
70	AT90 SLP 20GZ	Slope compensation for RF power at 90 dB attenuator setting from 20.0 to 26.5 GHz.	− 255 - +255	0.01 dB/GHz/ count
71	YTM OFFSET 1	UNUSED		
72	YTM OFFSET 2	UNUSED		
73	YTM OFFSET 3	UNUSED		
74	YTM OFFSET 4	UNUSED		
75	YTM TC GAIN	UNUSED		
76	YTM TC OFFSET	UNUSED		
77	YTM TC BKP GAIN	UNUSED		
78	YTM TC BKP FREQ	UNUSED		
79	OI MODEL	Specifies instrument model number outputted when HP-IB "OI" command received.	0 - 2	0=8340A 1=8341A 2=8340A-H02
80		UNUSED		
81	LOCKWORD	Defines password required to access calibration constants.	−32,768 - +32,767	

Table 8A-3. Calibration Constants (7 of 7)

No.	Name	Function	Range (Counts)	Significance
82	LOCKWORD ENABLE	Enables lockword function which is used to allow access to calibration constants only upon input of the correct password (lockword).	0/−23,875	Disabled/ Enabled
83		UNUSED		
84		UNUSED		
85		UNUSED		
86		UNUSED		
87		UNUSED		
88		UNUSED		
89		UNUSED		
90		UNUSED		
91		UNUSED		
92		UNUSED		
93		UNUSED		
94		UNUSED		
95		UNUSED		
96		UNUSED		
97		UNUSED		
98	MODEL #	Instrument model number.	0, 1, 99	0=8340A 1=8341A 99=8340A-HO2
99	CHECKSUM	Serves as check point for Cal Constant Accuracy. The sum of Cal Constants 1 through 98 is calculated, the sum is complemented, and the result is stored as the CHECKSUM.	—	—

TROUBLESHOOTING AIDS

INTRODUCTION

This section contains descriptions of the major HP 8340A troubleshooting aids.

SELF TEST

Self Test verifies the operation of the A60 Processor. It also verifies that address and data information can be transmitted accurately over the Instrument Address Bus and Instrument Data Bus. Refer to the **"OVERALL INSTRUMENT TROUBLESHOOTING"** section for complete information.

DIGITAL SIGNATURE ANALYSIS (DSA)

DSA information, instructions, and signatures are provided for the A60 Processor and various front panel assemblies. This information may be found in the troubleshooting sections for each of those assemblies. Refer to the appropriate functional group and troubleshooting procedure.

PHASE-LOCK INDICATION LEDS

Three green LEDS in the HP 8340A indicate when a phase-lock condition exists for three phase-lock loops. Each LED is lit when its specific loop is phase-locked. The LEDS and phase-lock loops are as follows:

1. A37DS1 - PLL1
2. A39DS1 - PLL3
3. A50DS1 - YO

POWER SUPPLY INDICATION LEDS

Several yellow LEDS indicate when the power supplies are at their required voltage. Each LED is lit when its specific power supply is up. The LEDS and power supplies are as follows:

1. A35DS1 - +22V
2. A52DS1 - +5.2V
3. A52DS2 - +20V
4. A52DS3 - +12V
5. A53DS1 - −5.2V
6. A53DS2 - −40V
7. A53DS3 - −10V
8. A56DS1 - −15V

Three red LEDS indicate when voltage is present on the A19 Capacitor Assembly, when the HP 8340A is in shutdown due to over temperature, and when the AC mains is connected. The LEDS are lit when the respective condition exists. The LEDS and conditions are as follows:

1. A19DS1 - voltage present on A19 Capacitor Assembly
2. A52DS4 - HP 8340A in overtemp condition
3. A62DS1 - AC mains connected

DIRECT I/O ADDRESSING

Refer to the **DIRECT I/O ADDRESSING** description on the following pages.

DIRECT I/O ADDRESSING

Introduction

Direct I/O Addressing is a tool that allows the user to directly access HP 8340A input and output devices from the front panel. It allows the user to exercise these devices and thus verify their operation.

Direct I/O Addressing may only be used when the HP 8340A self test passes (CHECK LED I and II off, see Controller functional group for more information) and the front panel (or HP-IB) is operational. It should be used when the troubleshooting has progressed to the point where the signal path has been determined and a specific I/O device needs to be checked to verify it is or is not the cause of the failure. The required equipment is:

* DVM
* Logic Probe
* Extender Boards
* Jumper Wires

I/O Device Description

Input devices are used to place data on the data bus for use by the processor. These devices consist of the HP-IB Interface and input registers/buffers. To test theses devices using Direct I/O Addressing, a known input must be placed on the device's input and a "read" command executed to cause the data to be placed on the data bus and then displayed in the front panel ENTRY DISPLAY.

Output devices are used to accept data transmitted by the processor on the data bus and then translate and transmit the data in a form required for use in other parts of the instrument. These devices consist of DACs, 3 to 8 decoders, output registers, and flip-flops. To test these devices using Direct I/O Addressing, a known input must be transmited on the data bus by means of a "write" command and the output of the device probed by a logic probe or DVM to verify that the signal was accepted and re-transmitted properly.

Table 8A-4 gives a listing of all the input and output devices that can be accessed by Direct I/O Addressing. The first two columns define the address (Channel/Subchannel) of the I/O Strobe that must be generated to cause the device to be read from or written to. The third column gives the strobe's mnemonic and the fourth column gives the IC from which the strobe is generated. The fifth and sixth columns define the IC that is being accessed (destination of the strobe) and what type of device it is. The final column defines if Direct I/O Addressing can be used for troubleshooting the specific device or if a different troubleshooting section should be referenced. Cross-referencing from an assembly schematic to this table should be done using the I/O Strobe address shown on the schematic. It will be shown on the schematic as

(x,Ry:)

which corresponds to Channel x, Subchannel y in the table.

Table 8A-4. I/O Devices (1 of 3)

I/O Chn	Strobe Subchn	Mnemonic	From IC	Destination IC	Destination Type	Direct I/O Capability
0	0	LCK2	A59U26	A42U14	Output	Yes
0	1	LCK3	A59U26	A43U9	Output	Yes
				A43U12	Output	Yes
0	2	LCK1	A59U26	A42U12	Output	Yes
				A42U13	Output	Yes
0	3	LCK4	A59U26	A36U5	Output	Yes
				A37U9	Output	Yes
				A37U10	Output	Yes
1	0	WSPAT	A59U26	A58U27	Output	Yes
				A58U29	Output	Yes
				A58U31	Output	Yes
1	1	WSPTM	A59U26	A58U23	Output	Yes
				A58U25	Output	Yes
				A58U26	Output	Yes
1	2	WRDAC	A59U26	A58U4	Output	Yes
				A58U19	Output	Yes
				A58U21	Output	Yes
1	3	LRSW	A59U26	A59U23	Output	Yes
2	0		A5U19	No Connection		
2	1		A59U19	No Connection		
2	2	UNASSIGNED				
2	3	UNASSIGNED				
3	0	TYOKP	A59U26	A54U9	Output	Yes
3	1	PHASE LOCK CNTRL	A59U26	A59U24	Output	Yes
3	2	WPDAC	A59U26	A54U11	Output	Yes
				A54U13	Output	Yes
3	3	M/N OSC CONTROL	A59U26	A59U10	Output	Yes
				A59U17	Output	Yes
4	0		A59U12	No Connection		
4	1		A59U10	No Connection		
4	2			No Connection		
4	3	READ STATUS	A59U12	A59U18	Input	Yes
5	0	STOP PROCESSOR	A59U12	A59U4	Output	Yes
5	1	WYOKW	A59U12	A54U9	Output	Yes
				A54U15	Output	Yes

Table 8A-4. I/O Devices (2 of 3)

I/O Chn	Strobe Subchn	Mnemonic	From IC	Destination IC	Destination Type	Direct I/O Capability
5	2	RESET PWR FAIL FF	A59U12	A59U4		No
5	3	WCDAC	A59U12	A54U16	Output	Yes
6	0	LEN 4	A6U15	A6U16		See A6 Service
6	1	LEN 5	A6U15	A6U6		
6	2	LEN 6	A6U15	A6U13 A6U18 A6U19		See A6 Service
6	3	LEN 7	A6U15	A6U11 A6U12		See A6 Service
7		UNASSIGNED				
8		UNASSIGNED				
9		UNASSIGNED				
10	0	WMOD	A27U27	A26U15	Output	Yes
10	1	WLEVEL	A27U27	A24U15 A27U13 A27U16	Output Output Output	Yes Yes Yes
10	2	WBAND	A27U27	A27U28 A28U14	Output Output	Yes Yes
10	3	RLEVEL	A27U27	A27U11 A27U12 A27U15 A27U21	Output Input Input Output	Yes Yes Yes Yes
11	0	WLSWP	A27U27	A27U23 A27U30	Output Output	Yes Yes
11	1	WSYTMSLP	A27U27	A28U15	Output	Yes
11	2	UNASSIGNED				
11	3	WSYTMCTL	A27U27	A28U13	Output	Yes
12	0	WRITE RAM	A57U28	A57U2 A57U15 A57U29	 Output	See A57 Service Yes
12	1	READ STS	A57U28	A57U24	Input	Yes
12	2	READ RAM	A57U28	A57U8 A57U16 A57U29	 Output	See A57 Service Yes

Table 8A-4. I/O Devices (3 of 3)

I/O Chn	Strobe Subchn	Mnemonic	From IC	Destination IC	Destination Type	Direct I/O Capability
12	3	WRITE ADR 3	A57U28	A57U1 A57U10	Output Output	Yes Yes
13	0	TRIGGER SEL	A57U28	A57U18	Output	Yes
13	1	WRITE STROBE	A57U28	A57U25	Output	Yes
13	2	MAN DAC	A57U28	A57U9 A57U17	Output Output	Yes Yes
13	3	WRITE CONTROL	A57U28	A57U23	Output	Yes
14	0	WATNS	A27U20	A27U8	Output	Yes
14	1	UNASSIGNED				
14	2	WBP1S	A27U20	A27U9	Output	Yes
14	3	WBP2S	A27U20	A27U10	Output	Yes
15	0	UNASSIGNED				
15	1	WADCC	A27U20	A27U29	Output	Yes
15	2	UNASSIGNED				
15	3	RSTAT	A27U20	A24714 A27U22	Input Input	Yes Yes

Implementation

STROBE VERIFICATION

The equipment that is required for strobe verification is a logic probe. The procedure is as follows:

1. With the HP 8340A switched to STANDBY, place the appropriate assembly on an extender board. Switch the HP 8340A ON and connect the logic probe to +5V and ground.
2. Press **[INSTR PRESET] [MANUAL]**.
3. Press **[SHIFT] [GHz]** xx **[Hz]**.
   This key sequence sets up the I/O Strobe Channel. Enter the desired Channel number where the xx is located.
4. Press **[SHIFT] [MHz]** yy **[Hz]**.
   This key sequence sets up the I/O Strobe Subchannel. Enter the desired Subchannel number where the yy is located.
5. Press **[SHIFT] [kHz]**.
   This sequence sets up an I/O write and will allow the Strobe to be pulsed.
6. Probe the appropriate IC pin and rotate the RPG. Verify that the probe (Strobe) is pulsing.

OUTPUT REGISTER VERIFICATION

The output registers are the devices which latch the data from the data bus and then transmit it to other parts of the instrument. No other manipulation is done. The equipment that is required to test these devices is either a logic probe or a DVM. The procedure is as follows:

1. Verify the operation of the output register's I/O Strobe as described in the strobe verification procedure.
2. Press **[INSTR PRESET] [MANUAL]**.
   Setting the instrument in MANUAL mode prevents the processor from writing data to the device being tested. This ensures that the data being entered from the front panel is not changed prior to testing the device.
3. Press **[SHIFT] [GHz]** xx **[Hz]**.
   This key sequence sets up the I/O Strobe Channel. Enter the desired Channel number where the xx is located.
4. Press **[SHIFT] [MHz]** yy **[Hz]**.
   This key sequence sets up the I/O Strobe Subchannel. Enter the desired Subchannel number where the yy is located.
5. Press **[SHIFT] [kHz]**.
   This key sequence sets up an I/O write and will allow data to be written to the device being accessed.

NOTE

Steps 6 through 9 assume that the data lines are connected to the output register in sequence. If this is not the case, ensure adjacent output pins are not set to the same logic level (refer to Table 8A-5). If an adjacent pin is high that should be low, subtract the decimal value of the data line from the number given in Table 8A-5a. If an adjacent pin is low that should be high, add the decimal value to the number given in step 6 or 8.

6. Press **[2] [1] [8] [4] [5] [Hz]**.
   This key sequence places alternate 1's and 0's onto the data bus and causes the data to be latched into the output register being accessed. Alternating the 1's and 0's allows the device being tested to be checked for highs and lows on the output and also for output pins that may be shorted together.

7. Using a logic probe or DVM, probe the output pins of the device being tested. Verify that the output pins are set as shown in Table 8A-5b.
8. Press **[−] [2] [1] [8] [4] [6] [Hz]**.
   This key sequence reverses the state of the output pins set in step 6. This verifies that the pins can be set to both TTL levels.
9. Using a logic probe or DVM, probe the output pins of the device being tested. Verify that the output pins are set as shown in Table 8A-5c.

Table 8A-5. Direct I/O Data Bit Information

a. Decimal Values for Set Data Bits.

Data Line	15	14	13	12	11	10	9	8
Decimal Value	−32768	16384	8192	4096	2048	1024	512	256
Data Line	7	6	5	4	3	2	1	0
Decimal Value	128	64	32	16	8	4	2	1

b. Bit Configuration for 21845 Entry.

Data Line	15	14 13 12	11 10 9	8 7 6	5 4 3	2 1 0
Bit Level	0	1 0 1	0 1 0	1 0 1	0 1 0	1 0 1

0 Level Typically <0.3V
1 Level Typically >3.0V

c. Bit Configuration for −21846 Entry.

Data Line	15	14 13 12	11 10 9	8 7 6	5 4 3	2 1 0
Bit Level	1	0 1 0	1 0 1	0 1 0	1 0 1	0 1 0

0 Level Typically <0.3V
1 Level Typically >3.0V

DAC VERIFICATION

The DACs which can be tested using Direct I/O Addressing are those which have a strobe listed in Table 8A-4 and the data bus connected to them. An example of one of these DACs is A54U15. Several other DACs have their data sent from an output register (eg. A54U6). These DACs may be tested in the same manner as described below but all the addressing and data entry must be to the output register. The equipment required is a DVM. The procedure is as follows:

1. Verify the operation of the DAC's I/O Strobe as described in the strobe verification procedure.
2. Press **[INSTR PRESET] [MANUAL]**. A few of the DACs only operate over a specific frequency range (eg. A27U10, frequencies >20 GHz). If this is the case for the DAC being tested, enter the appropriate MANUAL frequency.
3. Press **[SHIFT] [GHz]** xx **[Hz]**.
   This key sequence sets up the I/O Strobe Subchannel. Enter the desired Subchannel number where the xx is located.

4. Press **[SHIFT] [MHz]** yy **[Hz]**.
   This key sequence sets up the I/O Strobe Subchannel. Enter the desired Subchannel number where the yy is located.
5. Press **[SHIFT] [kHz]**.
   This key sequence sets up an I/O write and will allow data to be written to the device being accessed.
6. Press **[0] [Hz]**.
7. Connect the DVM to the output of the DAC and note the voltage reading. The measured voltage is the offset voltage associated with the DAC. (For current output DACs, voltage measurements must be made at the output of the following current to voltage stage.)
8. Enter the decimal value for the least significant data bit of the DAC (see Table 8A-5a) and press **[Hz]**.
9. Verify that the DVM reading changes (note that the change for the least significant data bit may be very small).
10. Repeat steps 8 and 9 for each of the data bits to the DAC.

3 TO 8 DECODER VERIFICATION

The 3 to 8 Decoders which may be tested using the following procedure are those which use 3 data bus lines to determine which one of eight output lines is set. These do not include the decoders which use the address bus to generate I/O Strobes. An example of a 3 to 8 Decoder which may be tested using the following procedure is A58U31 (see Block **E**, A58 Sweep Generator Assembly schematic). Using A58U34 as an example, the procedure for verifying the operation of a 3 to 8 Decoder is as follows:

1. Verify the operation of the device's I/O Strobe as described in the strobe verification procedure.
2. Press **[INSTR PRESET] [MANUAL]**.
3. Press **[SHIFT] [GHz]** xx **[Hz]**.
   This key sequence sets up the I/O Strobe Channel. Enter the desired Channel number where the xx is located.
4. Press **[SHIFT] [MHz]** yy **[Hz]**.
   This key sequence sets up the I/O Strobe Subchannel. Enter the desired Subchannel number where the yy is located.
5. Press **[SHIFT] [kHz]** to set up an I/O Write.
6. Verify the operation of the decoder by setting one output line at a time and verifying that the correct line is set and the other output lines are not. Since A58U34 is an inverting 3 to 8 Decoder, entering a **[0] [Hz]** from the front panel will set the output pin labeled 0 (pin 15) low (<0.3V) and the other output pins will remain high (>3V). To set the output labeled 1 (pin 14), press **[4] [0] [9] [6] [Hz]** (decimal value of data bit 12, see Table 8A-5a). To set the output pin labeled 7 (pin 7), press **[2] [8] [6] [7] [2] [Hz]** (sum of decimal values of set data bits 12, 13, and 14). The other five output lines are set in a similar manner.

INPUT LATCH VERIFICATION

The input latches are devices which receive information and place it on the data bus for use by the main instrument processor (eg. A59U18). Known data is placed on the input to one of these latches using jumper wires and an I/O Read is performed to verify that the latch is operating. The procedure is as follows:

1. Verify the operation of the input latch's I/O Strobe as described in the strobe verification procedure.
2. Switch the HP 8340A to STANDBY.

3. Using the jumper wires, connect +5V and ground alternately to the input pins of the latch being tested.
4. Verify that the connections were made accurately.
5. Switch the HP 8340A on.
6. Press **[INSTR PRESET] [MANUAL]**.
7. Press **[SHIFT] [GHz]** xx **[Hz]**.
   This key sequence sets up the I/O Strobe Channel. Enter the desired Channel number where the xx is located.
8. Press **[SHIFT] [MHz]** yy **[Hz]**.
9. Press **[SHIFT] [Hz]**.
   This key sequence generates an I/O Read and causes the data on the input of the latch to be displayed in the ENTRY DISPLAY.
10. The first number in the ENTRY DISPLAY is the octal equivalent of the data on the Data Bus. The second number is the decimal equivalent. Using the octal number, verify that the latch is operating correctly (see Example below).
11. Switch the HP 8340A to STANDBY. Reverse the +5V and ground connections on the input to the device being tested.
12. Repeat steps 4 through 10.

Input Latch Verification Example

Assuming that A59U18 is the device to be tested (refer to A59 Digital Interface Schematic), the inputs to the latch would be tied to +5V and ground alternately. The connections would be made as follows:

Input Pin	8	13	2	11	6	15	17	4
Voltage	+5	0	+5	0	+5	0	+5	0
Binary Value	1	0	1	0	1	0	1	0

When an I/O Read is initiated, the data on the input of A59U18 is transferred to the processor via the data bus (bits 8 through 15). The processor also reads bits 0 through 7 and displays the octal and decimal equivalents of all 16 bits in the ENTRY DISPLAY. To determine if A59U18 passed the data correctly, the following table would be constructed.

Bit Number	15	14 13 12	11 10 9	8 7 6	5 4 3	2 1 0
Binary Value	1	0 1 0	1 0 1	0 x x	x x x	x x x

Since A59U18 only sets data bits 8 through 15, bits 0 through 7 are "don't care" terms and are labeled with an x. Bits 8 through 15 are labeled with the binary value that should be set. The binary number above is not converted to an octal number and compared with the ocatal number in the ENTRY DISPLAY. The octal numbers that can be constructed are as follows:

1250xx
1251xx
1252xx
1253xx

Going from left to right, the first three octal digits are determined by bit numbers 9 through 15. The fourth octal digit is determined by bits 6 through 8 and since bits 6 and 7 are "don't care" terms, the fourth digit can range from 0 through 3. The last two octal digits are labeled as "don't care" terms because bits 0 through 5 are "don't care" terms. If one of the above octal numbers did not match the octal number in the ENTRY DISPLAY, then A59U18 would be defective.

If A59U18 passed the above test, the +5V and ground connections to the inputs of A59U18 would be reversed. The connections would be as follows:

Input Pin	8	13	2	11	6	15	17	4
Voltage	0	+5	0	+5	0	+5	0	+5
Binary Value	0	1	0	1	0	1	0	1

The following table would be constructed:

Bit Number	15	14 13 12	11 10 9	8 7 6	5 4 3	2 1 0
Binary Value	0	1 0 1	0 1 0	1 x x	x x x	x x x

The binary number above is converted to an octal number. The possible octal numbers are as follows:

0524xx
0525xx
0526xx
0527xx

If one of the above octal numbers did not match the octal number in the ENTRY DISPLAY, then A59U18 would be defective. If both the previous test and this one passed, then the operation of A59U18 would be verified.

FRONT PANEL DIAGNOSTIC FUNCTIONS

The HP 8340A has several self-checking diagnostic routines that can be activated by pressing keys on the front panel. These diagnostics are summaryized in the following text.

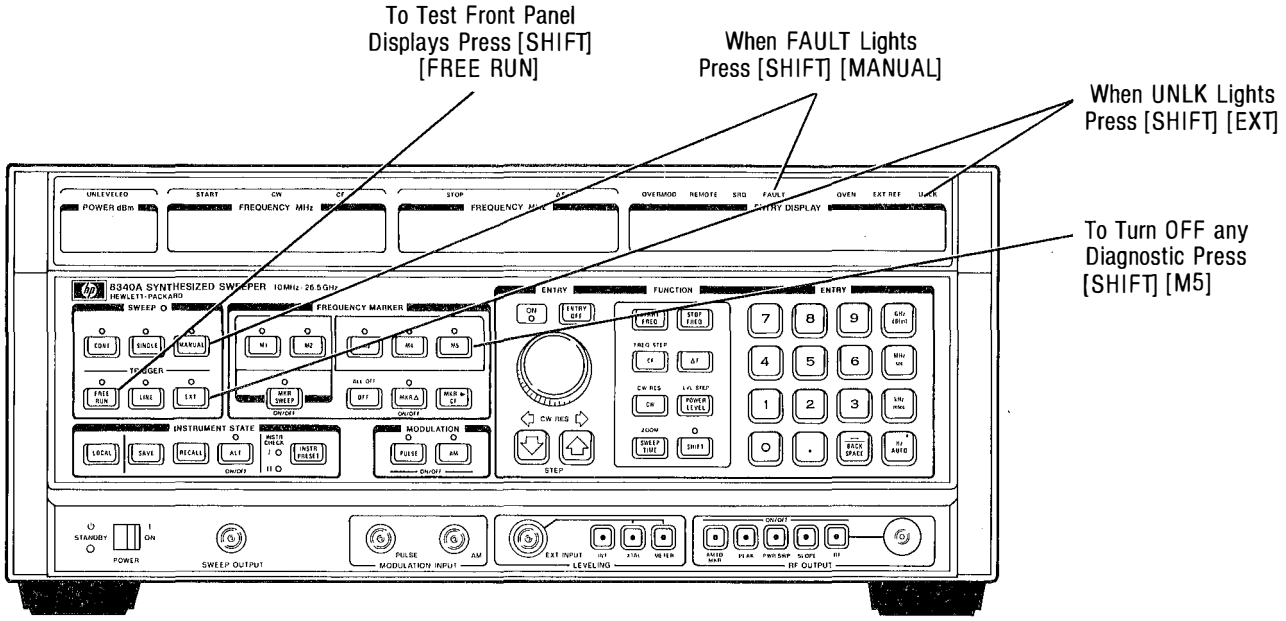


Figure 8A-5. Front Panel Diagnostics

[SHIFT] [MANUAL] (HP-IB: SHS3) activates the FAULT diagnostic routine. When the amber FAULT annunciator appears in the ENTRY DISPLAY, press **[SHIFT] [MANUAL]** to initiate the FAULT diagnostic, which will cause "FAULT: CAL KICK ADC PEAK TRK" to appear in the ENTRY DISPLAY. the flashing cursor indicates which circuit (**CAL**ibration constants, **KICK** sweep end-points, **A**nalog to **D**igital **C**onverter, power **PEAK**ing, or **TR**ac**K**ing) is causing the problem. Refer to Figure 8A-5, "Front Panel Diagnostics."

[SHIFT] [FREE RUN] (HP-IB SHT1) activates the display self-test diagnostic function. Press **[SHIFT] [FREE RUN]**, which will cause every segment of every LED in the displays to light, followed by a marching pattern of every character in the display. Press **[SHIFT] [M5]** to cancel this diagnostic routine and to restore the displays to their previous condition.

[SHIFT] [EXT] (HP-IB: SHT3) activates the oscillator diagnostic function. When the red UNLK annunciator appears in the ENTRY DISPLAY, press **[SHIFT] [EXT]**, which will cause "OSC: REF M/N HET YO N2 N1" to appear in the ENTRY DISPLAY. The flashing cursor indicates which oscillator circuit is causing the unlocked condition. Press **[SHIFT] [M5]** to cancel this diagnostic function and to return the displays to their previous condition.

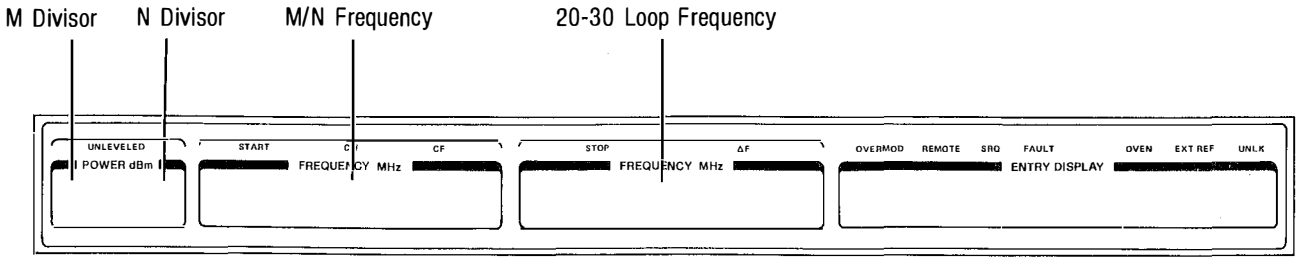


Figure 8A-6. M/N Diagnostics

[SHIFT] [M1] (HP-IB: SHM1) is a service diagnostic that shows from left to right, what the M divisor, N divisor, M/N frequency, and 20/30 loop frequency should be. See Figure 8A-6, "M/N Diagnostics."

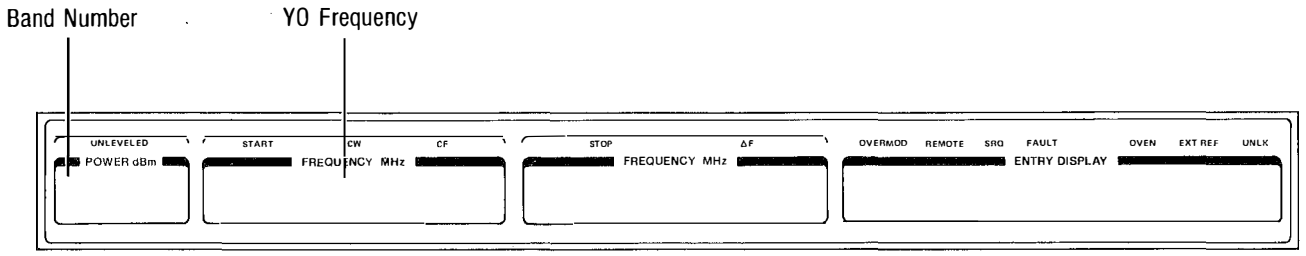


Figure 8A-7. YO Diagnostics

[SHIFT] [M2] (HP-IB: SHM2) is a service diagnostic that shows, from left to right, what the band number and the YIG oscillator (YO) frequency should be. See Figure 8A-7, "YO Diagnostics."

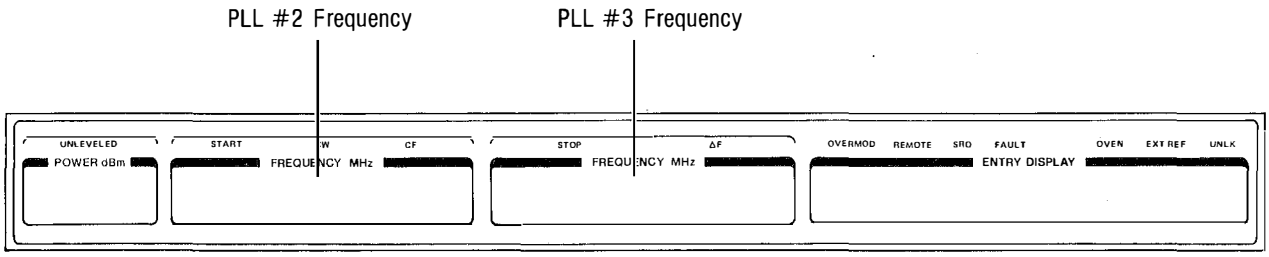


Figure 8A-8. 20-30 Loop Diagnostics

[SHIFT] [M3] (HP-IB: SHM3) is a service diagnostic that shows, from left to right, what the PLL #2 VCO frequency and the PLL #3 upconverter frequency should be. Refer to Figure 8A-8, "20-30 Loop Diagnostics."

[SHIFT] [M4] (HP-IB: SHM4) activates 32 service diagnostic routines which test several of the DACs and control circuitry on the A27 level control, A28 SYTM driver, A57 marker bandcross, and A58 sweep generator. This diagnostic also allows the results of the self-test, run at power on and after on **[INSTR PRESET]**, to be displayed in the front panel **ENTRY DISPLAY**. For more information, refer to the A60 Processor assembly troubleshooting in the Controller Section.

[SHIFT] [M5] (HP-IB: SHM5) turns off any of the above diagnostic routines and restores the displays to their previous condition.

[SHIFT] [XTAL] (HP-IB: SHA2) activates a band crossing diagnostic function. Press **[SHIFT] [XTAL]** to enable the diagnostic, then press **[SHIFT] [INT]**, which will cause the HP 8340A to sweep to the first band crossing point and stop at that point. Press **[SHIFT] [INT]** again and the HP 8340A will sweep to the next band crossing point and stop at that point. Continue pressing **[SHIFT] [INT]** to single-step through each of the bands. Press **[SHIFT] [XTAL]** again to cancel this diagnostic routine.

[SHIFT] [INT] (HP-IB: SHA1) allows single-stepping through each frequency band, and is used with **[SHIFT] [XTAL]** for a band crossing diagnostic routine. See **[SHIFT] [XTAL]** for an explanation of how these two shifted functions interact.

[SHIFT] [RF] (HP-IB: SHRF) disables the ALC (automatic leveling control) to allow direct control of the linear modulator circuit. This is useful when very narrow pulses are being

generated in pulse modulation mode. When **[SHIFT] [RF]** is engaged, there is no limit on the minimum pulse repetition frequency.

The following message will be displayed in the **ENTRY DISPLAY: "POWER SEARCH: X.XX dB"** (where X.XX is the last-entered value).

To set the power level, place the HP 8340A in CW mode, or in pulse modulation mode with pulses wider than 2 usec, and use the **[STEP]** keys, the RPG, or the data entry keypad with the **[dBm]** terminator key to enter the power level desired. The **POWER dBm** display shows the actual power when the instrument is in CW of pulse modulation mode. The accuracy of the **POWER dBm** display is typically the same as when the instrument is leveled. Table 1-1 contains this information under **PULSE MODULATION** specifications, **ACCURACY OF INTERNALLY LEVELED RF PULSE Vp (relative to CW mode level)**. The actual power changes very little as the pulse width is narrowed, even though the **POWER dBm** reading drops. Therefore, at very narrow pulse widths ignore this reading.

[SHIFT] [RF] can also be used as a diagnostic function of the ALC circuits (refer to the ALC loop description/troubleshooting in the beginning of the RF Section for more information).

[SHIFT] [METER] (HP-IB: SHA3) bypasses the ALC (automatic leveling control) to allow direct control of the linear modulator circuit, which is useful when very narrow pulses are being generated in pulse modulation mode. In this mode there is no limit on the minimum pulse repetition frequency: Press **[SHIFT] [METER]**, which will cause "ATN: X-xx dB, MOD: x.x dB" (where x is the last-entered value) to appear in the ENTRY DISPLAY. To set the power, place the HP 8340A in CW mode, or in pulse modulation mode with pulses wider than 2 μsec, and use the **[STEP]** keys to set the ATN (attenuator), and the rotary **[KNOB]** or numerical keys with **[dB(m)]** terminator key to set the MOD (linear modulator), as follows: Set MOD entry at 0 dB, increment ATN until the POWER dBm follows: Set MOD entry at 0 dB, increment ATN until the POWER dBm display shows a level 5 dB to 15 dB higher than the desired output power, then reduce the power to the desired level by changing the MOD value. The POWER dBm display shows actual power when the HP 8340A is in CW or wide-pulse pulses modulation modes; this actual power changes very little as the pulse width is narrowed, even though the POWER dBm reading drops. Therefore, at this point reduce the pulse width to the desired value and ignore the POWER dBm display. The ATN and MOD values in the ENTRY DISPLAY also have a limitation: Although the ATN displayed value is always accurate, the MOD becomes saturated in the top 10 dB (approximately) of its range at which point no change occurs in the true power; consequently, rely on the POWER dBm display for the true power level instead of the MOD value. **[SHIFT] [METER]** can also be used as a diagnostic function of the ALC circuits.

[SHIFT] [PEAK] (HP-IB: SHRP) is a more extensive version of peaking: **[PEAK]**, which requires a fraction of a second to implement, aligns the output filter with a single CW frequency, while **[SHIFT] [PEAK]** aligns all of the YTM tracking calibration constants and requires 5-10 seconds to implement. Use **[SHIFT] [PEAK]** to enhance the power output and spectral purity of swept modes, and to improve tracking performance (especially in harsh environments having wide temperature variations). Press **[SHIFT] [PEAK]**, which will cause "AUTO TRACKING" to appear in the ENTRY DISPLAY; "AUTO TRACKING" will disappear after 5-10 seconds when the calibration has been completed.

[SHIFT] [PWR SWEEP] (HP-IB: SHPS) decouples the attenuator (ATN) from the automatic leveling control (ALC), as explained in the preceding function. Recouple the ATN and ALC by pressing **[POWER LEVEL]**.

[SHIFT] [SLOPE] (HP-IB: SHSL) allows front panel control of the mechanical attenuator (ATN). Press **[SHIFT] [SLOPE]**, which will cause "ATN: xdB" (where x is the last-entered value) to appear in the ENTRY DISPLAY. Use the **[STEP]** keys, or the numerical keys with any terminator key to change the attenuator value within the range 0 dB to −90 dB in 10 dB steps. Keyboard entries are automatically rounded to the nearest 10 dB. The clicking sound heard after each attenuator change is the attenuator pad being mechanically switched into the RF output path.

OVERALL INSTRUMENT TROUBLESHOOTING

INTRODUCTION

This section contains information that is critical to the timely repair of the HP 8340A. when a failure occurs on the HP 8340A, it is important to first verify that the Calibration Constants in memory are good. Refer to the first page of this Service Introduction for details.

The troubleshooting information presented here is intended to guide the troubleshooter to the appropriate information in the manual.

Figure 8A-9, Overall Instrument Troubleshooting Diagram, and Figure 8A-10, Front and rear panel Items, indicate the proper sequence to follow to isolate specific symptoms. Each of these is described in detail in the following pages. Several categories make reference to Front and rear panel items shown in the diagram on the facing page.

The descriptions in the following pages are keyed to the numbers in the diagrams.

OVERALL INSTRUMENT TROUBLESHOOTING

THE FOLLOWING DIAGRAM INDICATES THE PROPER SEQUENCE TO FOLLOW TO ISOLATE SPECIFIC SYMPTOMS. EACH OF THESE IS DESCRIBED IN DETAIL IN THE FOLLOWING PAGES. SEVERAL CATAGORIES MAKE REFERENCES TO THE FRONT AND REAR PANEL ITEMS SHOWN IN FIGURE 8A-10 ON THE FACING PAGE

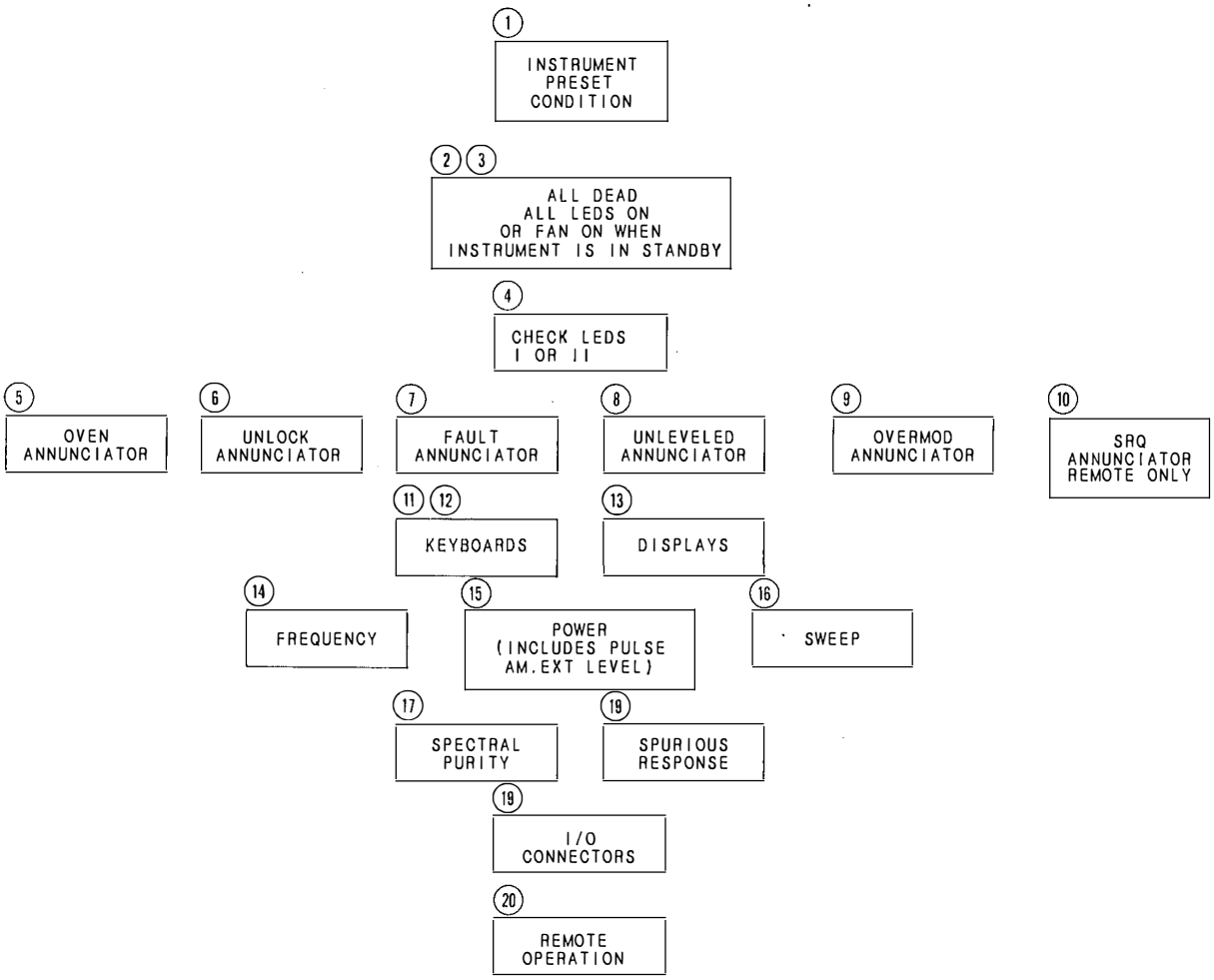
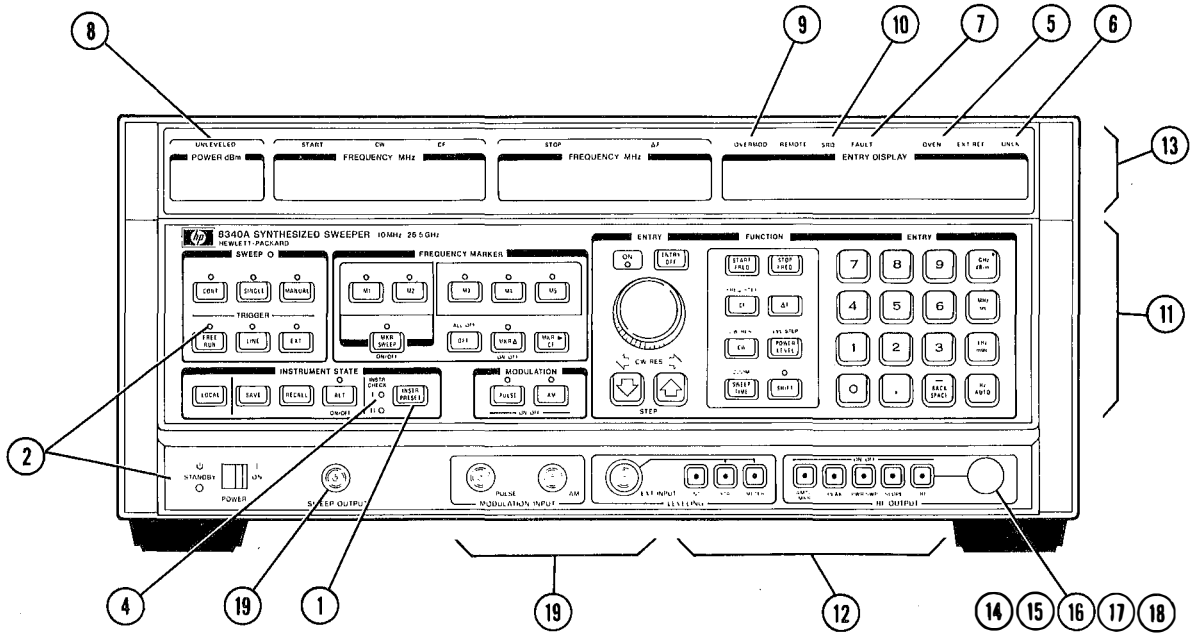


Figure 8A-9. Overall Instrument Troubleshooting Diagram

FRONT PANEL



REAR PANEL

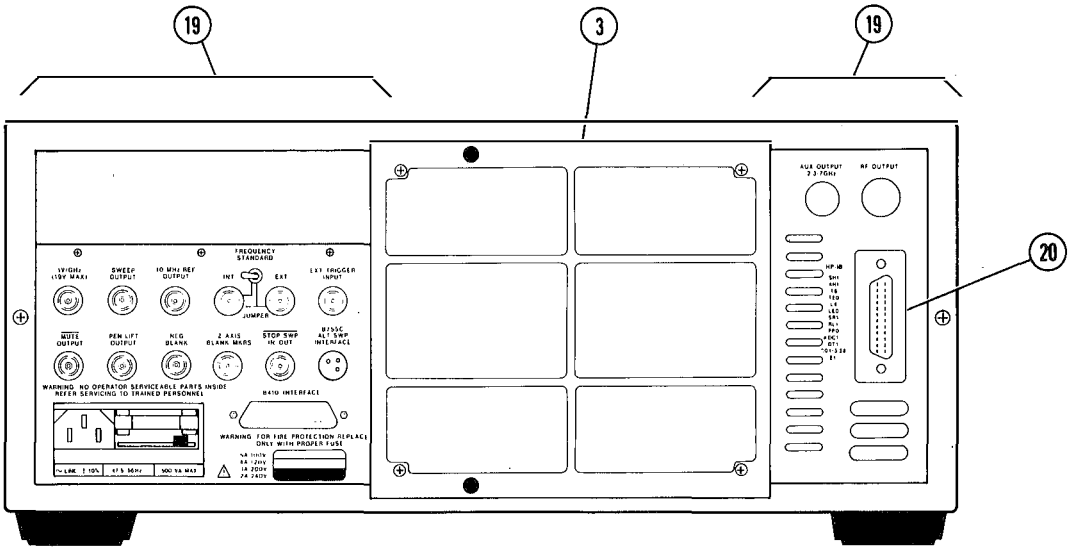


Figure 8A-10. Front and Rear Panel Items

1. **INSTRUMENT PRESET CONDITIONS [INSTR PRESET]**

After pressing **[INSTR PRESET]** the following HP 8340A settings should exist:

"POWER dBm" Display= 0.0 (Factory setting, determined by Cal Constant #56)

"FREQUENCY MHz" Display= 10.000000
"START" annunciator LED lit

"FREQUENCY MHz" Display= 26 500.000000
"STOP" annunciator LED lit

"ENTRY" Display= Blank (off)

"SWEEP" Block= Green LED flashing
"CONT" LED on
"FREE RUN" LED on

"FREQUENCY MARKER" Block= All LED's off

"INSTRUMENT STATE" Block= All LED's off

"MODULATION" Block= All LED's off

"ENTRY" Block= All LED's off

"LEVELING" Block= "INT" LED on

"RF OUTPUT" Block= "RF" LED on

After an **[INSTR PRESET]** the RF output should be a swept 10 MHz to 26.5 GHz signal leveled at 0 dBm.

EXCEPTIONS TO THE ABOVE CONDITIONS

a. If the rear panel INT/EXT REFERENCE switch is in the EXT position, then the EXT REF annunciator on the ENTRY DISPLAY will be on.

b. By changing calibration constant #56 on the HP 8340A can be set to come up with various output power levels after an **[INSTR PRESET]**. Refer to Calibration Constants in Section VIII for more detailed information.

2. **ALL DEAD**

ALL LED's OFF. If, after **[INSTR PRESET]**, all of the LED's and annunciators are off, suspect a power supply problem. Refer to the Power Supply Theory of Operation and Troubleshooting.

If some of the LED's that should be on are on and somethat should be on are off, suspect a problem in the HP 8340A front panel. Refer to the front panel Theory of Operation and Troubleshooting.

ALL LED's ON. If, after **[INSTR PRESET]**, all of the LED's and annunciators are on, suspect a problem in the instrument processor or memory (Self-Test not running). Refer to Processor Theory of Operation and Troubleshooting, in the Controller functional group.

CHARACTER MARCH. If, after an **[INSTR PRESET]**, there is a string of characters marching across the four display windows, suspect a processor or memory problem.

3. **FAN**. The HP 8340A's cooling fan should be off when the instsrument is in STANDBY and on when the POWER switch is in the ON position. If the fan will not turn on or off, refer to the Power Supply Theory of Operation and Troubleshooting.

If the fan is not working when the instrument is on, the temperature inside the HP 8340A could rise to a point that the power supplies will go into over-temperature mode and shut down (See overtemp LED, A52DS4).

4. **CHECK LED I AND II.**

The two front panel INSTR CHECK LED's are used to indicate the results of the instrument Self-Test. A Self-Test is initiated every time the POWER switch is cycled ON or **[INSTR PRESET]** is pressed. The Self-Test starts by turning both check LED's on.

CHECK LED I will be turned off when it is determined that all ROM and RAM are good and that the microprocessor is working.

CHECK LED II will be turned off when it is determined that the internal I/O Address Bus and all 16 bits of the I/O Data Bus are good.

If either one or both of the check LED's remain on, the problem is most likely on the A60 Processor board. Refer to Processor Theory of Operation and Troubleshooting, in the Controller functional group.

It is possible to have a fault in the instrument that could cause the check LED's to go out when they should stay on. The check LED's can be double checked by examining the LED's on the A60 Processor board. If the two INSTR CHECK LED's go off, all 16 Processor board LED's should be off.

5. **OVEN ANNUNCIATOR**

The front panel OVEN light is used to indicate the status of the internal frequency standard. When the OVEN light is lit, the frequency is more than 100 Hz away from 10 MHz. The A51 10 MHz Reference Oscillator has an internal circuit that monitors the temperature of its internal oven. When this oven temperature is too low the HOVC line is high ($>+15V$). When the oven temperature reaches the desired point (the frequency is within 100 Hz of 10 MHz) HOVC goes low ($\downarrow +15V$). HOVC is sent to the A59 Digital Interface board where the microprocessor reads it and determines when to turn the light on or off.

The OVEN LED is located on the A2 Display Driver board (Block **E**). These LED's are driven by the A3 Display Processor, Annunciator Latch/Driver.

The LED is turned on by the instrument processor. The processor outputs the appropriate bits on the Data Bus and then outputs address 15:R0 to latch the data bits.

6. **UNLK ANNUNCIATOR**

The UNLK light is used to indicate the status of the 6 different internal phase lock loops. If the UNLK light is on, one or more of the loops is unlocked. Press **[SHIFT] [EXT]**. The ENTRY DISPLAY will show the following:

OSC: REF M/N HET YO N2 N1

The name of the loop that is unlocked will be flashing.

REF - If the REF is flashing, refer to the Reference Loop Theory of Operation and Troubleshooting in the Reference Loop - M/N Loop functional group.

M/N - If the M/N is flashing, refer to the M/N Theory of Operation and Troubleshooting in the Reference Loop - M/N Loop Functional group.

HET - If the HET is flashing, refer to the RF Section (A8 3.7 GHz Oscillator) Theory of Operation and Troubleshooting.

YO - If the YO is flashing, refer to the YO Loop Theory of Operation and Troubleshooting in the Sweep Generator - YO Loop functional group.

N1 - If the N1 if flashing, refer to the 20/30 Loop (PLL1) Theory of Operation and Troubleshooting.

N2 - If the N2 is flashing, refer to 20/30 Loop (PLL2) Theory of Operation and Troubleshooting.

MULTIPLE LOOPS UNLOCKED

If more than one loop is unlocked at one time it is important to understand how the loops relate to each other. The REF loop generates reference signals that are required by all other loops. The YO loop uses signals generated by the M/N loop and the 20/30 loop.

The UNLK LED is located on the A2 Display Driver board (Block **E**). These LED's are driven by the A3 Display Processor, Annunciator Latch/Driver.

The LED is turned on by the instrument processor. The processor detects the unlock indication from the particular phase lock loop and outputs the appropriate bits on the Data Bus and then outputs address 15:R0 to latch the data bits.

7. **FAULT ANNUNCIATOR**

The FAULT light is used to monitor the status of 5 different internal functions. These functions are described below. If the FAULT light is on, press **[SHIFT] [MANUAL]**. The ENTRY DISPLAY will show the following.

FAULT: CAL KICK ADC PEAK TRK

The name of the function that has a problem will be flashing.

CAL - This refers to the Calibration Constants stored in RAM on the A60 Processor board. The Calibration Constants are checked only when an **[INSTR PRESET]** is done or at instrument power on. If the CAL light is flashing something has changed in the Cal Constants. Refer to Calibration Constants in Section VIII Introduction for more information. If any operation is performed that updates a Cal Constant, the processor will calculate a new checksum. After the next **[INSTR PRESET]** or power on, the FAULT light will be out, but the bad calibration constant(s) will still be there.

KICK - This refers to the kick pulses used to reset the YO and SYTM. AT end-of-sweep the YO and SYTM are tuned below their normal start frequencies by a kick pulse generated on the A54 YO Pretune DAC/Delay Compensation board or the A28 SYTM Driver board. These kick pulses last a finite period of time. If a pulses stays on longer than it should, the processor will detect it and indicate a KICK FAULT. Refer to the Sweep Generator - YO Loop Theory of Operation and Troubleshooting for the A54 Pretune and to the RF Section for the A28 SYTM Driver.

ADC - This refers to a check performed on the ADC circuits. This check is done at **[INSTR PRESET]** or power on. If the ADC light is flashing, refer to the RF Section (A27 Level Control board) Theory of Operation and Troubleshooting.

PEAK - This refers to an HP 8340A function that peaks the RF output power at one frequency by fine tuning the SYTM (Tunes the SYTM to the YO frequency). This fault can only come on if the **[PEAK]** button is pushed. If the PEAK light is flashing, something is wrong with the circuitry that peaks the SYTM. Refer to the RF Section (A28 SYTM Driver board or A27 Level Control board) Theory of Operation and Troubleshooting.

TRK - This refers to an HP 8340A function that peaks the RF output power while the instrument is sweeping. This fault can only occur if **[SHIFT] [PEAK]** has been pushed. The TRK light indicates the same things as if PEAK were flashing.

The FAULT LED is located on the A2 Display Driver board (Block **E**). These LED's are driven by the A3 Display Processor, Annunciator Latch/Driver.

The LED is turned on by the instrument processor. The processor detects the error from the particular circuitry and outputs the appropriate bits on the Data Bus and then outputs address 15:R0 to latch the data bits.

8. **UNLEVELED ANNUNCIATOR**

The UNLEVELED light is used to indicate the status of the RF output power. If the UNLEVELED light is off, the output power is leveled and if the light is on, the power is unleveled.

a. Make sure that the correct leveling mode is selected. If internal leveling is desired, the INT light should be on. If external leveling is desired, the XTAL light should be on. If power meter leveling is desired, the METER light should be on.

b. The power level requested should not be greater than the maximum power specification. If the instrument is sweeping, make sure that the power requested does not exceed the maximum power specification for the entire band or bands that are being swept.

c. If the output power is unleveled at all power levels and all frequencies, suspect a problem on the A25 ALC Detector board or the A26 Linear Modulator board. Refer to the RF Section Theory of Operation and Troubleshooting.

d. If the power will level at some frequencies and not others while the instrument is sweeping, the SYTM may not be tracking correctly. Try AUTO TRACKING. Press **[SHIFT] [PEAK]**.

e. If the power will level at some CW frequencies and not at others, press **[PEAK]** to optimize the SYTM tracking at the frequency of interest.

f. If the power is unleveled in Band 0 (10 MHz to 2.4 GHz) only, suspect a problem in the switching circuits on the A25 ALC Detector board or the A26 Linear Modulator board, the A12 Band 0 Splitter/Detector or the associated microcircuits. Refer to the RF Section Theory of Operation and Troubleshooting.

g. If the power is unleveled in Bands 1-4 (2.3 GHz to 26.5 GHz) only, suspect a problem in the switching circuits on the A25 ALC Detector board or A26 Linear Modulator board, or the A11 Band 1-4 Detector and the associated microcircuits. Refer to the RF Section Theory of Operation and Troubleshooting.

NOTE

Refer to the ALC Loop Overview in volume I, Section III, and the ALC description in the RF Section for more detailed information on troubleshooting unleveled power.

9. **OVERMOD ANNUNCIATOR**

The OVERMOD light is turned on by the instrument processor only when AM is selected and when MOD LVL (See A26 Linear Modulator, Overmodulation/Unleveled Detectors) exceeds a given limit. Refer to the RF Section Theory of Operation and Troubleshooting.

The OVERMOD LED is located on the A2 Display Driver board (Block **E**). These LED's are driven by the A3 Display Processor, Annunciator Latch/Driver.

The LED is turned on by the instrument processor. The processor outputs the appropriate bits on the Data Bus and then outputs address 15:R3 to latch the data bits.

10. **SRQ ANNUNCIATOR**

The SRQ (Service ReQuest) light should be on only during remote operation and when the instrument processor sets SRQ (to the processor) true.

Refer to Section IV, HP-IB Operation and Verification Program to read the HP 8340A Status Bytes.

Also, refer to the A60 Processor, HP-IB Interface Troubleshooting in the Controller functional group.

The SRQ LED is located on the A2 Display Driver board (Block **E**). These LED's are driven by the A3 Display Processor, Annunciator Latch/Driver.

The LED is turned on by the instrument processor. The processor outputs the appropriate bits on the Data Bus and then outputs address 15:R3 to latch the data bits.

11. **UPPER KEYBOARD**

12. **LOWER KEYBOARDS**

Refer to front panel Theory of Operation and Troubleshooting.

13. **DISPLAYS**

Refer to front panel Theory of Operation and Troubleshooting.

14. **FREQUENCY**

If the UNLK annunciator is not on and the frequency of the RF output signal is incorrect, refer to Section IV Performance Test, Frequency Range and CW Mode Accuracy. This test checks all of the divider bits that program the various phase lock loops. The test will indicate which phase lock loop is causing the problem and which bit(s) is incorrect. Then refer to the Theory of Operation and Troubleshooting for the appropriate phase lock loop.

15. **POWER**

The RF output should meet the specifications for maximum leveled power, power accuracy, and flatness.

For problems related to maximum leveled power, refer to UNLEVELED ANNUNCIATOR (number 8).

For problems related to flatness, consider the following:

The flatness adjustments in Section V improve overall flatness by varying the offset and slope correction factors. If the frequency response has large perturbations, the problem is most likely in the associated RF path. Refer to the RF Section block diagram. By observing if the problem is in Band 0 only, Band 1-4 only, or both Band 0 and Band 1-4, part of the RF circuitry may be eliminated.

If the RF power level is low at 10 MHz and increases with frequency, suspect the RF output connector. This connector contains a series capacitor that could exhibit this symptom. To verify that the problem is the RF connector, first remove the front panel - rear panel functional group, Figure 8H-4. Then, disconnect the SMA cable from the RF connector, and remove the RF connector. Measure the power level at the cable.

CAUTION

Extreme care should be taken when disconnecting or connecting the SMA cables from a mating 3.5 mm connector (RF Attenuator). The SMA cable center conductor must align with the 3.5 mm connector center conductor. If there is any axial force on the cable when disconnecting the SMA fitting, the 3.5 mm connector center conductor may be damaged. Remove any axial force on the cable by disconnecting the end of the cable that does not mate with a 3.5 mm connector first or by removing the mounting screws of the device having 3.5 mm connectors (A10 Direction Coupler).

For problems related to accuracy, consider the following:

NOTE

Option 001 and 005 instruments are not equipped with a step attenuator.

Flatness is adjusted and tested with the RF output power at 0 dBm (RF Attenuator at 0 dB and ALC at 0 dBm). The frequency response will normally remain the same over the ALC range. For accuracy problems within the ALC range, refer to the ALC adjustments in Section V and, if necessary, to the RF Section ALC Loop Theory of Operation and Troubleshooting.

If accuracy is within specifications over the ALC range and is out of specifications below the ALC range, the problem is most likely associated with the RF attenuator. Note that the RF attenuator is outside of the ALC Loop. The instrument processor programs the RF attenuator, but there is no way for the processor to know if the attenuator actually stepped properly. If the power level is off by a factor of 10 dB, the attenuator may not be responding properly. Select a CW frequency, set the power level to 0 dBm, press **[SHIFT] [PWR SWP]**. The Entry Display should indicate:

ATN: −00 dB, ALC: 0.00 dBm

Using the step keys step the RF attenuator (and RF power output) to −90 dB. The attenuator should "click" at each step and the RF power should decrease in 10 dB steps. If the attenuator does not perform properly, refer to the RF Section overall block diagram. Determine if the correct programming bits are being applied to the RF attenuator (See RF Attenuator truth table on the A24 Attenuator Driver/SRD Bias assembly, schematic diagram, located in the RF Section) or if the RF attenuator itself is not responding properly.

There is an offset and slope calibration constant correction factor for each RF attenuator step from 10 to 90 dB. These correction values are generated in the automated RF Attenuator Calibration Test program. A hard copy of values generated at the last calibration should be located inside the instrument (Remove the top cover - see pocket along left side rail). Check the calibration constants in HP 8340A memory against the hardcopy values. Restore the correct values if necessary. Refer to Section VIII Calibration Constants for more information.

If the attenuator is operating properly and the calibration constants are correct, check the RF connections from the A10 Directional Coupler to the RF attenuator and then measure the power accuracy at the attenuator output.

16. **SWEEP**

For sweep problems, refer to the Sweep Generator - YO Loop functional group, Sweep Generator Troubleshooting. The following information may be used to further define the symptom.

It is assumed that the instrument works properly in CW mode (no UNLK indication). Press **[INSTR PRESET]** and check for the following sweep indications:

1. Check front panel SWEEP LED. The LED should be blinking.

   The sweep LED is turned on at the start of sweep, turned off at each bandcross, and at end-of-sweep. The LED is controlled by LSPLD (Low Sweep LeD), see A58 Sweep Generator board Block P. The sweep LED is turned on when HSP (High Start Sweep) from A57 Block **M** is high, LRSP (Low Reset Sweep) from A59 Block **G** is low, and LBX (Low Bandcross) A58 Block **U** and A57 Block **F** is high.

   The sweep LED is turned off if HSP is low, at end-of-sweep if LRSP is low, and at bandcrossings if LBX is low.

2. Check front and/or rear panel SWEEP OUT signal.

   The SWEEP OUTPUTS come from the A57 Marker/Bandcross board Block **H** and are generated from the MKR RMP A58 Block **K**. For a detailed description of the SWEEP GENERATOR/YO LOOP Theory Of Operation under Multiband Sweeps.

   If the sweep out waveform is normal, the Ramp Generator on the A58 board is working, the WSPTM (Write Sweep TiMe) strobe (A59 Block **A**) is being generated, and LRESET (Low Reset) A58 Block **P** is OK.

3. Check rear panel 1V/GHz waveform.

   The 1V/GHz signal comes from the A28 SYTM DRIVER board Block **F** and is generated by the PRETUNE signal (A54 Block **C** TP3). The PRETUNE signal is generated from VSWP (A58 Block **N**).

   If the rear panel 1V/GHz signal is normal, VSWP and PRETUNE are OK.

NOTE

For sweep widths <500 kHz (20/30 sweeps), the 1V/GHz is fixed.

17. **SPECTRAL PURITY**

18. **SPURIOUS RESPONSES**

Normally spurious responses fall under the general category of spectral purity. However, in this instance we will consider spectral purity to be a phase noise problem and spurious responses to be discrete.

Phase Noise

It is assumed that the HP 8340A failed the Single Sideband Phase Noise test, Section IV, paragraph 4-17.

1. If the HP 8340A failed the test at offset frequencies less than 300 Hz, the problem is most likely the 100 MHz Reference section. Refer to the Reference Loop - M/N Loop. Replace the 400 MHz input to A31 M/N Phase Detector (J1) using a very stable source such as an HP 8662A. Be sure to use the 8662A Frequency Standard as the HP 8340A Frequency Standard EXT input. Repeat the failing test. If the HP 8340A now passes the test, the problem is in the HP 8340A Reference Loop.
2. If the HP 8340A failed the phase noise test at offset frequencies from 300 Hz to 50 kHz, the problem is most likely the M/N Loop. Replace the Reference Loop 400 MHz input to the M/N Loop as described in step 1 above.

   If the HP 8340A continues to fail the phase noise test, the problem is in the M/N or YO Loop. An external source could be used to replace the M/N input to the YO Loop, but the phase noise of the external source would have to be much better than the HP 8340A phase noise to eliminate the YO Loop.
3. If the HP 8340A failed the phase noise test at offset frequencies greater than 50 kHz, the problem is most likely the YO Loop.

Spurious Responses

It is assumed that the HP 8340A failed the Spurious Response test, Section IV, paragraph 4-15 or 4-16.

Spurious responses can be divided into several categories:

Harmonics/Sub-harmonics

Line Related Side Bands

Squegging

Synthesized

HARMONICS/SUB-HARMONICS

The HP 8340A is essentially three instruments in one. The instrument can function as a heterodyning (Band 0) source, an unmodified YIG oscillator source (Band 1), and a synthesized source (Bands 2-4). In Band 0 (10 MHz to 2.3 GHz) the 2.3 to 7.0 GHz YO output is mixed with a fixed 3.7 GHz oscillator to produce the RF frequency. In Band 1-4 the YO output is used directly or multiplied (by the band number) to produce the RF frequency.

In Bands 1-4 the SYTM is designed to pass only the RF output frequency and reject all other frequencies. In Band 0, the output of the Band 0 mixer passes directly through the SYTM.

To troubleshoot for harmonics and sub-harmonics in Band 0 (10 MHz to 2.3 GHz), refer to the RF Block Diagram and troubleshoot the Band 0 circuitry using a spectrum analyzer.

For Bands 1-4 the SYTM is designed to pass only the fundamental or desired harmonic of the YO. If the instrument does not meet its harmonic/sub-harmonic specification, suspect the SYTM.

LINE RELATED SIDEBANDS

Line related spurs are normally caused by magnetic radiation from the power transformer being coupled into the M/N Loop, the Reference Oscillator, or the SYTM.

The amplitude of any line related spur coupled into the M/N Loop will be greater at 6.9 GHz (maximum M/N Loop frequency). The amplitude of any line related spur coupled into the SYTM will be greater at 2.3 GHz (minimum SYTM drive current).

An increase in line voltage or the line voltage selector PC board installed incorrectly may increase the radiation and thus the spur amplitude.

Check the waveform on the unregulated power supplies. These supplies have full-wave bridge rectifiers. If one diode is open, the supply will operate similar to a half-wave rectifier. The output of the regulated supplies may be normal. However, the transformer current will be unbalanced and the magnetic radiation may increase.

Magnetic radiation coupled into the M/N Loop can sometimes be reduced by replacing A29U1 (The amplifier limiter on the Reference Phase Detector board).

SQUEGGING (Band 1-4 only)

Observe the spurious response on a spectrum analyzer while changing the HP 8340A output power level. If the frequency of the spur changes with power level, suspect squegging. Refer to the SRD Bias adjustments in Section V.

SYNTHESIZED SPURS

NOTE

The screws on the 20/30 and M/N section covers must be tight to obtain proper shielding.

Explanation of synthesized spurs - A frequency synthesizer like the HP 8340A has several internal oscillators that are used to generate the desired output frequency. All of the output frequencies that are possible can be described by the following equation:

$$Fout = k1*F1 + k2*F2 + k3*F3 \ldots\ldots\ldots\ldots$$

where k1, k2, and k3 are integers (positive or negative) and F1, F2, and F3 are the frequencies of the internal oscillators. Since F1, F2, and F3 are phase locked to the internal reference (10 MHz standard) they will be related to the reference frequency by:

$$F1 = Ref*I1/J1 \quad F2 = Ref*I2/J2 \quad F3 = Ref*I3/J3$$

where the I's and J's are integers. The combination of all these shows the relationship of the output frequency to the reference frequency:

$$Fout = Ref * (k1*I1/J1 + k2*I2/J2 + k3*I3/J3 \ldots)$$

The intended output frequency is the result of only one set of integers in the above equation. Spurs are possible at all other choices of integers. These choices are normally eliminated through careful use of filtering, attention to signal levels, shielding, etc.

The key is to treat the spurs as FAMILIES of spurs. A spur family is characterized by having the same mixing path through the instrument. For example, if it can be determined that the 5th harmonic of the M/N VCO is mixing with the 9th harmonic of the 20/30 output, then the location of the spur can be predicted as the 20/30 frequency is changed. Also more spurs in this family can be hypothesized such as the 9th 20/30 harmonic with the 6th M/N harmonic. The common thread between all of these is that somehow the M/N VCO is allowed to mix with the 20/30 to cause a spur.

The spurs normally show up as phase modulations of the YO frequency. As the spur frequency is changed (by changing the carrier frequency), its amplitude will remain constant as long as the offset from carrier remains less than the YO Loop bandwidth (50 kHz). Beyond the YO Loop bandwidth, the amplitude decreases until the spur is gone.

These spurs are called CROSSING SPURS, and are possible whenever the harmonic frequencies of any two oscillators are equal (5th harmonic of 20 MHz = 4th harmonic of 25 MHz). A characteristic of crossing spurs is that the offset of the spur from the carrier changes as the carrier is moved; therefore, there is some frequency that the offset must be zero (Assuming the sources of the spurs can be tuned to this frequency). This frequency is called the CROSSING FREQUENCY of the spur. The ratio of the change in spur offset to the change in carrier frequency is called the ORDER.

Names can be assigned to the different spur families such as: type A, B, C1, C2, C3, etc. Each of these have a set of defining conditions to determine the crossing frequencies.

Type B, crossing frequency whenever:

10*Flf/10 = I or Flf = I

where Flf = 20/30 loop output frequency

ORDER of the spur = 10

This type is caused by the 20/30 mixing with the Ith harmonic of 10 MHz in the Reference Phase Detector.

Type C1 and C3 are both due to the 20/30 output and its harmonics mixing with the M/N VCO.

Given:

Fmn = M/N Output freuency = 200 − 10*M/N (MHz)

Flf = 20/30 Output Frequency = 20 to 30 (MHz)

M, N are the divider numbers for the M/N Loop

I, J, K are integers

then the conditions for the two spurs are:

Type C1, crossing frequency whenever:

Fmn/Flf = 20 * (20-M/N)/I

ORDER of spur = I/2

This type can be caused by several factors. Some possibilities are, the A48 Sampler board 70 MHz Low Pass Filter, or the A46 Low Pass Filter Assembly.

Type C3, crossing frequency when:

Fmn/Flm = 20*I ± J/(2*K)

or

F1f = 20 * K * (20-M/N)/20*I ± J

ORDER of spur = 20*I ± J/(2*K)

This type is caused by the Ith harmonic of the PLL1 VCO sampled by the Kth harmonic of the M/N VC0.

For any CW frequency, selecting the appropriate SHIFT functions will display the M/N frequency, 20/30 frequency and YO frequency. A synthesized spurious response must be a function of these signals. As mentioned above, the elimination of these spurs is primarily a design considseration; however, any coupling from one signal path into another may result in a spurious response (i.e., loose connectors, poor shielding, cable routing, etc.).

Band 0 spurs are caused by mixing products in the Band 0 mixer. These are not crossing spurs because they are not YO Loop sidebands. Instead, they are added to the output as part of the down-conversion process. The YO output should mix with the 3.7 GHz oscillator output and produce a single mixer output at Fyo - 3.7 GHz. However, harmonics of both oscillators are present, or are generated in the mixer. These mix to form spurs on the output.

Troubleshooting synthesized spurs - One way to eliminate various RF paths is to determine the YO frequency at which the spur occurs, then select a CW frequency in both Band 0 and Band 1 that uses the YO frequency. If the spur occurs only in Band 0, troubleshoot the Band 0 RF path. If the spur occurs in Band 1, troubleshoot the Band 1-4 RF path.

Change the CW frequency such that the M/N output remains constant and only the 20/30 output changes. Determine the order of the spur (i.e., Ratio of YO frequency change to spur frequency change). If the spur is a crossing spur at some point the spur will be on top of the YO frequency and at some point (50 kHz away from the YO frequency) the spur amplitude will decrease. If the spur is a crossing spur, refer to the appropriate spur family type above.

It may help determine which internal frequency source(s) is generating the spur by:

Change the CW frequency while monitoring the SHIFT function diagnostics, looking for a sudden change in spur frequency and/or amplitude. For example, press **[SHIFT] [M1]** then change the CW frequency. Look for a correlation between any sudden change in spur frequency and/or amplitude with a change in M/N output frequency or 20/30 output frequency. If a sudden change in the spur occurs at the same time the M/N or 20/30 makes a large change, the internal frequency source that changed is probably one of the signals that is generating the spur.

If the 20/30 loop is suspected, press **[SHIFT] [M3]** to display the PLL2 VCO frequency and PLL3 Up Converter frequency and repeat the above test.

NOTE

For more information on the diagnostic modes, refer to the Frequency Range and CW Mode Accuracy test in Section IV.

19. I/O CONNECTORS

To determine source or destination of input or output connector signals, refer to the Front and rear panel section wiring diagrams. For troubleshooting, refer to the source or destination assembly Theory of Operation and Troubleshooting.

20. REMOTE OPERATION

Section IV contains an HP 8340A HP-IB Operation Verification Programming Listing. This program will verify the ability of the HP 8340A to respond to a remote input (complete HP-IB handshake).

The program will test each data bit and read the HP 8340A Status bytes.

If the HP 8340A exhibits a problem while running this test, refer to the A60 Processor Troubleshooting in the Controller functional group.

If a problem is not observed while running this program and the HP 8340A does not respond properly to other remote commands, refer to the computer documentation to read the computer HP-IB I/O card status. By outputting the I/O card status, the source of the problem may be determined.

THIS PAGE SUPERSEDES MANUAL CHANGE SUPPLEMENT PAGE C-171 IN CHANGE 4

REPAIR PROCEDURES

INTRODUCTION

This section contains important information concerning the repair of this instrument. Other important information is contained in the **"POWER SUPPLY - FAN"** and the **"RF SECTION"** portions of the manual concerning the repair of these assemblies.

CAUTION

This section contains procedures in which one must handle assemblies that contain static sensitive components. Handle any printed circuit board by the edges and never touch finger contacts. Service this instrument only at a work station that is equipped with an anti-static surface. Any persons working on this instrument should wear a grounding strap that provides a path to ground of no less than 1 Megohms and no more than 2.5 Megohms. All anti-static safeguards must conform to state and federal safety standards and statutes.

The thermal connection between two of the instrument heat sinks and the components mounted to them is the dominant factor in the component's long term reliability. Be sure to properly apply thermal compound (HP Part Number 6040-0454 CD0) when installing or replacing any of these parts. Refer to the POWER SUPPLY - FAN functional group for thermal compound application procedure.

Use only oil based thermal compound. The use of silicone based thermal compount may cause serious reliability problems. Silicone based oil migrates to pass element sockets, switch contacts, or printed circuit board edge connectors. The compound then tends to raise contact resistance or electrically isolate the contacts. Silicone based thermal compounds disperse into the air and deposit themselves anywhere in the instrument. Applying this material to a warm component (e.g. a heat sink or pass element) increases the rate of dispersion.

Use only Rosin Mildly Activated solder when repairing a PC Board. Rosin Activated solder may cause reliability problems if used.

Never clean solder flux from a PC Board after replacing a component! This may cause serious reliability problems. The solder flux that remains on the PC Board is composed of activator that is completely encapsulated by rosin. When this flux is "cleaned" off, the rosin and the activator separate and are smeared all over the PC Board. They also flow under the edge of PC Board traces (all traces have undercuts along their edges from the etching process). Once under the edge of a trace the material collects moisture. The dissimilar metals that make up the trace react to the clorides in the activator and begin to migrate, disolving the trace. The activator will also create an electrical path from one trace to another. This allows metal migration between the two traces. As

THIS PAGE SUPERSEDES MANUAL CHANGE SUPPLEMENT PAGE C-172, IN CHANGE 4

more metal migrates the impedance between the traces decreases, allowing metal to migrate faster. This process continues until a short develops. The later process is known as dendrite growth. Dendrites form a fern-like pattern of metal growth that is visible between the traces.

Use only solder stations equipped with a grounded tip as well as low static de-soldering aids. When removing a motherboard connector it is recommended that in order to avoid the unnecessary cost and down time causesd by damaged motherboard pads, a specialized solder removal tool should be used. The Ungar HOT VAC or equivalent device is recommended. Figure 8A-2 lists recommended soldering equipment and supplies.

Cleaning P.C. Board fingers by any other method than the one described below may cause serious reliability problems. NEVER clean fingers with any kind of eraser. NEVER use tap water in the cleaning solution described below. Tap water contains chlorine. Chloride contamination from tap water, salt (from skin contact), or any other source may cause serious reliability problems (dendrite growth, trace damage, see the preceding warning). Always wear a ground strap when handling any internal HP 8340A component or assembly. Always hold printed circuit boards by the edges.

PRINTED CIRCUIT BOARD FINGER CLEANING PROCEDURE

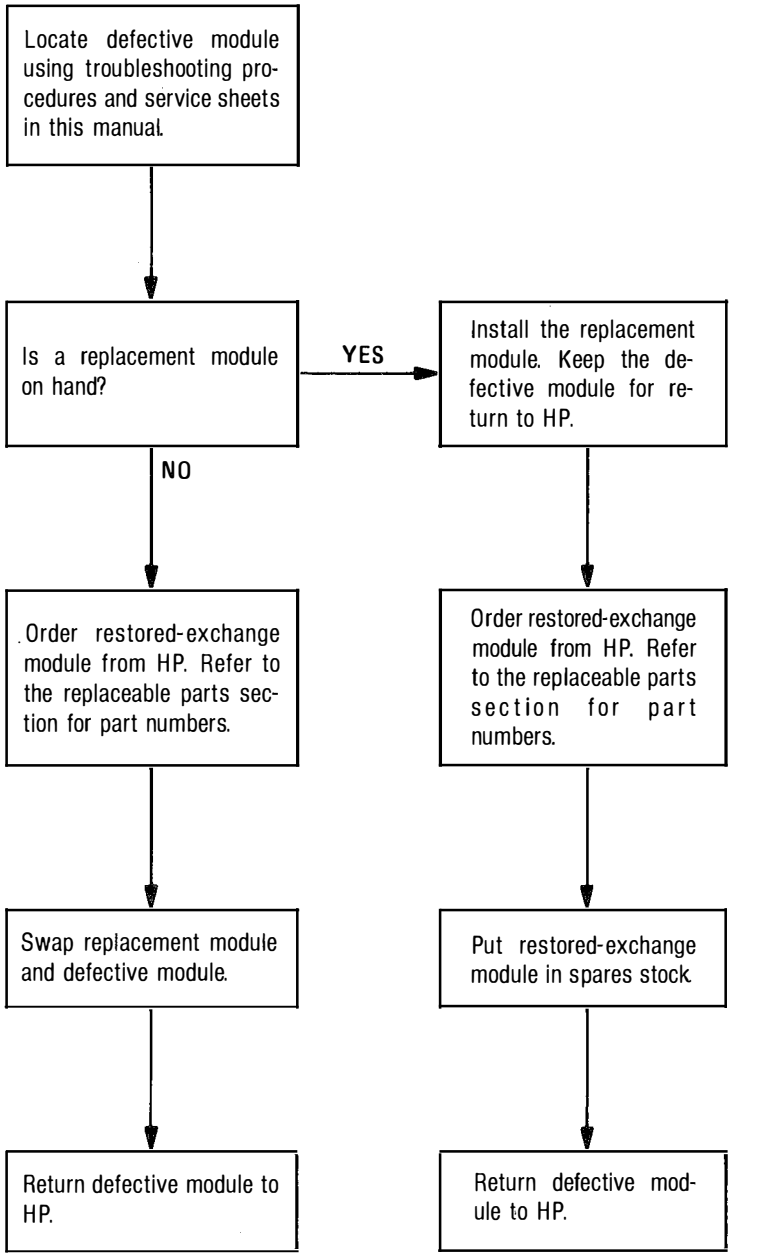
Mix one part deionized water with two parts isopropyl alcohol. Apply this solution to a clean, lint free, cloth (HP Part Number 9310-0039 CD3). Rub the fingers carefully and then dry with a clean part of the cloth.

MODULE EXCHANGE PROGRAM

Table 6-1 (in Volume 2, Section VI Replaceable Parts) lists assemblies within the instrument that may be replaced on an exchange basis, thus affording a considerable cost saving. Exchange, factory-repaired and tested assemblies are available only on a trade-in basis; therefore, the defective assemblies must be returned for credit. For this reason, assemblies required for spare parts stock must be ordered by the new assembly part number.

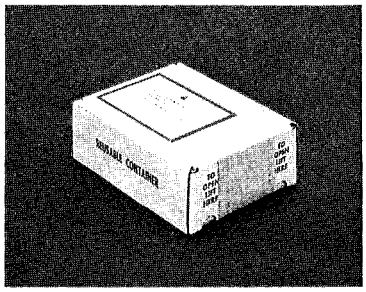
Table 8A-6. Omitted

The module exchange program described here is a fast, efficient, economical method of keeping your Hewlett-Packard instrument in service.



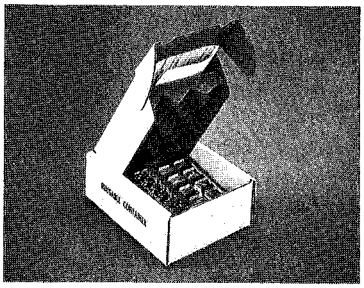
*HP pays postage on boxes mailed in U.S.A.

A.



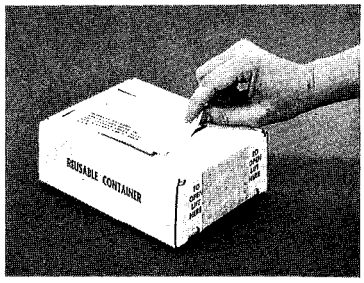
Restored-exchange modules are shipped individually in boxes like this. In addition to the circuit module, the box contains:
Exchange assembly failure report
Return address label

B.



Open box carefully - it will be used to return defective module to HP. Complete failure report. Place it and defective module in box. Be sure to remove enclosed return address label.

C.



Seal box with tape. Inside U.S.A.*, stick preprinted return address label over label already on box, and return box to HP. Outside U.S.A., do not use address label: instead address box to the nearest HP office.

Figure 8A-11. Module Exchange Program Instructions

AFTER SERVICE SAFETY CHECKS

Visually inspect the interior of the instrument for any signs of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. Determine and remedy the cause of any such condition.

Using a suitable ohmmeter, check the resistance from the instrument enclosure to the ground pin on the power cord plug. The reading must be less than one ohm. Flex the power cord while making this measurement to determine whether intermittent discontinuities exist.

Check the resistance from the instrument enclosure to the line and neutral (tied together) with the line switch on the ac mains disconnected. The minimum acceptable resistance is 2 megohms. If the instrument does not pass either of the above tests, **do not connect the instrument to the ac mains**. Troubleshoot the source of the problem at once.

Check the line fuse to verify that a correctly rated fuse is installed. Make sure the line module's line voltage selector pc board is set to the correct voltage.

AIR FILTER REPLACEMENT

CAUTION

The following procedure must be performed periodically to retain the safety features which have been designed into the instrument.

The air filter (HP Part Number 08340-00018 for pkg of 10), attached to the cooling fan assembly (rear panel), will require periodic replacement. Due to the variety of environmental conditions, the interval between replacement cannot be estimated. These filters are inexpensive, and do not lend themselves to cleaning. Filter replacement is therefore most cost-effective. Replace as follows:

1. Disconnect the line power cord.
2. Remove four screws holding the air filter housing to the rear panel.
3. Replace the filter and reassemble.

BASIC COMPONENT SYMBOLOGY

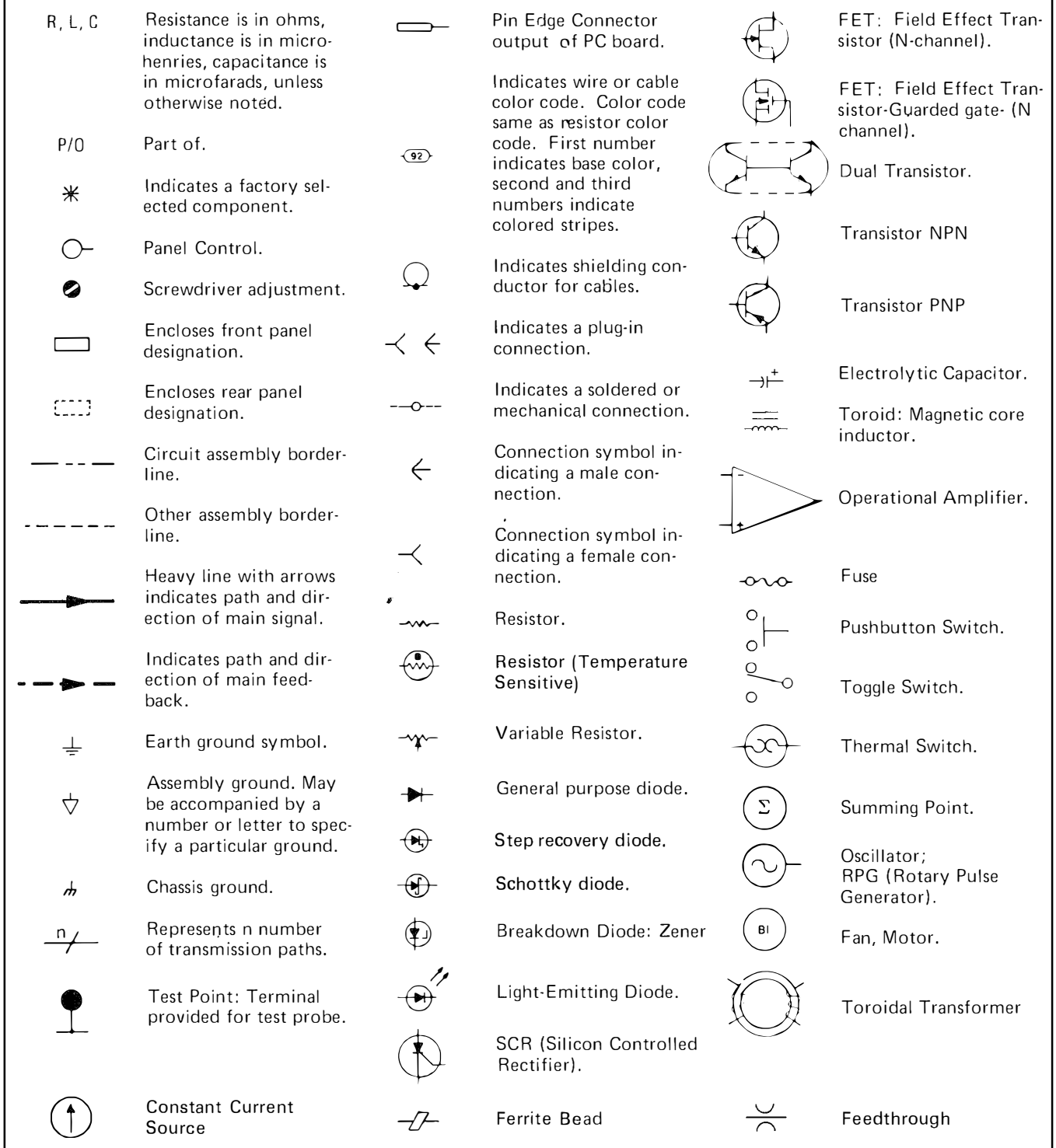


Figure 8A-12. Schematic Diagram Notes (1 of 2)

LOGIC SYMBOLOGY

	AND Gate		NOR Gate		Inverter
	OR Gate		Exclusive OR Gate		Negation symbol. Line is active low.
	NAND Gate		Buffer/Amplifier		Indicated edge-sensitive input.
	Wired OR				

FUNCTION LABEL ABBREVIATIONS

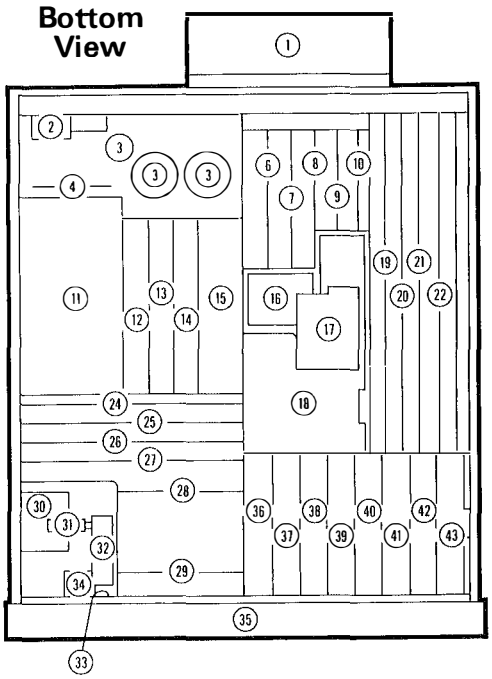
Σ	Adder	◇	Open Collector	LED	Light-Emitting Diode
	Amplifier/Buffer		Non Retriggerable Monostable Multivibrator	MUX	Multiplexer
	Schmitt Trigger		Retriggerable Monostable Multivibrator	RAM	Random-Access Memory
&	AND	BCD	Binary Coded Decimal	REG	Register
≥1	OR	CTR	Counter where n = number of bits in counter	ROM	Read Only Memory
=1	Exclusive OR	DAC	Digital-to-Analog Converter	RPG	Rotary Pulse Generator
X→Y	Encoder, Decoder	FF	Flip-Flop	3-ST	3 State
	Edge sensitive	I/O	Input/Output	H PRI	Highest Priority Encoder
		AN SW	Analog Switch	SREG n	where n = number of bits shifted

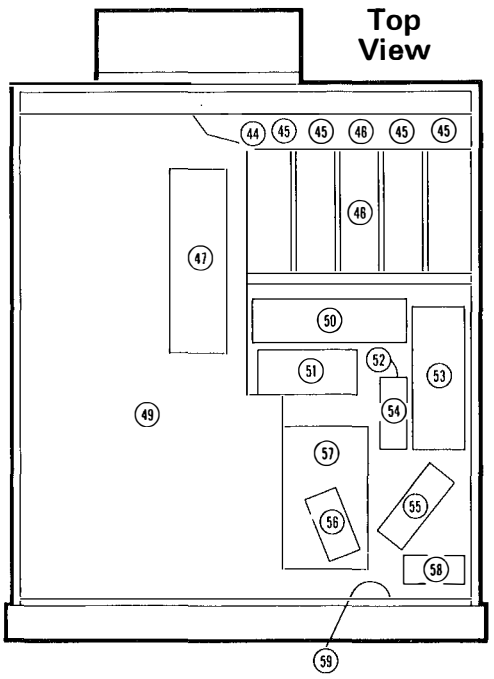
LINE LABEL ABBREVIATIONS

C	Control	MSB	Most Significant Bit	T	Trigger Input (Monostable)
D	Data or Delay Input (Flip-Flop)	NC	No Connection	WR	Write
◀▶	Direction	Q	Output	+1	Count Up
EN	Enable, 3-State Enable Input	$\overline{Q}$	Not Q Complement of Q	−1	Count Down
G	Gating Input	R	Reset or Clear Input		
LSB	Least Significant Bit	RD	Read		
		S	Set Input		
		▼	3 State Output		

Figure 8A-12. Schematic Diagram Notes (2 of 2)

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 3					Volume 4		
			Ref.-M/N Loops	20-30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	33					●			
A2	Display Driver	33					●			
A3	Display Processor	33					●			
A4	Not Assigned	-								
A5	Keyboard	35					●			
A6	Keyboard Interface	35					●			
A7	Lower Keyboard	35					●			
A8	3.7 GHz Oscillator	57						●		
A9	Band 0 Pulse Modulator	56						●		
A10	Directional Coupler	32						●		
A11	Band 1-4 Detector	31						●		
A12	Band 0 Splitter/Detector	34						●		
A13	SYTM (Switched YIG Tuned Multiplier)	30						●		
A14	Band 1-4 Power Amplifier	53						●		
A15	Band 0 Low Pass Filter	52						●		
A16	Band 1-4 Modulator/Splitter	51						●		
A17	Band 0 Mixer	54						●		
A18	Band 0 Power Amplifier	55						●		
		60						●		
A19	Capacitor Assembly	48								●
A20	RF Section Filter	50						●		
A21	Pulse Modulator Driver	29						●		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRO Bias	28						●		
A25	ALC Detector	27						●		
A26	Linear Modulator	26						●		
A27	Level Control	25						●		
A28	SYTM Driver	24						●		
A29	Reference Phase Detector	12	●							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	●							
A31	M/N Phase Detector	14	●							
A32	M/N VCO (Voltage Controlled Osc.)	15	●							
A33	M/N Output	15	●							
A34	Reference-M/N Motherboard	5	●							
A35	Rectifier	4								●
A36	PLL1 VCO (Voltage Controlled Osc.)	36		●						
A37	PLL1 Divider	37		●						
A38	PLL1 IF	38		●						
A39	PLL3 Upconverter	39		●						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		●						
A41	PLL2 Phase Detector	41		●						
A42	PLL2 Divider	42		●						
A43	PLL2 Discriminator	43		●						
A44	YIG Oscillator (YO)	18			●					
A45	Directional Coupler	18			●					
A46	7 GHz Low Pass Filter	18			●					
A47	Sense Resistor Assembly (YO circuit)	47			●					
	(SYTM circuit)	47						●		
A48	YO Loop Sampler	18			●					
A49	YO Loop Phase/Detector	18			●					
A50	YO Loop Interconnect	17			●					
A51	Reference Oscillator	16	●							
A52	Positive Regulator	6								●
A53	Negative Regulator	7								●
A54	YO Pretune/Delay Compensation	8			●					
A55	YO Driver	9			●					
A56	−15V Regulator	10								●
A57	Marker/Bandcross	19					●			
A58	Sweep Generator	20			●					
A59	Digital Interface	21					●			
A60	Processor	22					●			
A61	Not Assigned	23					●			
A62	Motherboard	49				●				
A63	90 dB RF Attenuator	59						●		
AT1	Peripheral Mode Isolator	58						●		
AT2	15 dB Attenuator	18			●					
B1	Fan Assembly	1								●
A62C1-3	Power Supply Filter Capacitors	3								●
FL1	AC Line Module	2								●
A62Q1-4	Power Supply Regulating Transistors	45								●
A62S1	Power Supply Thermal Switch	44								●
T1	Power Supply Translormer	11								●
A62U1	Power Supply Regulator	46								●

M/N LOOP – REFERENCE LOOP B

REFERENCE LOOP - M/N LOOP
INTRODUCTION

This section provides information and instruction for troubleshooting, repairing, or replacing assemblies and components in the Reference Loop and the M/N Loop. Information includes circuit descriptions, troubleshooting procedures, block diagrams, schematics, and component location diagrams for each printed circuit board assembly.

The Reference Loop produces all of the translation and reference signals that are used in the other phase-locked loops in the 8340A.

The Reference Loop consists of the following sections:

* A29 Reference Phase Detector Assembly

* A30 100 MHz VCXO Assembly

The M/N Loop generates the 177-197 MHz signal that drives the A48 Sampler in the YO Loop.

The M/N Loop consists of the following sections:

* A31 M/N Phase Detector Assembly

* A32 M/N VCO Assembly

* A33 M/N Output Assembly

REFERENCE LOOP AND M/N LOOP THEORY OF OPERATION

REFERENCE LOOP DESCRIPTION

The Reference Loop produces all of the translation and reference signals that are used in the other phase-locked loops in the 8340A. These signals are all derived from either the internal 10 MHz Standard (A51) or an external 10 MHz source connected to the EXT REF BNC connector on the rear panel. The frequency stability of the 8340A is directly related to the stability of this 10 MHz signal.

The Reference Loop consists of two assemblies:

1. A29 Reference Phase Detector board
2. A30 100 MHz VCXO board

The Reference Phase Detector Board compares the phase of the 10 MHz reference to the divided-by-10 output of the 100 MHz VCXO and generates a tuning voltage for the VCXO so that phase lock can be achieved. The 10 MHz reference signal is buffered and then converted into a pulse train which drives a sampler where the actual phase detection is performed. The output of the sampler is integrated and then applied as a tuning voltage to the 100 MHz VCXO on A30 100 MHz VCXO board. The VCXO is a crystal-stabilized voltage-controlled oscillator with exceptional noise performance. The tuning range of the VCXO is approximately ±1 kHz of its nominal frequency. The output of the 100 MHz VCXO is buffered and then split several ways. One output is used to drive the sampler in the A8A1 3.7 GHz Oscillator Assembly. Another output is first quadrupled in frequency (to 400 MHz) amplified and then sent to A31 M/N Phase Detector where it drives the RF port of a down converting mixer. The remaining output is amplified and sent back to the A29 Reference Phase Detector Board where four more reference signals are derived. On A29 this 100 MHz signal is first divided by 5 to 20 MHz, and then divided by 2 to 10 MHz. The 20 MHz signal is amplified and sent to the A31 M/N Phase Detector where is becomes the reference for the M/N loop. The 10 MHz signal drives three buffers whose outputs go to:

1. 20-30 Loop A42 PLL1 Divider
2. 20-30 Loop A37 PLL2 Divider
3. Rear Panel 10 MHz Reference Output

Finally the 10 MHz signal is amplified and sent to the sampler thereby completing the return path of the Reference phase-locked loop. A block dagram of the Reference and the M/N Loops is shown in Figure 8B-1, Reference and M/N Simplified Block Diagram.

M/N LOOP DESCRIPTION

The M/N Loop generates the 177-197 MHz signal that drives the A48 Sampler in the YO Loop. Harmonics of the M/N signal are generated in the Sampler and are used to down convert the 2.3-7.0 GHz YO output to the 20-30 MHz range so that the YO can be phase locked to the output of the 20-30 Loop.

The M/N Loop consists of three assemblies:

1. A31 M/N Phase Detector board
2. A32 M/N VCO Assembly
3. A33 M/N Output board

The M/N Phase Detector Board contains a phase detector, a mixer, and two programmable frequency dividers. (Refer to Figure 8B-1, Reference and M/N Simplified Block Diagram) The mixer is used to down convert the VCO output signal (from A33) from 355-395 MHz to 5-45 MHz by using the 400 MHz reference signal from A30 100 MHz VCXO. This 5-45 MHz IF signal is then divided in frequency by the M divider, one of the two identical programmable dividers on this board. The M divider is programmed to divide by an integer ranging from 8 to 27. The phase of the output of this divider is compared to the output of the other programmable divider, the N divider, in the phase detector whose differential output is used to tune the VCO. This tune voltage keeps the M/N Loop phase locked to the output of the N divider. The N divider is programmed to divide the 20 MHz reference signal by an integer from 13 to 36.

The M/N VCO is a foreshortened cavity resonator that is varactor tuned from 355 to 395 MHz. The M/N VCO assembly consists of the cavity oscillator and a small PC board. This assembly is mounted on A33 M/N Output Board. On A33, the output of the VCO is split two ways. One output is used for closing the phase locked loop, and the other is used to generate the YO Loop Sampler drive. The phase lock path contains an amplifier that drives the down converting mixer on the A31 M/N Phase Detector board. The YO Loop Sampler path contains an amplifier and then a divide-by-2 circuit that produces a Sampler Drive signal in the range of 177-197 MHz.

The YO Loop Sampler drive output of the M/N Loop (after being divided by 2) can be related to the M and N numbers by the following equation:

$$f_{M/N} = 200 - 10 * (M/N) \text{ MHz}$$

The Nth harmonic of this signal is used in the YO Loop Sampler (A48) to down-convert the 2.3-7.0 GHz YO output to 20-30 MHz. For every increment in M number, the YO output will decrease by 10

MHz, and for every increment in N number, the output will increase by 200 MHz. This relationship is given in the following equation where $f_{20,30}$ is the output of the 20 to 30 Loop:

$$f_{YO} = 200*N - 10*M - f_{20,30} \text{ MHz}$$

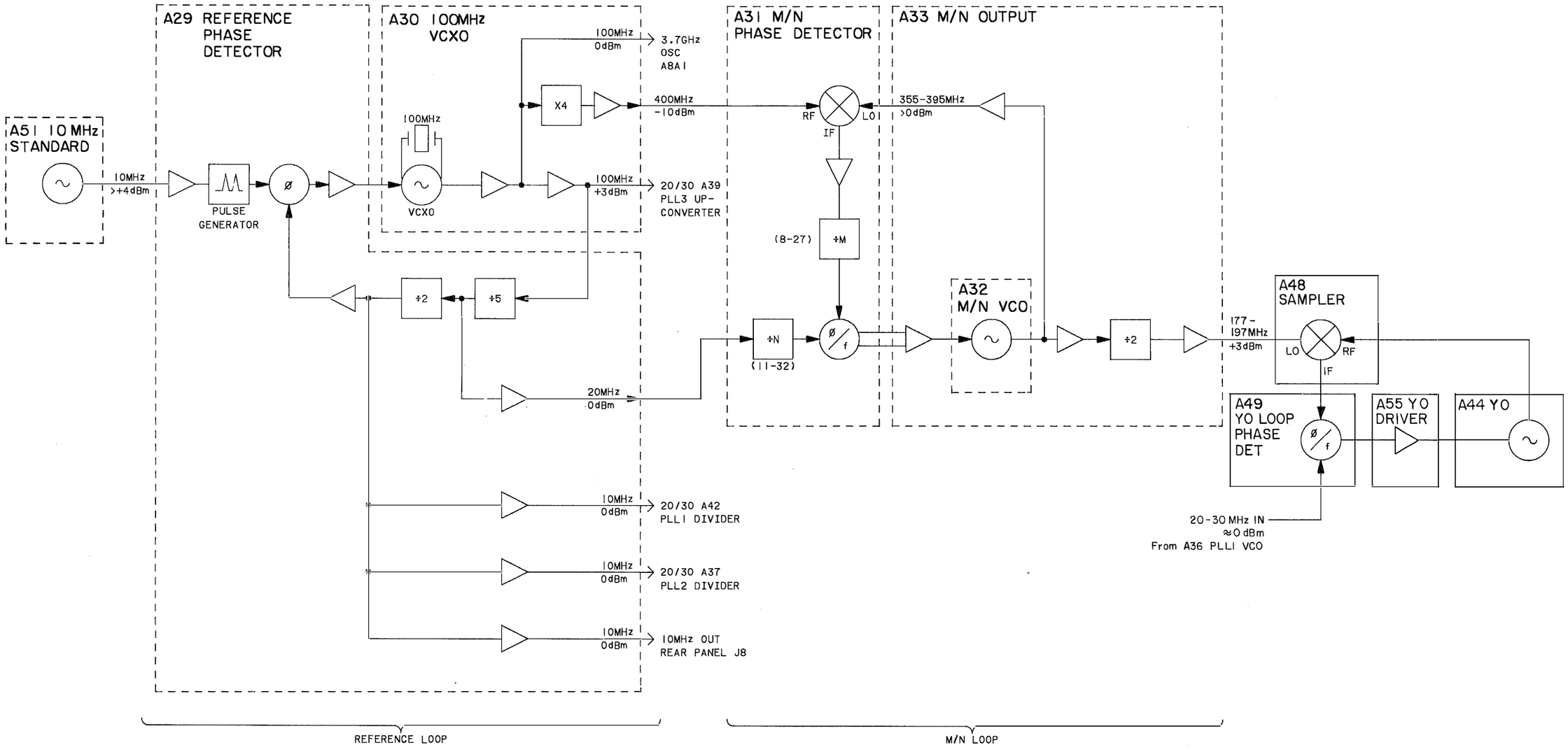


Figure 8B-1. Reference and M/N Simplified Block Diagram

REFERENCE LOOP - M/N LOOP
TROUBLESHOOTING TO ASSEMBLY LEVEL

REFERENCE UNLOCK TROUBLESHOOTING

First check that the INT/EXT switch on the rear panel is in "INT" position.

Check that a jumper cable is connected between rear panel connectors "INT" and "EXT".

Check that there is a 10 MHz, 0 dBm signal out of the "INT" jack on the rear panel.

If there is no 10 MHz signal at the rear panel, the problem is probably the 10 MHz Standard, A51, or the power supplies to it. Refer to Figure 8B-2, Reference Loop - M/N Loop Block Diagram. If the power supplies are present, and there is no 10 MHz output signal at A51J1, replace the Reference Oscillator. (Note: +20 V to A51 is switched on by "HSTD" on the positive regulator board, A52).

If there is a good 10 MHz signal at the rear panel, the problem is probably on the Reference Phase Detector board, A29, or the 100 MHz VCXO, A30.

Measure the voltage on TP1, "TUNE", on the cover of A30 board. This voltage should be approximately -8 volts. If it is at -8 volts then the Reference Loop is most likely locked up and the problem is on the unlock detector portion of the A29 Reference Phase Detector or A59 Digital Interface board.

If the voltage is not -8 volts, adjust A30C4 and see if it will vary the tune voltage.

If the tune voltage was off by more than 3 volts and A30C4 is able to bring it back to -8 volts, then the 100 MHz VCXO crystal, A30Y1, is probably drifting too much and should be replaced.

If A30C4 is not able to vary the tune voltage, then suspect low power or a missing signal out of A30J1, or a missing 10 MHz reference on A29. See Section V, Adjustments, for verification of 100MHz VCXO. See theory description of 10 MHz Reference Phase Detector, A29.

M/N UNLOCK TROUBLESHOOTING

In order for the M/N Section to lock up, the Reference Section must be locked. (Refer to Figure 8B-2, Reference Loop-M/N Loop Block Diagram)

Check that a 20 MHz signal at 0 dBm +3dB is coming out of A29J2. If there is no 20 MHz signal or it is low in power, then there is most likely a problem on the A29 Reference Phase Detector board.

Check that there is 400 MHz at -10 dBm + 3dB coming out of A30W1. If there is no 400 MHz signal or it is low, then there is probably a problem on the A30 VCXO board.

If both of the above signals are correct, then the problem is most likely on the A31 M/N Phase Detector board or the A33 M/N Output board.

Set up the 8340A by pressing **[INSTR PRESET] [CW] [2] [.] [4] [9] [GHz], [SHIFT] [M1]**. In the "POWER dBm" window are the numbers 08 13. The number 08 is the M DIVIDE number and number 13 is the N DIVIDE number. In the first frequency window is a frequency that is expected out of A33J2 M/N OUT. Measure the frequency out of A33J2. (NOTE: When measuring the M/N frequency, it is advisable to have the 8340A and the measuring device, ie. counter or spectrum analyzer, both locked to the same 10 MHz standard.)

If the measured frequency and the frequency in the first window are the same and the M/N Loop is still unlocked, then the problem is most likely on the UNLOCK indicator portion of the A31 M/N Phase Detector board or the UNLOCK Detector portion of the A59 Digital Interface board.

If there is no signal out of A33J2, then the problem is most likely on the A33 M/N Output board or the A32 M/N VCO. See Section V, Adjustments, for details on verifying the M/N VCO and Output board.

If the measured frequency and the indicated frequency do not match, then the problem is most likely on the A31 M/N Phase Detector board or the A33 M/N Output board. It is now important to see if the M/N output frequency is off due to divider failure on A31 or VCO tuning failure on A32 or A33.

Press **[SHIFT] [CF] [1] [0] [MHz] [CW]**. This sets the 8340A up to step the CW frequency in 10 MHz increments. For each 10 MHz step, the "M" Divide number will change by a value of 1. Step the CW frequency from 2.49 GHz to 2.3 GHz ("M" Number from 8 to 27). At each step, record the measured M/N output frequency and the frequency displayed in the first window.

Check the list of frequencies. If some of the measurements match

and some do not, then the problem is most likely on the M Divider portion of the A31 M/N Phase Detector board.

Press **[SHIFT] [CF] [2] [0] [0] [MHz] [CW]**. This sets the 8340A to step the CW frequency in 200 MHz increments. For each 200 MHz step, the "N" Divide number will change by a value of 1. Step the CW frequency from 2.3 GHz to 6.9 GHz ("N" Number from 13 to 36). At each step, record the measured M/N output frequency and the frequency displayed in the first window.

Check the list of frequencies. If some of the measurements match and some do not, then the problem is most likely on the N Divider portion of the A31 M/N Phase Detector board.

If the measured frequencies in the above two tests do not change as the M or N number is changed, then the problem is most likely on the A33 M/N Output board or the A32 M/N VCO.

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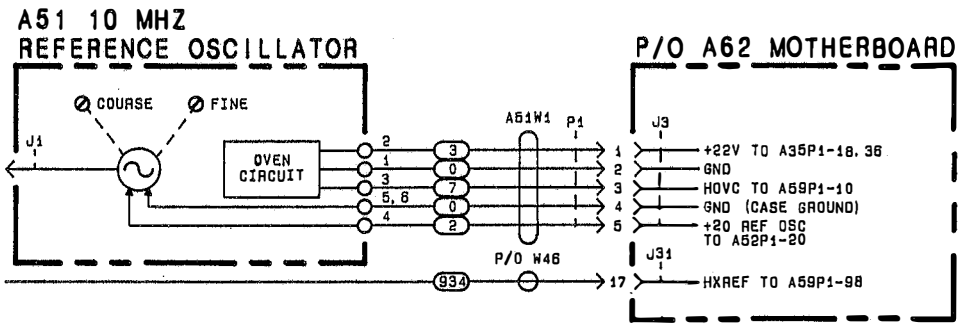


P/O Figure 8B-2. Reference Loop - M/N Loop Block Diagram

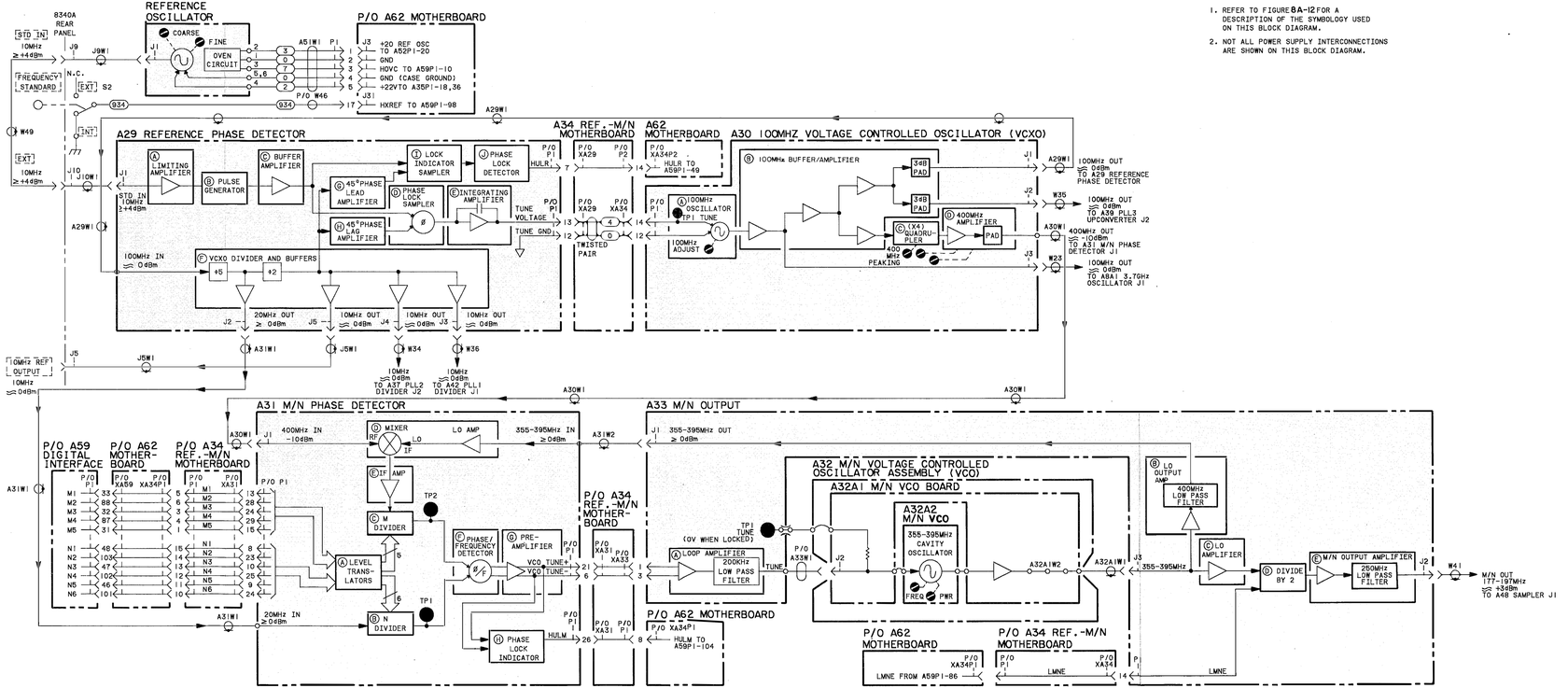


Figure 8B-2. Reference Loop — M/N Loop Block Diagram

REPAIR PROCEDURES

Refer to the REPAIR PROCEDURES description in the beginning of Section VIII.

A29 REFERENCE PHASE DETECTOR

INTRODUCTION

The A29 Reference Phase Detector contains the frequency divider, phase detector, and integrating amplifier for the 100 MHz Reference phase-locked loop. Basically, 100 MHz from the A30 VCXO is divided by 10 and compared to the 10 MHz frequency standard by the phase detector. The error voltage from this comparison is fed back to the VCXO to keep its frequency locked to 10 times that of the frequency standard. The bandwidth of the reference phase-locked loop is 100 Hz; the 10 MHz derived from the 100 MHz VCXO must be within 100 Hz of the 10 MHz frequency standard for the loop to lock reliably. Refer to Figure 8B-4, A29 Reference Phase Detector, Schematic Diagram.

A29 REFERENCE PHASE DETECTOR CIRCUIT DESCRIPTION

Limiting Amplifier A

U1 amplifies and limits the amplitude of the 10 MHz signal from the frequency standard. U1A and U1B form a limiting differential pair, while the emitter follower, U1C, provides a low impedance output.

Pulse Generator B

U2D is biased with feedback resistor R10 to further limit the 10 MHz signal to a well-shaped square wave and set the proper logic levels for digital buffer U2C. U2A and U2B generate narrow pulses, the width being the gate delay of U2A plus the delay from R11 and C5. When the output of U2C goes low, the output of U2B goes high after one gate delay (of U2B). After a delay due to R11, C5, and U2A gate delay, the output of U2A goes high which causes U2B output to return low again, thus generating a narrow pulse.

Phase Lock Sampler D

The phase lock sampler performs the function of phase detector. The 10 MHz pulses from the buffer amplifier are applied to the primary of T1 which causes CR3 and CR4 to turn on for the duration of the pulses. This samples the divided by 10 VCXO frequency and stores this voltage on C26. When the loop is locked, the feedback due to the complete phase-locked loop forces this voltage to be nearly zero. When the loop is unlocked, this voltage may be zero or varying, depending on the reason for unlock.

Integrating Amplifier E

Q4 is a differential input pair which together with Q5 and Q6 forms a high gain amplifier. Feedback is added with C32 and R49 to make an integrating amplifier. C32 provides ac feedback only, so for the amplifier to remain linear, dc feedback is accomplished by virtue of the entire phase-lock loop.

VCXO Divider and Buffers F

A 100 MHz signal from A30 VCXO is applied to counter U3 which divides by 5, then by 2. Its outputs are 10 MHz and 20 MHz which are buffered by U4 to be used as reference frequencies by other assemblies in the instrument. The other 10 MHz output is used to drive the Phase Lock Sampler **D** and Lock Indicator Sampler **I**.

Fourty Five Degree Phase Lead Amplifier G and Fourty Five Degree Phase Lag Amplifier H

The 45 degree phase shift buffers are used to provide two 10 MHz signals which are 90 degrees apart in phase. The purpose of these signals is explained in Lock Indicator Sampler **I** description. the 45 degree phase shift in **G** is accomplished with C35 and R53, while in **H** it is done by R59 and C38.

Lock Indicator Sampler I

The lock indicator sampler functions the same as the phase lock sampler **D**. The only difference is that the 10 MHz is 90 degrees shifted in phase. This causes the output of the lock indicator sampler to be a maximum negative voltage when the loop is locked.

Phase Lock Detector J

The output of the lock indicator sampler is compared to -0.5 volt by U5. When the output voltage becomes closer to 0 than to -0.5 volt, U5 switches its output to TTL high to indicate to the A59 Digital Interface that the loop is unlocked.

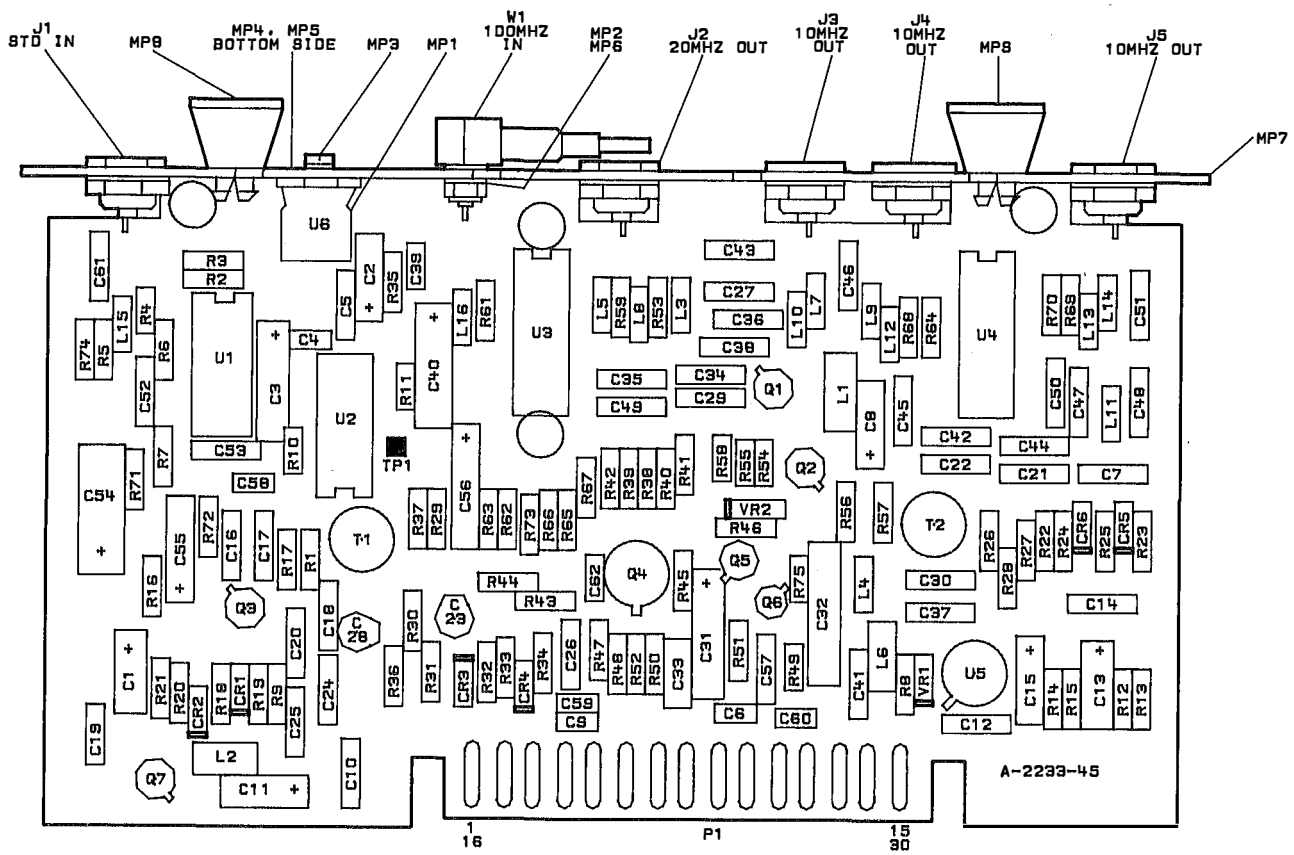


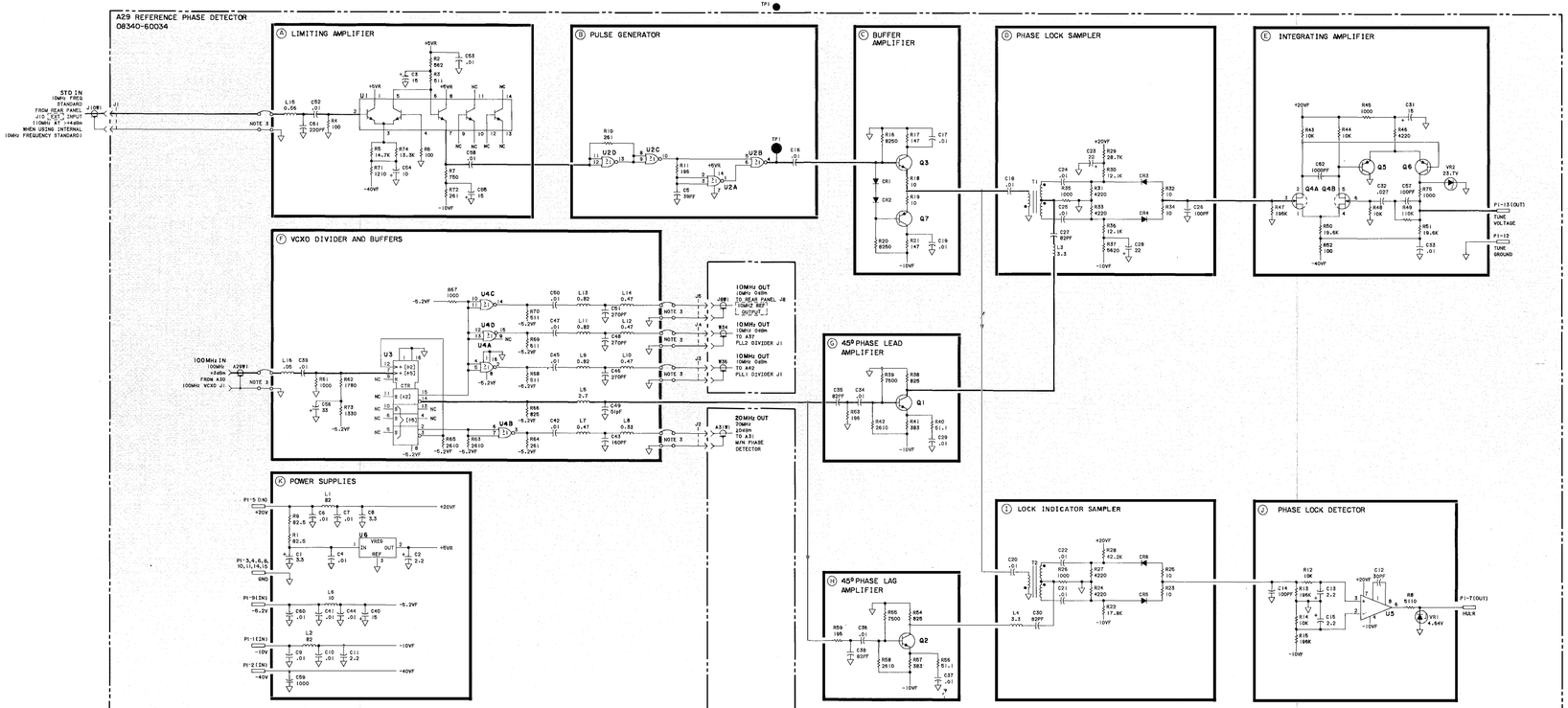
Figure 8B-3. A29 Reference Phase Detector, Component Location Diagram

A29 Reference Phase Detector Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1	−10V	−10V	XA34P2-8, 9	*K
2	−40V	−40V	XA34P2-6, 7	*K
3	GND	0V	INSTRUMENT GROUND	*K
4	GND	0V	INSTRUMENT GROUND	*K
5	+20V	+20V	XA34P2-2, 3	*K
6	GND	0V	INSTRUMENT GROUND	*K
7	HULR	TTL (HIGH TRUE)	J	XA34P2-14
8	GND	0V	INSTRUMENT GROUND	*K
9	−5.2V	−5.2V	XA34P2-12, 13	*K
10	GND	0V	INSTRUMENT GROUND	*K
11	GND	0V	INSTRUMENT GROUND	*K
12	TUNE GROUND	0V	E	XA30P1-12
13	TUNE VOLTAGE		E	XA30P1-14
14	GND	0V	INSTRUMENT GROUND	*K
15	GND	0V	INSTRUMENT GROUND	*K

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A34 Reference Loop — M/N Motherboard Schematic Diagram for a complete representation of signal sources and destinations.



NOTES:

1. REFER TO THE SERVICE SECTION INTRODUCTION FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES SHOWN ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN NANOHENRIES UNLESS OTHERWISE NOTED.
3. J1-J5 AND A30W1 CENTER CONDUCTORS ARE ELECTRICALLY CONNECTED TO THE PC BOARD THROUGH SOLDERED 24 GAUGE FINE WIRES. THEIR OUTER CONDUCTORS ARE ELECTRICALLY CONNECTED THROUGH MECHANICAL SCREW CONNECTIONS IN THE ASSEMBLY COVER PLATE.

Figure 8B-4. A29 Reference Phase Detector, Schematic Diagram

A30 100 MHz VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR (VCXO)

INTRODUCTION

The A30 100 MHz VCXO contains a Voltage Controlled Crystal Oscillator, a 100 MHz Buffer Amplifier, a frequency Quadrupler, and a 400 MHz Amplifier. With the A29 Reference Phase Detector, it forms the Reference Phase-Locked Loop. The 100 MHz and 400 MHz outputs are used as frequency references by other assemblies in the instrument. Refer to Figure 8B-6, A30 100 MHz VCXO, Schematic Diagram.

A30 100 MHz VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR CIRCUIT DESCRIPTION

100 MHz Oscillator A

Q5 and associated circuitry function as a 100 MHz Voltage Controlled Crystal Oscillator. Q5 is a common-base amplifier with positive feedback to form an oscillator. The signal at the output of Q5 goes through the parallel combination of C8 and C4, where it is limited to an amplitude swing of ±0.4 V by CR3, CR4, and R7 and becomes the output signal to the 100 MHz Buffer Amplifier (Block **B**). This output signal is also divided down by C11 and C10 to a level of ±0.25 V and fed back to the emitter of Q5 through the 100 MHz crystal, Y1, and the varactor diode, CR1. This completes the feedback loop and causes Q5 to oscillate.

The frequency controlling elements of the feedback network are Y1, CR1, C4, and C8. Y1, a 100 MHz quartz crystal, is the principle frequency-determining element. CR1, a varactor diode, provides the electrical tuning for the oscillator. Changing the (reverse) bias voltage on the varactor varies it's capacitance; this varies the phase shift of the feedback path around the oscillator and thus changes the oscillator frequency. The tuning input for the varactor comes from the output of the A29 Reference Phase Detector. It can tune the oscillator ±1 kHz as needed to lock the loop. C4 is a variable capacitor that is used to manually adjust the center of the tuning range to 100 MHz.

The tune voltage is applied to CR1 through L19, R53, R5, L4, L3, R54, and L18. This voltage, TUNE, is brought out to a test point, TP1, on the top cover of the casting that houses the board. C4 is adjusted with the loop locked so that TUNE is approximately -8.0 Vdc; this centers the tuning range. L4 is a factory-selected inductor that is used to adjust the symmetry of the oscillator output signal over the VCXO tuning range. The signal level must be maximum at 100 MHz and it must, over its tuning range, be symmetrical about 100 MHz.

R1, R2, R3, R11, R54, and L1 determine the bias and gain of Q5. TP3 should be at approximately -14.8 Vdc for correct bias.

100 MHz Buffer Amplifier B

Transistors Q9 and Q8 function as buffer amplifiers to isolate the VCXO from variations in load which would otherwise cause frequency pulling of the oscillator. Q9 is an emitter-follower amplifier which presents a high impedance to the VCXO output. Q8 buffers the output of Q9. Components L6, C15, and C16 form a tuned circuit to match the impedance of the collector output of Q8 to 50 ohms. This signal, 100 MHz OUT, is sent to the A8 3.7 GHz Oscillator.

The signal at the emitter of Q8, equal to the input signal (emitter-follower configuration), is input to the emitter of Q11, a common-base buffer amplifier. The output at the collector of Q11, through the tuned circuit of L7, C19, and C20, is applied to the power splitter, T3, which splits the signal into two paths.

In one path, the signal from T3 goes to Q6 through a 3 dB pad. Q6 is a common-emitter amplifier with emitter degeneration (R27) for gain stability. The output at the collector of Q6, through the tuned circuit of L8, C27, and C28, is applied to the power splitter, T2, which splits the signal into two paths. In each path, the signal goes through a 3 dB pad and a tuned LC circuit and becomes the 100 MHz OUT signal sent to the A29 Reference Phase Detector and the A39 PLL3 Upconverter.

In the second path from power splitter T3, the signal goes to Q7, a common-emitter buffer amplifier. The output at the collector of Q7, through the tuned circuit of L9, C32, and C33, is applied to the Quadrupler, Block **C**.

Quadrupler C

The 100 MHz signal from Q7 in Block **B** is applied to power splitter T1. The two outputs of T1 are input to transistors Q3 and Q4, which form a Class C amplifier, full-wave rectifier circuit. Positive half-cycles of the 100 MHz signal into T1 turn on Q3 while negative half-cycles turn on Q4. The collector outputs are connected together to provide a fullwave rectified signal that is rich in even harmonics. The tank circuit of C3 and L10 is tuned to pass the 4th harmonic, 400 MHz. This signal is applied to the 400 MHz Amplifier, Block **D**.

400 MHz Amplifier D

Q2 and Q1 are both common-emitter amplifiers which have approximately 20 dB gain each. Both have tuned outputs to filter

undesired harmonics of 100 MHz. The output of Q1 is passed through a pad comprised of R67, R68, and R69. The nominal attenuation of the pad is 5 dB, however the actual attenuation is selected to set the 400 MHz OUT signal level to -10 dBm ±1 dB. This signal is sent to the A31 M/N Phase Detector.

Power Supplies E

Q10, R9, and C43 function as a capacitance multiplier circuit to filter the 20 V supply. The filtering takes place in the base current which controls the collector current. This provides improved noise filtering for a given capacitor value. The voltage at TP2 should be approximately 18.2 V. C48, R62, C49, and C50 filter the -10 V supply, with R62 and the parallel combination of C49 and C50 forming a low-pass filter. The voltage at TP4 should be approximately -8.6 V.

A30 100 MHz VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR TROUBLESHOOTING

100 MHz Oscillator A

REFERENCE UNLOCK

The output of the 100 MHz VCXO should be phaselocked at 100 MHz. When troubleshooting the VCXO for a REFERENCE UNLOCK, first disconnect the cable at A30J1, the 100 MHz OUT signal to the A29 Reference Phase Detector. This breaks the Reference loop. Apply -8.0 Vdc to the TUNE test point, TP1 (on the top cover of the casting that houses the board). This should tune the oscillator to 100 MHz $\pm$100 Hz. (For this test, the board must be kept inside the casting.) If the signal is missing at J1, then troubleshoot Q5 and surrounding circuitry. If the signal is present, then proceed to the Oscillator Adjustment Procedure section below.

The typical bias voltage levels for Q5 are as follows: emitter, -12.8 V; base, -11.9 V; collector, 0.0 V. TP3 should be approximately -14.8 V.

OSCILLATOR ADJUSTMENT PROCEDURE

As stated in the previous section, a dc voltage of -8.0 V applied to TUNE should tune the frequency to 100 MHz $\pm$100 Hz. To test the sensitivity to TUNE, change the voltage to -25.0 V; this should cause the frequency to increase > 1.0 kHz. Apply 0.0 V to TUNE; this should cause the frequency to decrease > 1.0 kHz. If TUNE is not working correctly, then troubleshoot Q5 and surrounding circuitry. If TUNE is working correctly and the frequency at -8.0 V is correct, then troubleshoot the A29 Reference Phase Detector. If the frequency with TUNE at -8.0 V is not 100 MHz $\pm$100 Hz, then proceed in this section.

The value of the inductor, L4, is selected to center the VCXO tuning range about 100 MHz. This assures that the output power is maximum at 100 MHz and the tuning curve is symmetrical about its maximum point. To test this, disconnect cable A30J1 and connect a dc voltage of -8.0 V to TUNE, TP1. Measure the 100 MHz OUT signal with either a signal analyzer or a power meter and frequency counter. Adjust A30C4 so that the signal level is maximum. Record the frequency, A (measured to at least a 10 Hz resolution). Slowly tune to a higher frequency until the power drops 1 dB; record this frequency, B. Tune to a lower frequency until the power drops by 1 dB; record this frequency, C. The VCXO centering is correct if

$$0.5 \leq \frac{(A-B)}{(B-C)} \leq 2.0$$

If the above ratio is less than 0.5, then decrease A30L4 one value to increase the center frequency. If the above ratio is greater than 2.0, then increase A30L4 one value to decrease the center frequency. Repeat as necessary. Refer to Table 8B-1 for inductor values. Note: this adjustment is done at the factory and normally will not need to be repeated unless other components are changed.

Table 8B-1. L4 Inductor Values and Part Number

Value	HP Part Number	Value	HP Part Number
0.68uH	9140-0141	0.33uH	9100-0368
0.56uH	9100-2256	0.27uH	9100-2252
0.47uH	9100-2255	0.22uH	9100-2251
0.39uH	9100-2254		

With -8.0 Vdc applied to TUNE, adjust A30C4 until the oscillation frequency is 100 MHz ±100 Hz. Remove the dc source from TUNE and reconnect the cable at A30J1 to close the Reference Loop. If TUNE changes less than ±1.0 V (from -8.0 V), then readjust A30C4 until TUNE (closed loop) -8.0 V; if TUNE changes more than ±1.0 V, then trouble-shoot the A29 Reference Phase Detector.

100 MHz Buffer Amplifiers B

The signal level of the 100 MHz OUT signals at A30J1, J2, and J3 should be 0 dBm ±1 dB. If no signal is present at J3, then troubleshoot Q9, Q8, and the 100 MHz Oscillator. If the output of J3 is correct but the signal at J2 and/or J1 is low or missing, then troubleshoot the signal path that includes Q11 and Q6.

The approximate bias voltage levels for the transistors in the 100 MHz Buffer Amplifiers is shown in Table 8B-2.

Table 8B-2. Approximate Bias Voltage Levels for 100 MHz Buffer Amplifier

Transistor	Q6	Q7	Q8	Q9	Q11
Emitter	3.8	3.8	4.3	5.0	3.8
Base	4.5	4.5	5.0	5.5	4.5
Collector	9.2	9.1	10.0	11.0	9.3

The 100 MHz OUT signal at J1 and J2 and the 400 MHz OUT signal are set to the correct power level by resistive pads (R30, R31, and R32; R33, R34, and R35; and R67, R68, and R69). The attenuation of these pads is selected to give the required power. For a given level of attenuation, the required resistor values are given in Table 8B-3.

Table 8B-3. Attenuation and Resistor Values for 100 MHz OUT and 400 MHz OUT

ATTENUATION (dB)	RESISTORS (OHMS)		
	R30 R33 R67	R31 R34 R68	R32 R35 R69
3	261	17.8	261
4	215	23.7	215
5	178	31.6	178
6	147	38.3	147
7	133	46.4	133
8	121	51.1	121
9	110	61.9	110

Quadrupler C and 400 MHz Amplifier D

The 400 MHz OUT signal level should be between -9 and -11 dBm. If the signal level is outside these limits, then check also the harmonic levels (see below). If they are out of spec, then make the adjustment of C2 and C3 and then recheck the signal level. If the harmonic levels are correct and the signal level is still low or if the 400 MHz signal is missing, and if the 100 MHz OUT signals are correct, then troubleshoot the signal path that includes the 100 MHz Buffer Amplifier Q7 (Block **B**), the Quadrupler transistors Q3 and Q4, and the 400 MHz Amplifier Q2 and Q1. The typical bias voltage levels for Q1-4 are given in Table 8B-4. To adjust the 400 MHz OUT power level to the required level, then change R67, R68, and R69, referring to Table 8B-3 for values.

Table 8B-4. Approximate Bias Levels for Quadrupler and 400 MHz Amplifier

Transistor	Q1	Q2	Q3	Q4
Emitter	-6.6	-6.6	-4.6	-5.1
Base	-5.9	-5.9	-5.9	-5.9
Collector	0.0	0.0	0.0	0.0

The 200 and 800 MHz harmonics of 100 MHz at A30W1, relative to the 400 MHz signal level, should be at least 25 dB down. The 100, 300, 500, 600, 700, and 900 MHz harmonics should be at least 40 dB down. If the harmonic levels are too high, then adjust A30C1 and A30C2 for the maximum 400 MHz signal level with the lowest possible harmonic levels. Then recheck the 400 MHz OUT signal level.

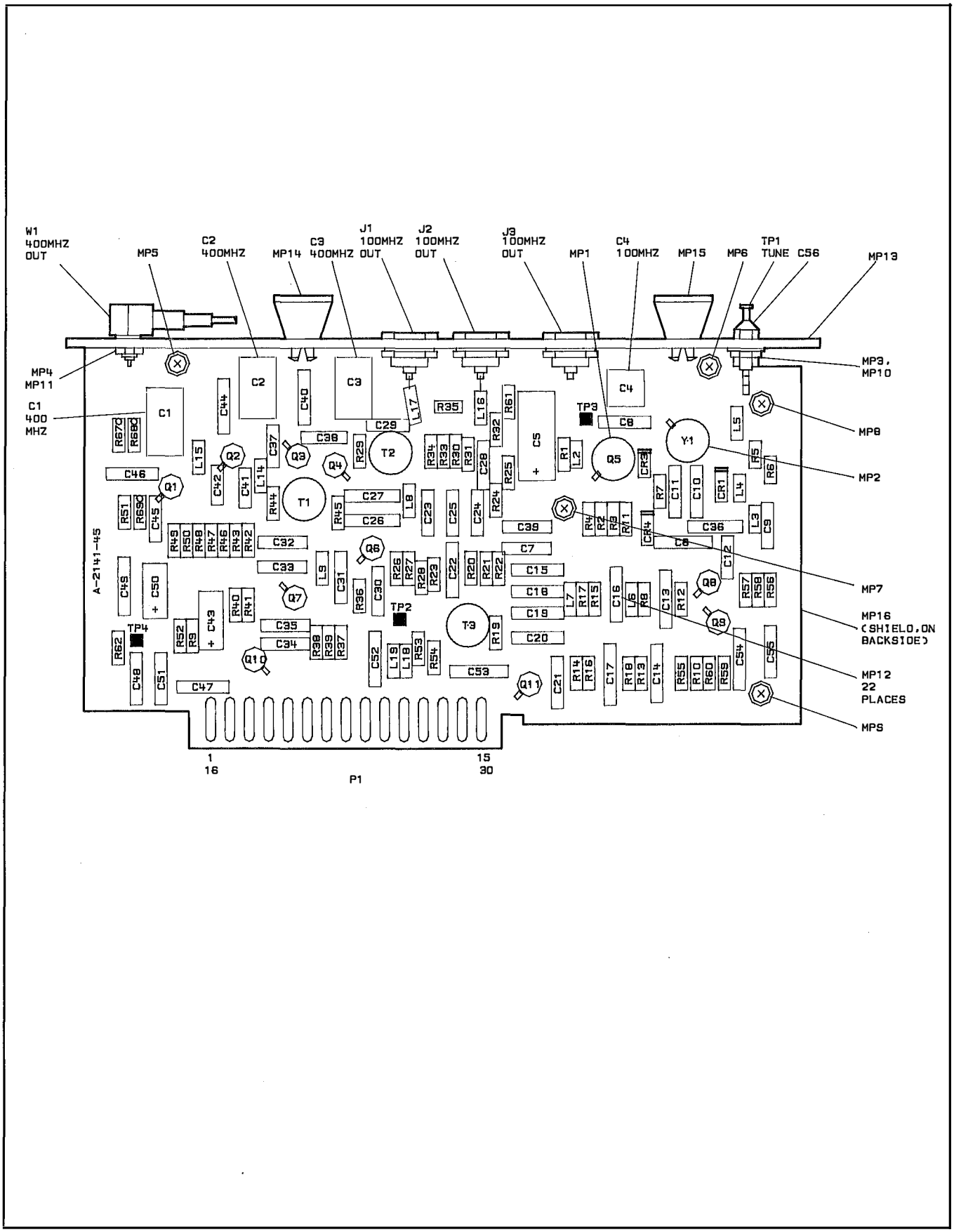


Figure 8B-5. A30 100 MHz VCXO, Component Location Diagram

A30 100 MHz VCXO Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 2	−10V	−10V	XA34P2-8, 9	*E
3 4	−40V	+40V	XA34P2-6, 7	*A
5 6	+20V GND	+20V 0V	XA34P2-2, 3 INSTRUMENT GROUND	*E *E
7 8	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*E *E
9 10	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*E *E
11 12	GND TUNE GROUND	0V 0V	INSTRUMENT GROUND XA29P1-12	*E A
13 14	TUNE VOLTAGE		XA29P1-13	A
15	GND	0V	INSTRUMENT GROUND	*E

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A34 Reference Loop — M/N Motherboard Schematic Diagram for a complete representation of signal sources and destinations.

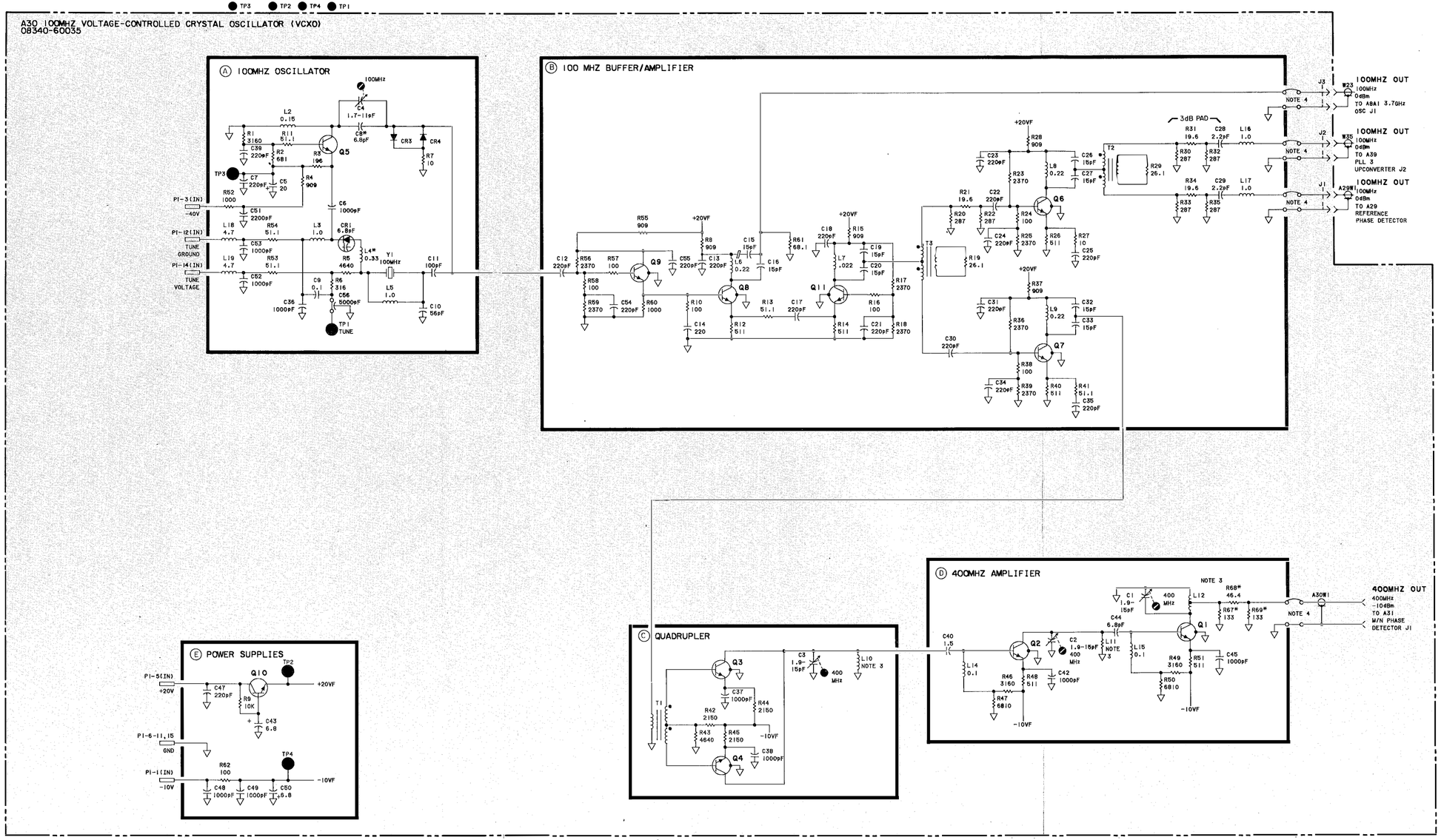


Figure 8B-6. A30 100 MHz VCXO, Schematic Diagram

A31 M/N PHASE DETECTOR

INTRODUCTION

The M/N phase detector has two programmable frequency dividers: an M divider and an N divider. M and N are integer numbers which give the ratio of divider input frequency to divider output frequency (i.e. the divide number). The input to the N divider is 20 MHz; the M divider input is the difference frequency between the M/N VCO (355-395 MHz) and 400 MHz. The two divider outputs are compared in a phase/frequency detector. The detector output is amplified and applied to A33 M/N Output where it is used to tune the M/N VCO.

In general, the M/N output frequency from A33 is (200-10*M/N) MHz. The M/N VCO frequency is twice the M/N output frequency. Refer to Figure 8B-10, A31 M/N Phase Detector, Schematic Diagram.

A31 M/N PHASE DETECTOR CIRCUIT DESCRIPTION

TTL ECL Level Translators A

The numbers to program the frequency dividers come from the A59 Digital Interface in binary at TTL levels. U3, U13, and U17 shift these to ECL levels which are approximately -1 volt logic high and -2 volts logic low. N1 and M1 designate the least significant bits.

N Divider B and M Divider C

The Phase Detector Assembly's M and N Dividers are essentially identical in operation. In each case the input frequency is divided by the divide number (a binary coded number input from the Digital Interface Board). The resulting output pulses are frequency and phase compared to produce an error voltage which ultimately tunes the M/N VCO. The following formulas show the frequency relationship of the inputs and outputs of the dividers:

$$f_N = (4/N)(20\ \text{MHz})$$

$$f_M = (4/M)(f_{IF})$$

Where f_N = N Divider Output pulse repetition frequency (PRF) (MHz).

f_M = M Divider Output PRF (MHz)

N = N Divide Number

M = M Divide Number

f_{IF} = M Divider Clock frequency (MHz)

20 MHz = N Divider Clock frequency

$f_N = f_M$ when the loop is phase locked;

Therefore,

$$(4/N)(20\ \text{MHz}) = (4/M)(f_{IF})$$

and f_{IF} = [(M/N) 20] MHz for the phase locked condition.

Because of the similarities of the M and N Dividers, only the N Divider will be described in detail.

The N Divider circuit is clocked by a pulse train derived from the input frequency (in this case the 20 MHz reference signal). The divider outputs 4 pulses for each sequence of clock pulses which add up to the N number. In other words, a pulse is output for each N/4 or N/4 + 1 clock pulses. If dividing the N number by 4 leaves no remainder, the number of clock pulses between output pulses is determined solely by N/4. If there is a remainder, the number of clock pulses between outputs is determined by N/4 and N/4 + 1 where N/4 + 1 replaces N/4 once for each unit in the remainder. For example, if N = 16, then N/4 = 16/4 = 4 with a remainder R = 0. An output pulse occurs for each 4 clock pulses. If N = 19, then N/4 = 19/4 = 4 with R = 3. An output pulse occurs once with a spacing of 4 clock pulses and three times with a spacing of 5 clock pulses.

a. Counting Operation and Control. Refer to the schematic block diagram and the following figure and table entitled Divider Operation, and consider the example of N = 16. At the beginning of a divide sequence (clock 1), the 4 most significant bits (MSB) of

the N number (0100) are loaded into U6 (a programmable counter). Clock 2 subtracts 4 (0001) from the previous total leaving (0011); Clock 3 subtracts 4 more and the 0010 output enables the End of Count Decoder. At Clock 4, both the Count Control (U4B) and Output Flip-Flop (U4A) are set. The Count Control outputs (1) inhibit the End of Count Decoder, (2) cause U6 to enter its load mode, and (3) clock the Divider Flip-Flops (U10). The Output Flip-Flop outputs a high to the Phase/Frequency Detector. Clock 5 resets the flip-flops and loads the counter. This series of events repeats itself 3 more times for the N = 16 sequence.

b. Increment Decoder Operation. The Increment Decoder and Divider (U10) (divide-by-four) circuits come into play if the N number cannot be divided by 4 evenly. The 2 least significant bits (LSB) of the N number (N2 and N1) control the output of the Increment Decoder. The divide-by-four circuit provides a sequence of four sequential states, that are input to the Increment Decoder. Each state coincides with one of the four count down sequences whose length is characterized by N/4 or N/4 + 1. Refer to the table entitled Increment Decoder Operation. Note that for the N = 16 sequence, N2 = N1 = 0. As explained in Counting Operation and Control, the Increment Decoder Output Sequence (TP3) never leaves the low state and the count down sequences are N/4. For N = 19 (N2 = N1 = 1) the first output is low with the remaining three high. This means that the first pulse occurs after N/4 clock pulses and the other three occur after N/4 + 1 pulses. During the final three count down sequences, the high at the Increment Decoder Output inhibits U9B allowing the counter to count down to 0001 (rather than 0010) before the End of Count Decoder is enabled through U9A. This allows the extra count to occur. The rest of the sequence occurs as indicated in the previous section. See also the table and figure entitled Divider Operation for N = 19.

With the N input equal to or greater than 16, the N5 or N6 inputs are high and the Divide-by-1 or 2 Decoder is enabled. Thus the Output Flip-Flop follows the Count Control Flip-Flop and each End of Count pulse is passed directly to the output. If N < 16, then the Divide-by-1 or 2 Decoder is enabled and therefore passes only every other End of Count pulse to set the Output Flip-Flop. (Refer to the table entitled Divider Operation and the figure entitled Divider Clock Pulses versus Output Pulses). This circuit reduces the apparent gain of the Phase/Frequency Detector. This keeps the Delta F_{VCO}/Delta V sensitivity of the VCO in a specific portion of its tuning curve thereby keeping the M/N loop bandwidth constant. Note that the N5 and N6 inputs are also connected to the M-Divider in the same manner as in the N Divider. Note also that the frequency of the M and N Divider Outputs is halved for N < 16.

Mixer D

Q3 is an amplifier that drives the LO port of mixer U24. It supplies about +5 dBm over the 355 to 395 MHz range. The output of the mixer is the difference between 400 MHz and the M/N VCO frequency which gives an IF frequency between 5 and 45 MHz. The IF level is about -17 dBm.

IF Amplifier E

The 60 MHz low-pass filter rejects unwanted mixing products from the mixer. Q4 and U18B amplify and limit the IF signal and give it the proper levels to run the following ECL circuitry. These levels are approximately -0.9 volts and -1.7 volts.

Phase/Frequency Detector F

The outputs of the M and N dividers are compared in U1. When they are in phase, the outputs of U1 are narrow, coincident pulses. For unlock conditions, the outputs pulses are of varying widths.

Preamplifier G

Q1 and Q2 are a low-noise differential pair preamplifier. Their outputs are combined in the integrating amplifier of A33.

Phase Lock Indicator H

U2A and U2B are voltage comparators which compare each tune line to the average plus a small offset provided by R29. If the loop unlocks, one of the preamplifier outputs is higher than the comparison voltage, and the phase lock indicator goes high, indicating the unlock condition.

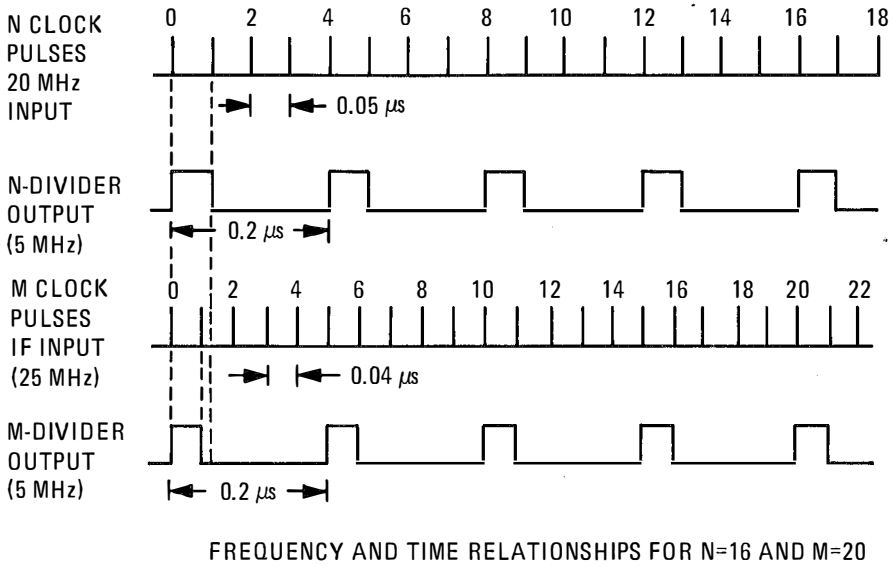


Figure 8B-7. Divider Clock Pulses Versus Output Pulses Frequency and Time Relationship

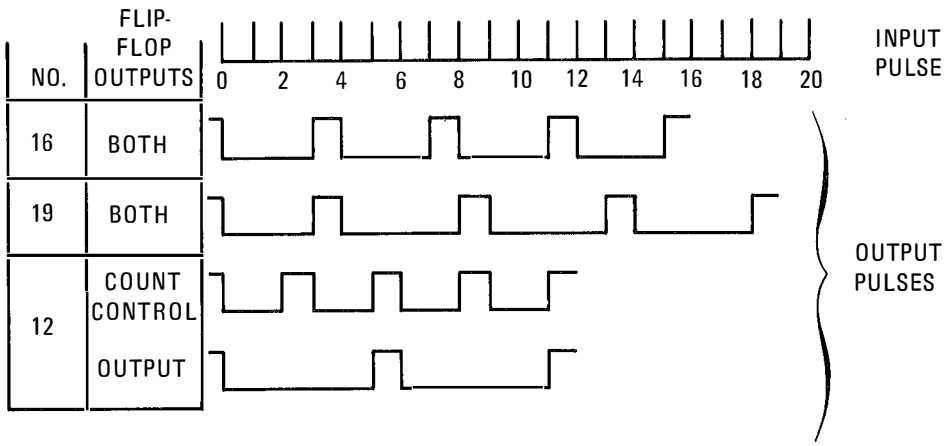


Figure 8B-8. Divider Operation

Table 8B-5. Divider Operations

N	Input Clock Pulses	Operation	N number in Counter (4 MSB)	End of Count Decoder	Flip-Flop	
					Count Control	Output
16	0, 4, 8, 12	Load Counter	0100	Inactive	Reset	Reset
	1, 5, 9, 13	Minus 4	0011	Inactive	Reset	Reset
	2, 6, 10, 14	Minus 4	0010	Active	Reset	Reset
	3, 7, 11, 15	Minus 4	0001	Inactive	Set	Set
19	0, 4, 9, 14	Load Counter	0100	Inactive	Reset	Reset
	1, 5, 10, 15	Minus 4	0011	Inactive	Reset	Reset
	2, 6, 11, 16	Minus 4	0010	Inactive[1]	Reset	Reset
	3, 7, 12, 17	Minus 4	0001	Active[2]	Reset[3]	Reset[3]
	8, 13, 18	Minus 4	0000	Inactive	Set	Set
12	0, 3, 6, 9	Load Counter	0011	Inactive	Reset	Reset
	1, 4, 7, 10	Minus 4	0010	Active	Reset	Reset
	2, 5, 8, 11	Minus 4	0001	Inactive	Set	Set[4]

[1] Active for step 3 only
[2] Inactive for step 4 only
[3] Set for step 4 only
[4] The Output Flip-Flop is set only every other time the counter control Flip-Flop is set for N<16.

Table 8B-6. Increment Decoder Operation

Increment Decoder Control Inputs		Increment Decoder Output Sequence*			
N2	**N1**	**1**	**2**	**3**	**4**
L(0)	L(0)	L	L	L	L
L(0)	H(1)	L	L	H	L
H(1)	L(0)	L	H	L	H
H(1)	H(1)	L	H	H	H

*The Sequence of four states is controlled by a modified ring counter made up of the two flip-flops contained in U10. The count sequence of U10 may be checked by verifying that the active high outputs of the flip-flops follow the sequence LL, HH, LH, and HL (U10A pin 2, and U10B pin 15, respectively).

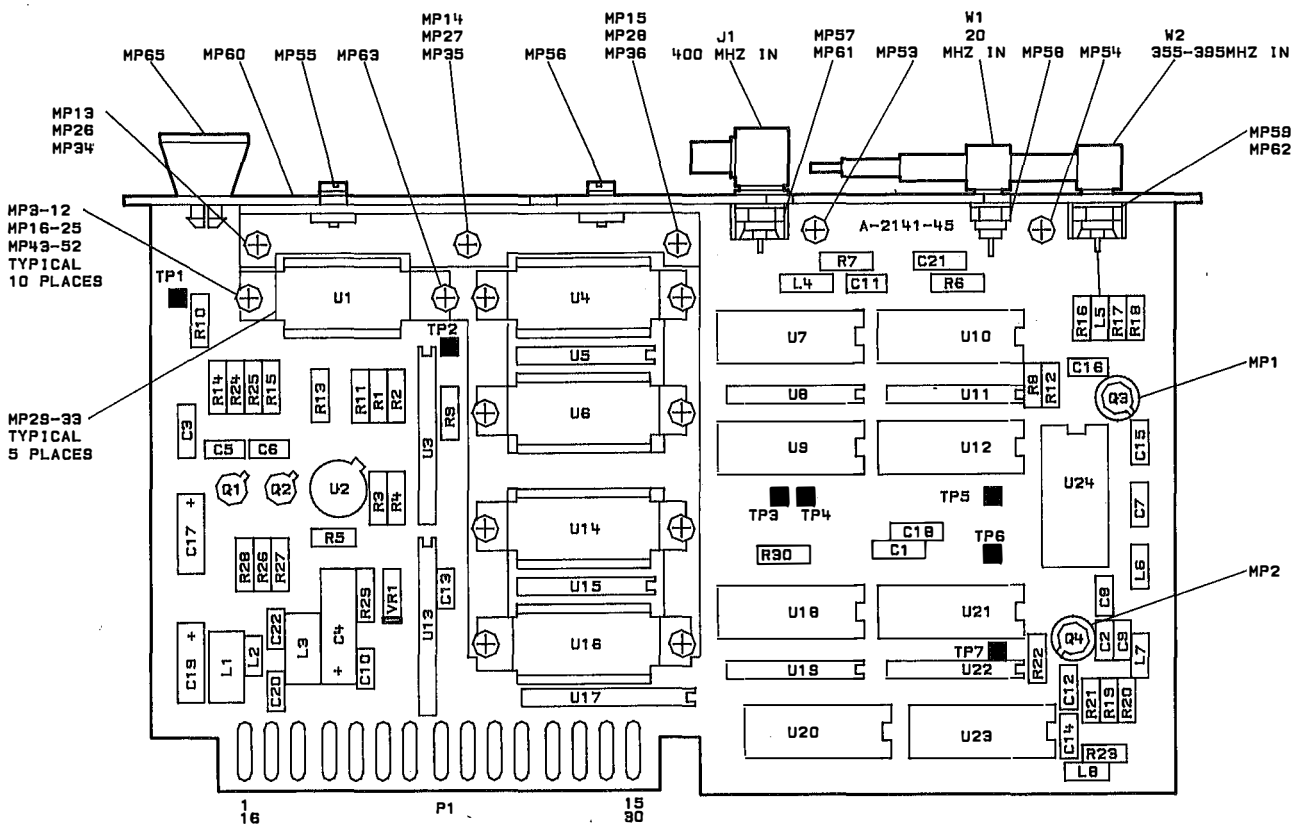


Figure 8B-9. A31 M/N Phase Detector, Component Location Diagram

A31 M/N Phase Detector Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 16	−10V −10V	−10V −10V	XA34P2-8, 9 XA34P2-8, 9	* *
2 17	+20V +20V	+20V +20V	XA34P2-2, 3 XA34P2-2, 3	* *
3 18	−5.2V −5.2V	−5.2V −5.2V	XA34P2-12, 13 XA34P2-12, 13	* *
4 19	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	* *
5 20	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	* *
6 21	VCO TUNE (−) VCO TUNE (+)		G G	* *
7 22	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	* *
8 23	N1 N2	TTL TTL	XA34P1-15 XA34P1-14	A A
9 24	N5 N6	TTL TTL	XA34P1-11 XA34P1-10	A A
10 25	N3 N4	TTL TTL	XA34P1-13 XA34P1-12	A A
11 26	GND HULM	0V TTL (HIGH TRUE)	INSTRUMENT GROUND H	* XA34P1-8
12 27	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	* *
13 28	M1 M2	TTL (HIGH TRUE) TTL (HIGH TRUE)	XA34P1-5 XA34P1-6	A A
14 29	M3 M4	TTL (HIGH TRUE) TTL (HIGH TRUE)	XA34P1-3 XA34P1-4	A A
15 30	M5 LMNE	TTL (HIGH TRUE) TTL (LOW TRUE)	XA34P1-1 XA34P1-2	A NOT USED

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A34 Reference Loop — M/N Motherboard Schematic Diagram for a complete representation of signal sources and destinations.

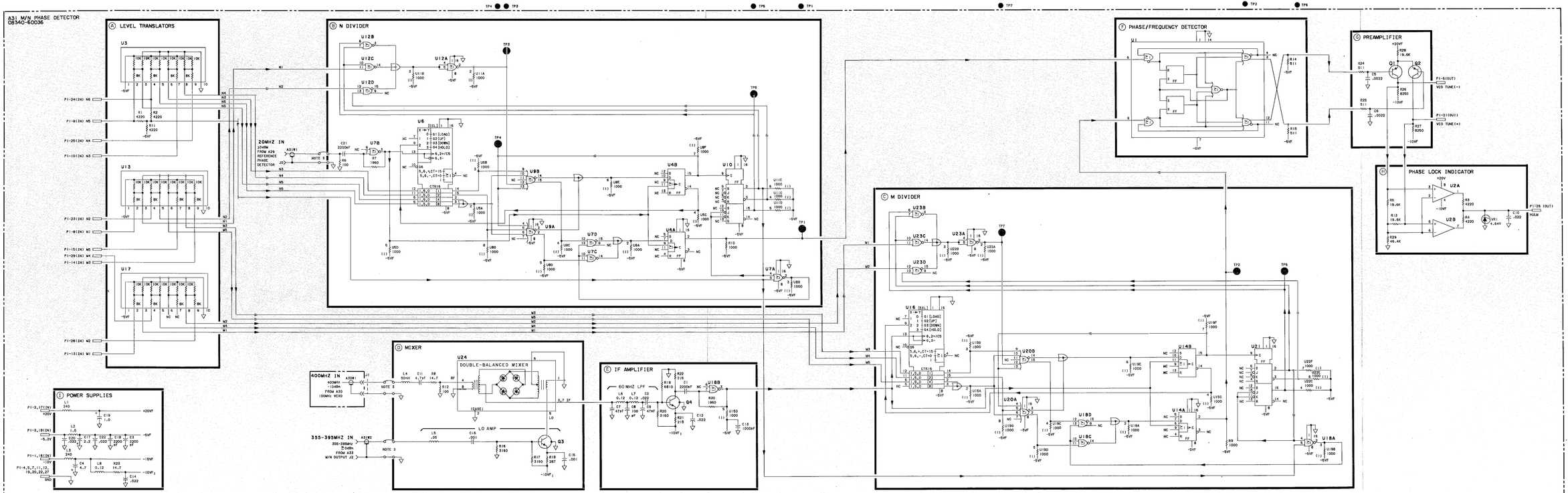


Figure 8B-10. A31 M/N Phase Detector, Schematic Diagram

A32 M/N VOLTAGE-CONTROLLED OSCILLATOR

INTRODUCTION

The M/N VCO (voltage-controlled oscillator) is a varactor-tuned cavity oscillator. It consists of a fore-shortened coaxial cavity resonator, a transistor circuit, and both a mechanical and an electrical tuning mechanism. Refer to Figure 8B-13, A32 M/N VCO and A33 M/N Output Assembly, Schematic Diagram.

A32 M/N VOLTAGE-CONTROLLED OSCILLATOR CIRCUIT DESCRIPTION

A32A2 Voltage-Controlled Oscillator A

The emitter of oscillator transistor, Q2, exhibits negative resistance because of the base inductance, L3, which consists of a fixed length of wire surrounded by air. The function of C8 and R9, together with L3, is to match the (reflective) emitter of Q2 to the cavity resonator. C2 provides a dc block required because the transistor is physically connected to the cavity center post (inductive coupling) that is at DC ground potential. R1, R4, R6, and R8 establish the dc bias for Q2. C3, C5, and C7 are bypass capacitors that also filter power supply noise.

The frequency of the oscillator can be tuned mechanically by adjusting C1, which is a tuning screw that capacitively loads the cavity center post. This is used to adjust the frequency to within the electrical tuning range. The frequency is adjusted electrically by using reverse biased varactor diodes, CR1 and CR2. The reverse bias to the diodes is the TUNE voltage from A33 M/N Output Board. The actual electrical tuning network components are physically located inside the resonator housing. Chip capacitors C2 and C3 are soldered onto the cavity center post. The anodes of varactor diodes CR1 and CR2 are soldered to C2 and C3, respectively, and their cathodes are soldered together to a post contacting the outer wall of the cavity. The result is that the combinations of CR1/C2 and CR2/C3 provide capacitive loading to the cavity resonator at the frequency of oscillaton. The (VCO) TUNe voltage is brought to the varactor diodes through inductors L1 and L2, which are also soldered to C2 and C3, respectively, and to a post that is electrically insulated from the outer wall of the cavity housing and is soldered to the A32A1 PC board.

The output of the VCO is taken directly from the cavity resonator through C5, a capacitively coupled E-field probe. The output power level is adjusted by varying the length of the probe. This signal is applied to the Buffer Amplifier, Block **B**.

R13 and C11 are part of the feedback network that determines the frequency response of the M/N Phase Locked Loop. (See also the M/N Loop Frequency Response section in the A31 M/N Phase Detector circuit description.)

A32A1 Buffer Amplifier B

The Buffer Amplifier provides both isolation and gain for the VCO output signal. L1 provides an impedance match to the cavity output for the base of Q1, the amplifier transistor. R3, R5, R7, R10, and R11 provide the dc bias for Q1. R3 provides negative feedback for the amplifier, and R2 and L2 provide the output impedance. The Buffer Amplifier provides at least 0 dBm output over the 355 to 395 MHz range of the VCO.

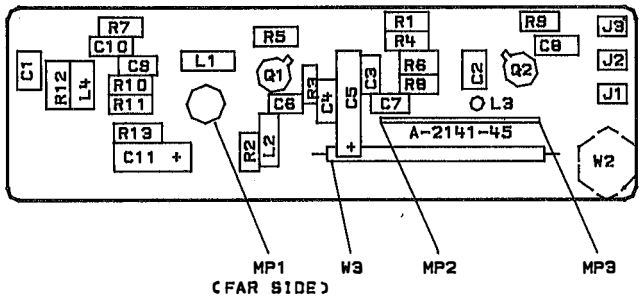


Figure 8B-11. A32 M/N VCO, Component Location Diagram

A33 M/N OUTPUT

INTRODUCTION

The A33 M/N Output board amplifies the output of the A32A2 M/N VCO in two different paths. One path contains amplification and buffering to drive the mixer in the A31 M/N Phase Detector. The other path drives a divide-by-two IC, and the output of the IC, after further amplification, goes to A48 YO Loop Sampler.

Also included on the A33 assembly is the integrating loop amplifier which generates the tuning voltage for the M/N VCO. Refer to Figure 8B-13, A32 M/N VCO and A33 M/N Output Assembly, Schematic Diagram.

A33 M/N OUTPUT CIRCUIT DESCRIPTION

Loop Amplifier A

U1 is connected as a differential-input integrating amplifier. The inputs, VCO TUNE(+) AND VCO TUNE(-), are from the A31 M/N Phase Detector. The single-ended output signal in the range of -5 to -35 volts tunes the A32A2 M/N VCO. C13 and C14 are the integrating capacitors and, with R14-17, establish the frequency response of the integrator. (See also the M/N Loop Frequency Response section in the A31 M/N Phase Detector circuit description.) C12 and C15 are feed-forward compensation capacitors for U1.

The network consisting of VR1, VR2, CR3, and CR4 function to speed up the charging-time response of the output load of U1 whenever the output voltage is changing very rapidly. It does this by bypassing R34 whenever the voltage drop across it reaches approximately 5.6 Vdc (corresponding to an output current of 1.8 mA), thus allowing the circuit to charge with a faster time constant.

At the output of U1, a 200 kHz low-pass filter provides further rejection of the sampling frequency noise (20 MHz divided by N) from the Phase/Frequency Detector (A31 M/N Phase Detector board, Block **F**). The filter has an insignificant effect on the M/N Loop frequency response within the loop bandwidth.

LO Output Amplifier B

The LO Output Amplifier functions as an isolation amplifier. Its forward gain is such that the output signal level is $\geq$ 0dBm, and the reverse isolation is > 60dB. Q5 is a common-emmiter amplifier

followed by a resistive pad (R8, Rl2, and Rl3). Q2 is a common-base buffer amplifier which has a tuned output match (L2, Ll0, and C3). Ql is another common emitter amplifier that is followed by a 400 MHz low-pass filter for rejection of harmonics. The output, 355-395 MHz OUT, is routed to the A31 M/N Phase Detector board.

LO Amplifier C

The LO Amplifier is used to amplify the coupled-off portion of the A32A2 M/N VCO output signal to increase its level back up to 0 dBm. Q6 is a common-emitter amplifier with gain, and Q7 is an emitter-follower amplifier to provide a low impedance output to drive Divide-By-2, U2, Block **D**. R24 and R25 set the proper dc bias voltage for the ECL divider, U2, so that it can be driven by the 0 dBm signal.

Divide-By-2 D

U2 is an EECL (HP ECL) divider used to generate the M/N output signal which is at one-half the frequency of the M/N VCO. LMNE (Low = M/N Enable) is an M/N Loop control line that could be used to turn on and off the divider through the operation of the TTL-ECL Level Shifter. In the 8340A, the LMNE line is hard wired to ground so that LMNE ia always low. (This board is also used in the M/N loop of the 8566 Signal Analyzer where the LMNE feature is implemented.)

M/N Output Amplifier E

The M/N Output Amplifier buffers and amplifies the output of the Divide-By-2 (Block **D**). Q3 is an emitter-follower buffer amplifier, and Q4 is a common-emitter amplifier. The output of Q4 passes through a 250 MHz low-pass filter to provide the M/N OUT signal which is input to the A48 YO Loop Sampler.

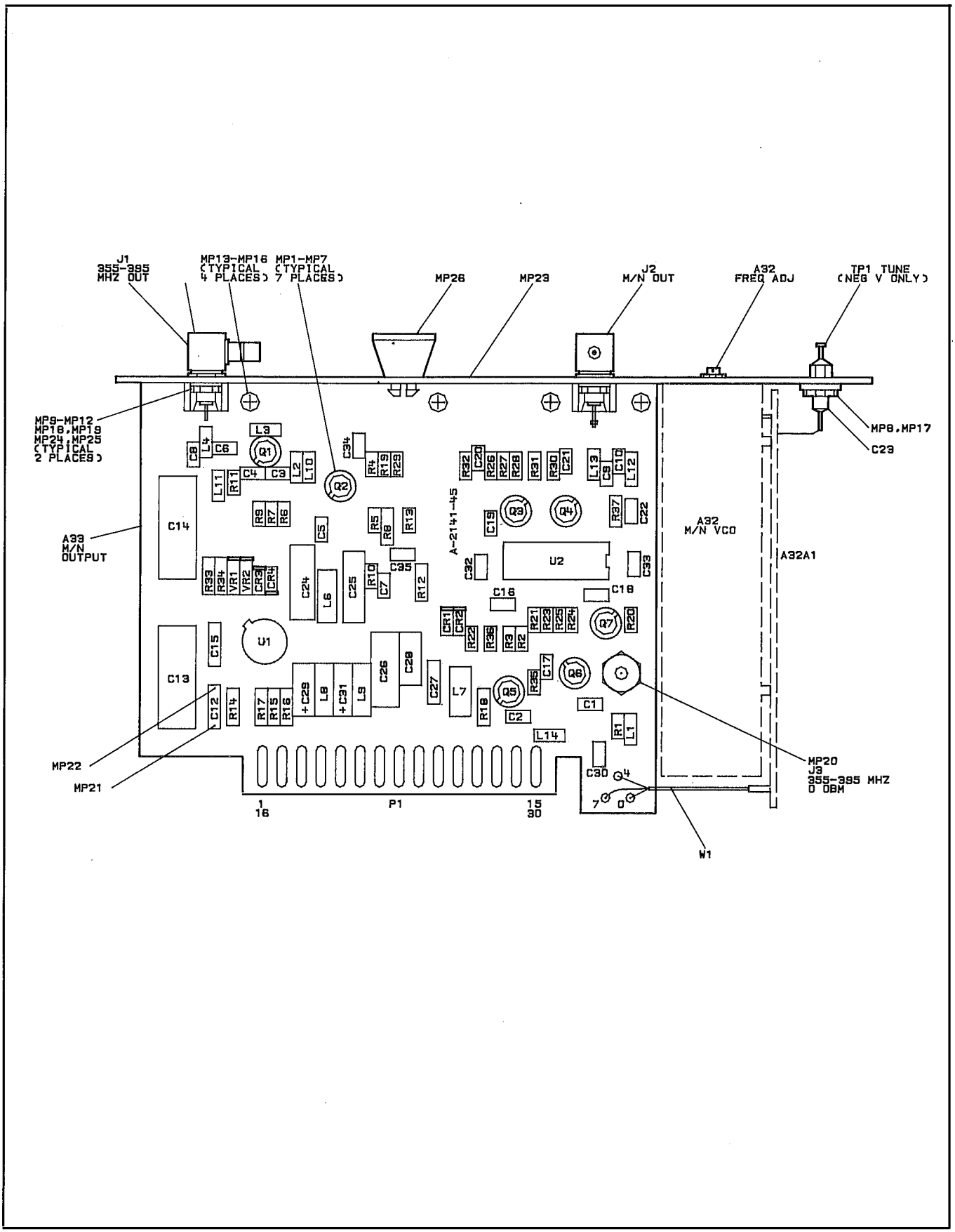


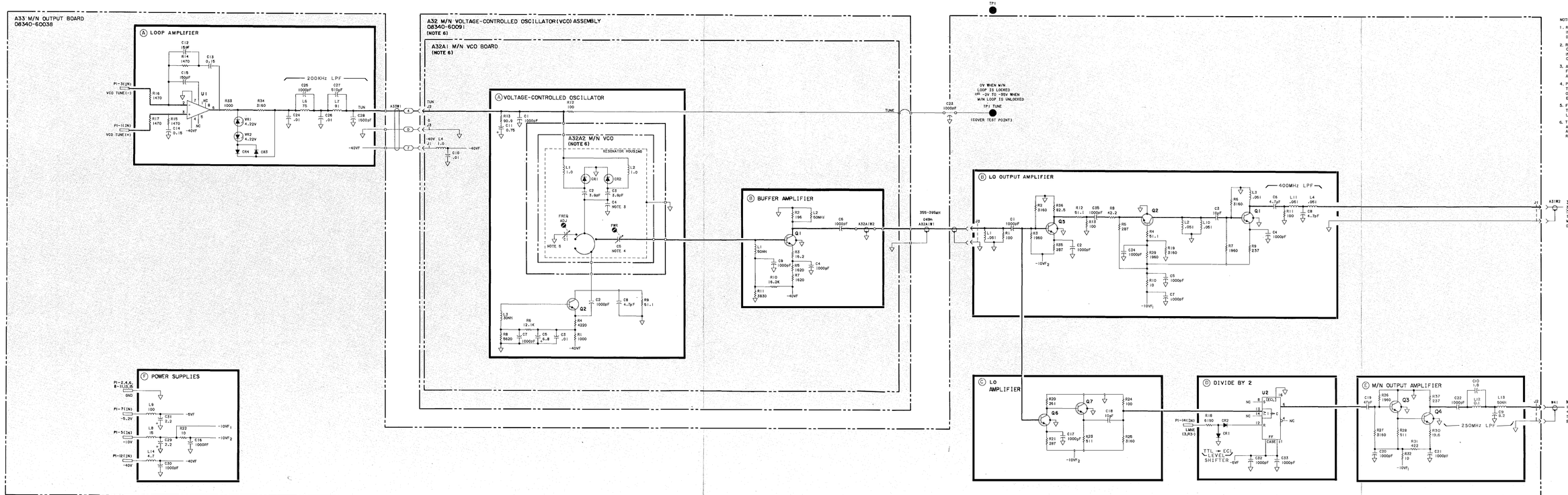
Figure 8B-12. A33 M/N Output Assembly, Component Location Diagram

A33 M/N Output Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1	VCO TUNE (+)		XA31P1-21	A
2	GND	0V	INSTRUMENT GROUND	*F
3	VCO TUNE (−)		XA31P1-6	A
4	GND	0V	INSTRUMENT GROUND	*F
5	−10V	−10V	XA34P2-8, 9	*F
6	GND	0V	INSTRUMENT GROUND	*F
7	−5.2V	−5.2V	XA34P2-12, 13	*F
8	GND	0V	INSTRUMENT GROUND	*F
9	GND	0V	INSTRUMENT GROUND	*F
10	GND	0V	INSTRUMENT GROUND	*F
11	GND	0V	XA34P2-6, 7	*F
12	−40V	−40V	INSTRUMENT GROUND	*F
13	GND	0V		*F
14	LMNE	TTL (LOW TRUE)	INSTRUMENT GROUND	D
15	GND	0V		*F

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A34 Reference Loop — M/N Motherboard Schematic Diagram for a complete representation of signal sources and destinations.

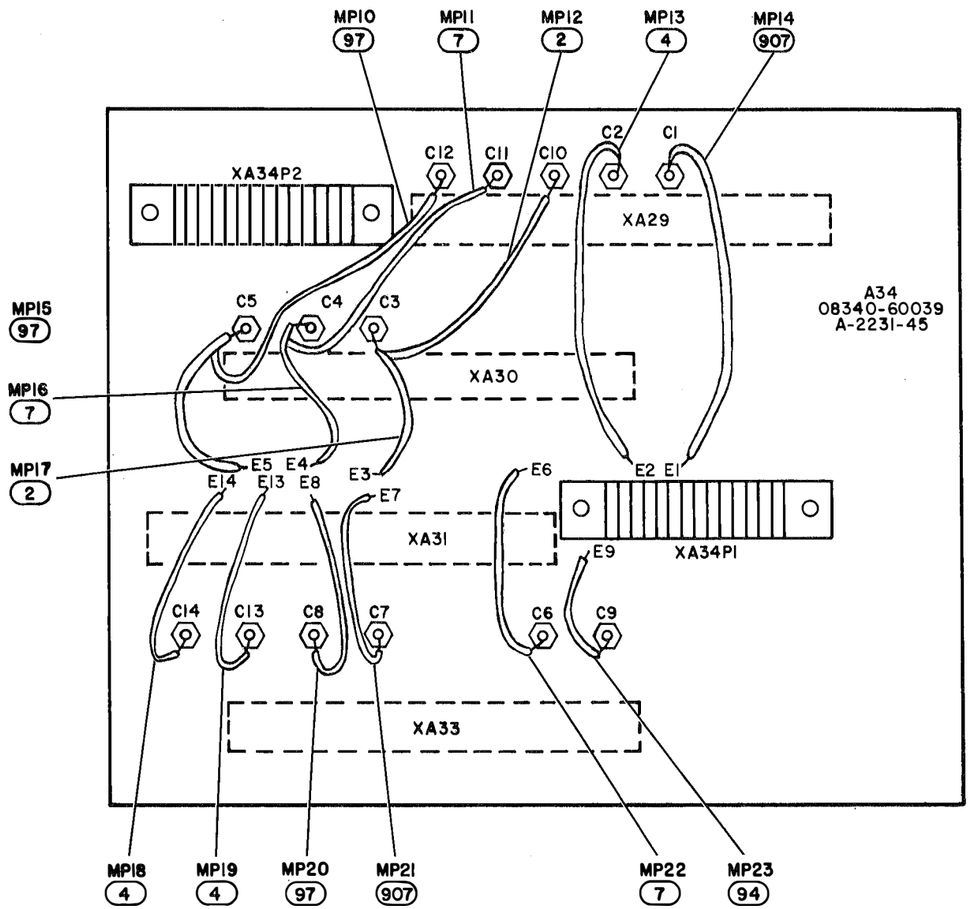


NOTES:

1. REFER TO THE SERVICE SECTION INTRODUCTION FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. A32AIC4 IS AN AIR DIELECTRIC CAPACITOR FORMED BY THE RESONATOR HOUSING AND THE RESONATOR CENTER CONDUCTOR.
4. PWR ADJUSTMENT. THIS IS AN ADJUSTABLE PROBE MOUNTED ON THE A32A1 M/N VCO PC BOARD AND EXTENDING INTO THE RESONATOR HOUSING.
5. FREQ ADJ. THIS IS AN ADJUSTMENT SCREW LOCATED ON THE A33 BOARD COVER.
6. THE A32 ASSEMBLY INCLUDES A32A1 AND A32A2. INDIVIDUAL COMPONENTS IN THE A32A2 ASSEMBLY ARE NOT SEPARATELY REPLACEABLE.

Figure 8B-13. A32 M/N VCO and A33 M/N Output Assembly, Schematic Diagram

A34 M/N – REFERENCE MOTHERBOARD
(Bottom View)



A34 M/N – REFERENCE MOTHERBOARD
(Top View)

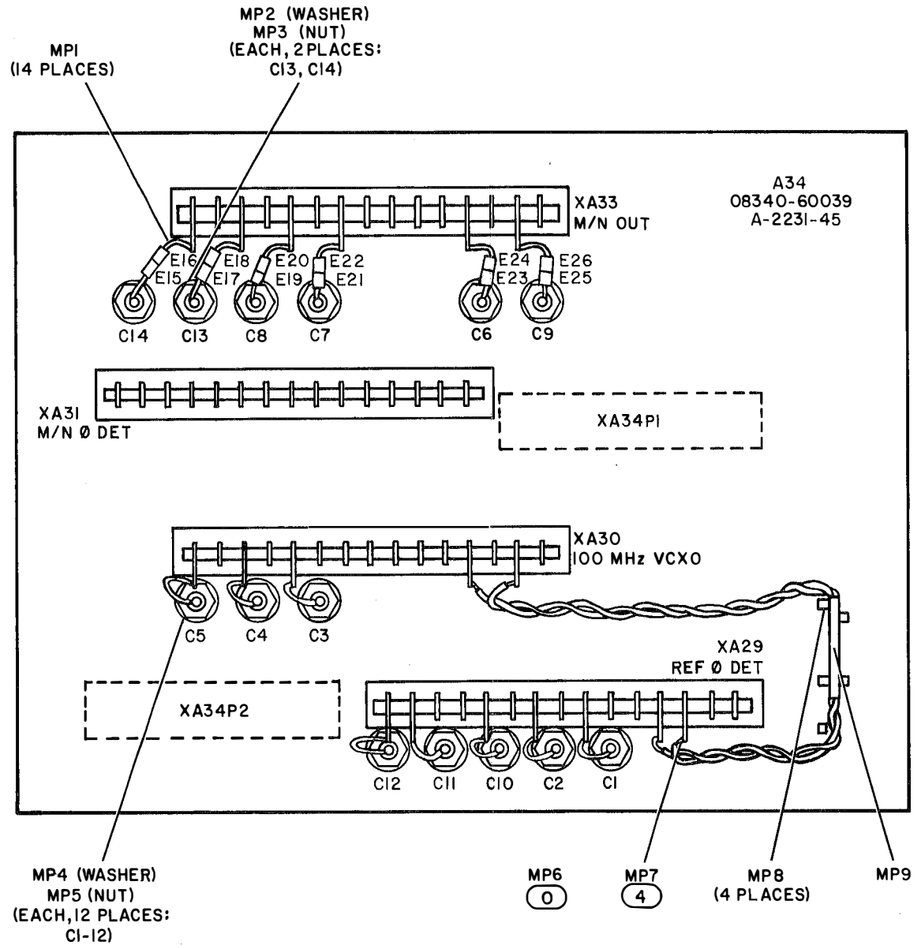


Figure 8B-14. A34 Reference Loop – M/N Loop Motherboard Component Location Diagram

A34 Reference — M/N Motherboard P1 Pin I/O

A34

Pin	Mnemonic	Levels	Source	Destination
1	M5	TTL (HIGH TRUE)	XA59P1-31	XA31P1-15
2	LMNE	TTL (LOW TRUE)	XA59P1-86	*
3	M3	TTL (HIGH TRUE)	XA59P1-32	XA31P1-14
4	M4	TTL (HIGH TRUE)	XA59P1-87	XA31P1-29
5	M1	TTL (HIGH TRUE)	XA59P1-33	XA31P1-13
6	M2	TTL (HIGH TRUE)	XA59P1-88	XA31P1-28
7				
8	HULM	TTL (HIGH TRUE)	XA31P1-26	XA31P1-26
9				
10	N6	TTL	XA59P1-101	XA31P1-24
11	N5	TTL	XA59P1-46	XA31P1-9
12	N4	TTL	XA59P1-102	XA31P1-25
13	N3	TTL	XA59P1-47	XA31P1-10
14	N2	TTL	XA59P1-103	XA31P1-23
15	N1	TTL	XA59P1-48	XA31P1-8

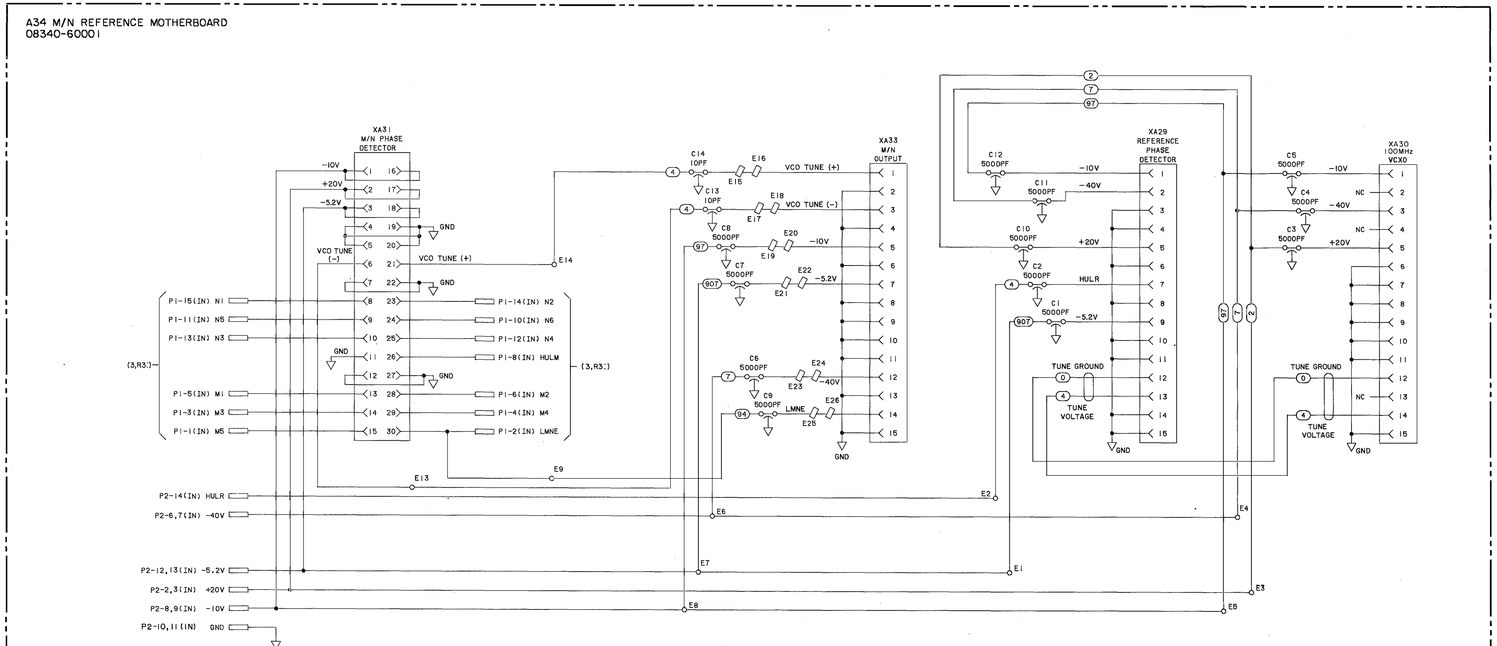
A34 Reference — M/N Motherboard P2 Pin I/O

A34

Pin	Mnemonic	Levels	Source	Destination
1				
2	+20V	+20V	XA52P1-16, 40	*
3	+20V	+20V	XA52P1-16, 40	*
4	+5.2V	+5.2V	XA52P1-17, 18, 41, 42	*
5	+5.2V	+5.2V	XA52P1-17, 18, 41, 42	*
6	−40V	−40V	XA53P1-11, 30	*
7	−40V	−40V	XA53P1-11, 30	*
8	−10V	−10V	XA53P1-12, 13, 31, 32	*
9	−10V	−10V	XA53P1-12, 13, 31, 32	*
10	GND	0V	A62 STAR GND	*
11	GND	0V	A62 STAR GND	*
12	−5.2V	−5.2V	XA53P1-18, 36	*
13	−5.2V	−5.2V	XA53P1-18, 36	*
14	HULR	TTL (HIGH TRUE)	XA29P1-7	XA29P1-7
15				

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A34 Reference Loop — M/N Motherboard Schematic Diagram for a complete representation of signal sources and destinations.



NOTES:

1. REFER TO THE SERVICE SECTION INTRODUCTION FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES SHOWN ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.

Figure 8B-15. A34 Reference Loop – M/N Loop Motherboard, Schematic Diagram

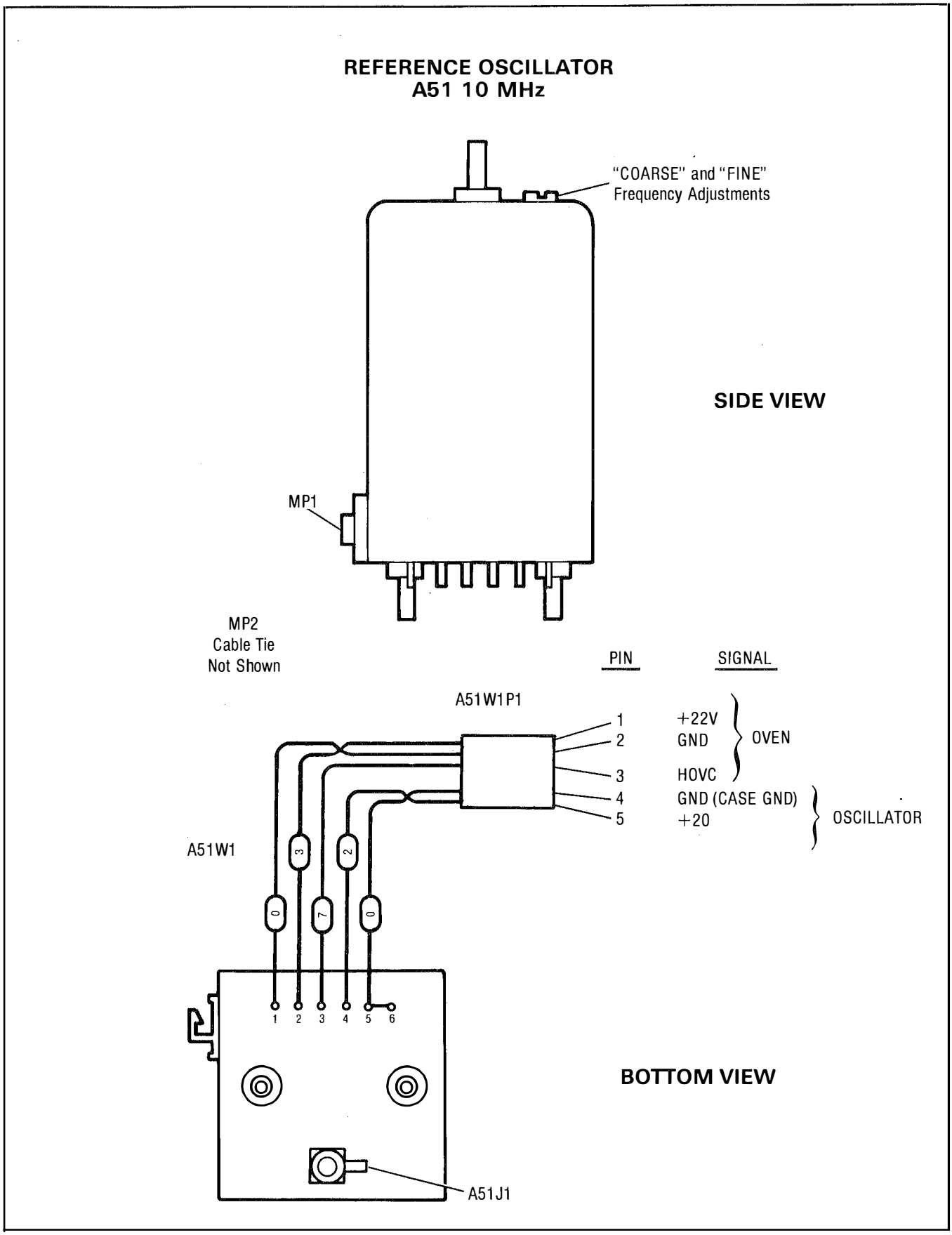


Figure 8B-16. A51 10 MHz Reference Oscillator, Component Location Diagram

A62J3 to A51WIPI Pin I/O

A62J3

Pin	Mnemonic	A51W1P1	Levels
1	+20V REF OSC	PIN 1	0V/+20V
2	GND	PIN 2	0V
3	HOVC	PIN 3	+3V/OVEN WARM
4	GND	PIN 4	0V
5	+22V	PIN 5	+22V

Note: Refer to M/N and Reference Loops Troubleshooting Block Diagram and A62 Motherboard Wiring List for signal source and destination information.

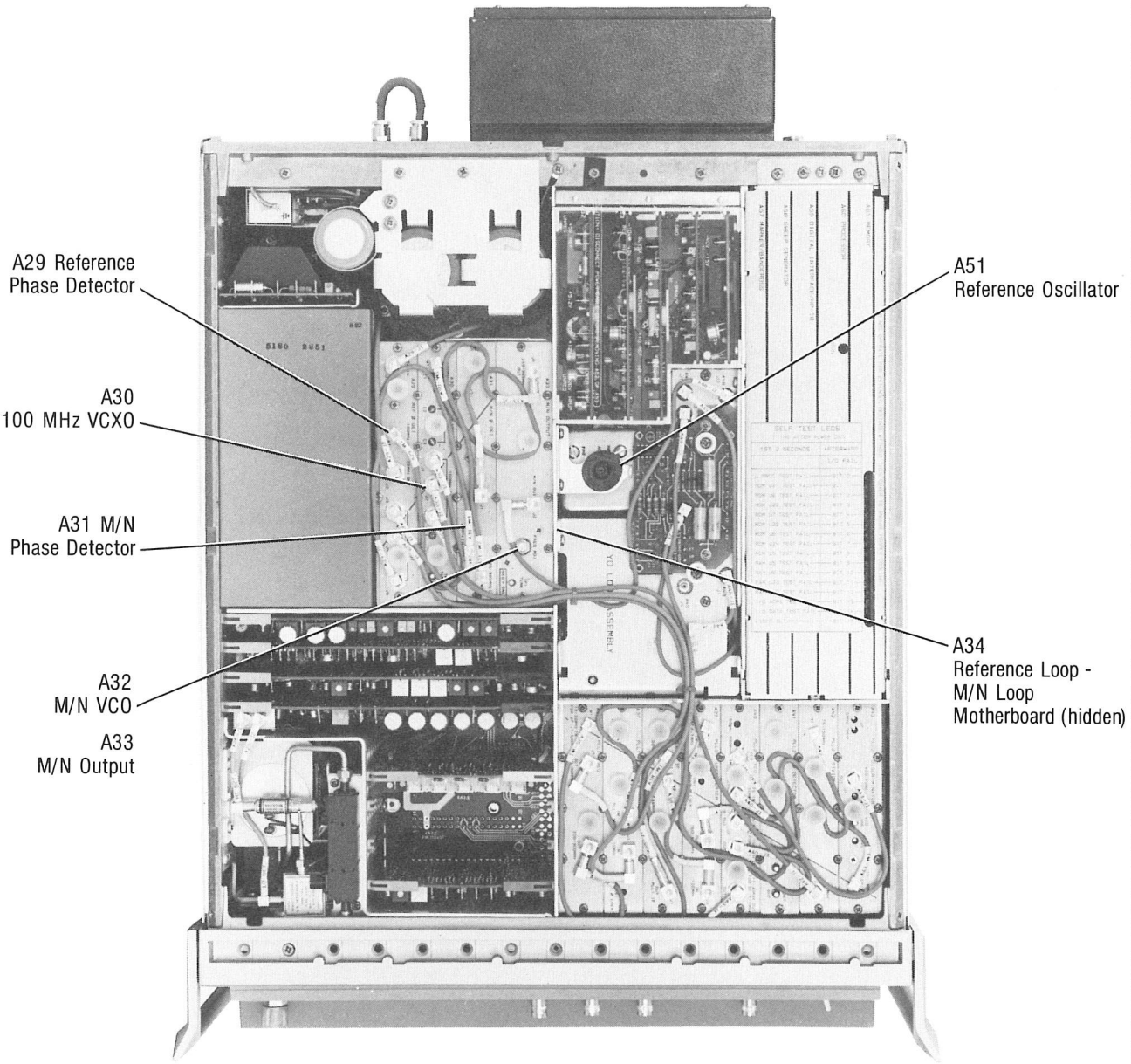
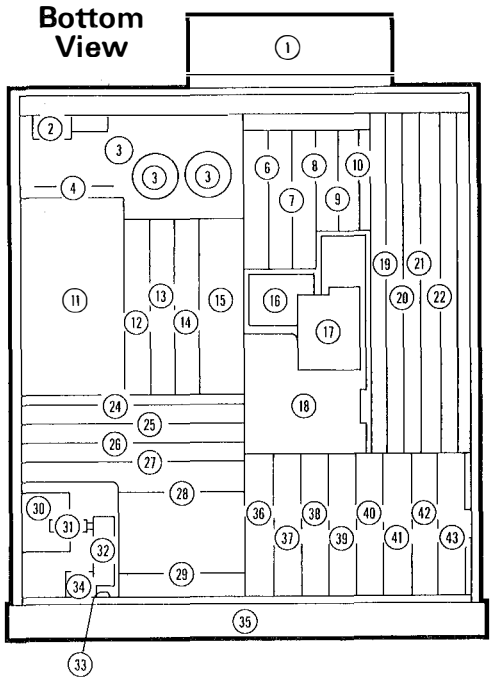
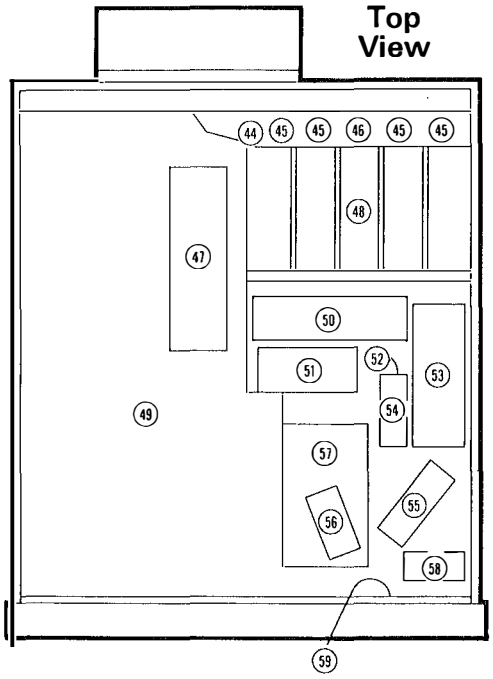


Figure 8B-17. Reference Loop - M/N Loop Major Assemblies Location

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 3						Volume 4	
			Ref.-M/N Loops	20-30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	33					•			
A2	Display Driver	33					•			
A3	Display Processor	33					•			
A4	Not Assigned	-								
A5	Keyboard	35					•			
A6	Keyboard Interface	35					•			
A7	Lower Keyboard	35					•			
A8	3.7 GHz Oscillator	57						•		
A9	Band 0 Pulse Modulator	56						•		
A10	Directional Coupler	32						•		
A11	Band 1-4 Detector	31						•		
A12	Band 0 Splitter/Detector	34						•		
A13	SYTM (Switched YIG Tuned Multiplier)	30						•		
A14	Band 1-4 Power Amplifier	53						•		
A15	Band 0 Low Pass Filter	52						•		
A16	Band 1-4 Modulator/Splitter	51						•		
A17	Band 0 Mixer	54						•		
A18	Band 0 Power Amplifier	55						•		
		60						•		
A19	Capacitor Assembly	48								•
A20	RF Section Filter	50						•		
A21	Pulse Modulator Driver	29						•		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						•		
A25	ALC Detector	27						•		
A26	Linear Modulator	26						•		
A27	Level Control	25						•		
A28	SYTM Driver	24						•		
A29	Reference Phase Detector	12	•							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	•							
A31	M/N Phase Detector	14	•							
A32	M/N VCO (Voltage Controlled Osc.)	15	•							
A33	M/N Output	15	•							
A34	Reference-M/N Motherboard	5	•							
A35	Rectifier	4								•
A36	PLL1 VCO (Voltage Controlled Osc.)	36		•						
A37	PLL1 Divider	37		•						
A38	PLL1 IF	38		•						
A39	PLL3 Upconverter	39		•						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		•						
A41	PLL2 Phase Detector	41		•						
A42	PLL2 Divider	42		•						
A43	PLL2 Discriminator	43		•						
A44	YIG Oscillator (YO)	18			•					
A45	Directional Coupler	18			•					
A46	7 GHz Low Pass Filter	18			•					
A47	Sense Resistor Assembly (YO circuit)	47			•					
	(SYTM circuit)	47						•		
A48	YO Loop Sampler	18			•					
A49	YO Loop Phase/Detector	18			•					
A50	YO Loop Interconnect	17			•					
A51	Reference Oscillator	16	•							
A52	Positive Regulator	6								•
A53	Negative Regulator	7								•
A54	YO Pretune/Delay Compensation	8			•					
A55	YO Driver	9			•					
A56	−15V Regulator	10								•
A57	Marker/Bandcross	19					•			
A58	Sweep Generator	20			•					
A59	Digital Interface	21					•			
A60	Processor	22					•			
A61	Not Assigned	23					•			
A62	Motherboard	49				•				
A63	90 dB RF Attenuator	59						•		
AT1	Peripheral Mode Isolator	58						•		
AT2	15 dB Attenuator	18			•					
B1	Fan Assembly	1								•
A62C1-3	Power Supply Filter Capacitors	3								•
FL1	AC Line Module	2								•
A62Q1-4	Power Supply Regulating Transistors	45								•
A62S1	Power Supply Thermal Switch	44								•
T1	Power Supply Transformer	11								•
A62U1	Power Supply Regulator	46								•

20-30 LOOPS C

20-30 LOOP
INTRODUCTION

This functional group contains the following information:

- Overall description of the 20-30 Loop.
- Simplified Block Diagram.
- Overall descriptions of individual PLL2, PLL3, and PLL1 Loops.
- Troubleshooting Block Diagram.
- Circuit Descriptions, Component Location Diagrams, Pin I/O Tables, and Schematic Diagrams for all 20-30 Loop Assemblies.

LIST OF ASSEMBLIES

PLL2 Assemblies

- A40 PLL2 VCO (Voltage Controlled Osc.)
- A41 PLL2 Phase Detector
- A42 PLL2 Divider
- A43 PLL2 Discriminator

PLL3 Assembly

- A39 PLL3 Upconverter

PLL1 Assemblies

- A36 PLL1 VCO (Voltage Controlled Osc.)
- A37 PLL1 Divider
- A38 PLL1 IF

20-30 LOOP
OVERALL DESCRIPTION

INTRODUCTION

The 20-30 Loop consists of the following assemblies:

A36 PLL1 VCO
A37 PLL1 DIVIDER
A38 PLL1 IF
A39 PLL3 UP CONVERTER
A40 PLL2 VCO
A41 PLL2 PHASE DETECTOR
A42 PLL2 DIVIDER
A43 PLL2 DISCRIMINATOR

DESCRIPTION

The 20-30 Loop provides the 8340A with 1 Hz CW (YO) tuning resolution. In swept frequency modes the 20-30 Loop provides high resolution tuning in sweep widths from 100 Hz to 5 MHz.

In sweep widths less than 5 MHz, the YO Loop remains phase-locked during the sweep, and the 20-30 Loop is swept the desired amount. For sweep widths greater than 5 MHz, the 20-30 Loop remains fixed and the YO is swept (lock and roll sweep).

These assemblies form a frequency synthesizer with the following performance characteristics:

- Fixed frequency output range from 20 to 30 MHz
- Analog sweep widths between 100 Hz and 5 MHz
- CW frequency resolution as low as 1 Hz

The 20-30 Loop contains three phase locked loops that are used in three different configurations to achieve the required CW resolution and sweep range. The loops are referred to as PLL1, PLL2 and PLL3. PLL2 is always used in the 8340A, regardless of the instrument's mode of operation. PLL1 and PLL3 are arranged to be phase-locked to the output of PLL2, and can sweep while locked to PLL2.

NOTE:

Figure 8C-1, 20-30 Loop Simplified Block Diagram, illustrates the three configurations mentioned below.

CONFIGURATION 1

This configuration is used in YO sweep widths from 5 MHz to >100 kHz.

PLL2 phase-locks a 75 to 150 MHz VCO to a 10 MHz reference frequency derived from the Reference Loop. The PLL2 VCO is programmable in 5 kHz steps, and it can be swept a maximum of 25 MHz using a lock and roll analog sweep. To improve the linearity of this sweep, a very linear discriminator is used in a feedback loop around the VCO. This results in sweep accuracies that are mainly a function of discriminator linearity, and removes the effects of VCO tuning non-linearities. The sample-and-hold circuit for the PLL2 Loop has an extremely low amount of drift. A capacitor cannot hold the error voltage constant during a slow sweep, due to the amount of leakage that is present. Instead, the majority of the error voltage is stored in digital form so that it will remain stable during the sweep.

The output of the PLL2 VCO is divided-down through several stages of digital frequency dividers. By dividing the 75 to 150 MHz VCO by 5 an output is generated in the frequency range of 15 to 30 MHz. The VCO resolution is 5 kHz, so the divided output will have 1 kHz resolution. The VCO can be swept a maximum of 25 MHz, so the divided output will sweep up to 5 MHz sweep widths. This path is used directly as one of the three configurations of the 20-30 Loop. Notice that PLL1 and PLL3 are not used at all in this configuration.

CONFIGURATION 2 & 3

These configurations are used in sweep widths $\leq$ 100 kHz. For sweep widths below .1 MHz, configuration 1 provides insufficient resolution (1 kHz) to set the start frequency to closer than 0.5% of the sweep width. To provide for finer resolution, the output of the PLL2 VCO is divided by 25 (divided by 5 twice). The resultant signal has a 200 Hz resolution, is between 3 and 6 MHz, and can be swept with sweep widths up to 1 MHz. This PLL2 output is used in configuration 2. For sweep widths less than 5 kHz, configuration 2 will not provide sufficient resolution, so a third output (configuration 3) is provided. The PLL2 VCO is divided by 500 (divided by 5 twice, then divided by 20) and the output is used in configuration 3.

The two divided outputs of the PLL2 VCO (divided by 25, divided by 500) are used for configuration 2 and 3 to improve the resolution of PLL2. The frequency, however, is also reduced such that it is no longer in the 20 to 30 MHz range. PLL1 and PLL3

Loops are used to translate the high resolution, low frequency PLL2 output up to a 200 to 300 MHz range. Since a translation is a fixed offset in frequency, it will not change the resolution as does dividing or multiplying. After the frequency translation, the output of PLL1 is divided by 10 to reduce the frequency from 200-300 MHz to 20-30 MHz. This also increases the output resolution by a factor of 10.

PLL3 functions as a fixed 160 MHz frequency offset to the PLL2 output. PLL3 phase-locks a 160 to 166 MHz VCO to one of the divided down outputs of the PLL2 VCO, such that PLL3 VCO will be 160 MHz above the selected PLL2 output. PLL3 uses a reference signal from the 100 MHz VCXO reference to generate the 160 MHz offsetting frequency. As the PLL2 divided-down output changes frequency, the PLL3 output will also change frequency with the same resolution and sweep width, but at a higher operating frequency.

PLL1 functions as a programmable offset to the output of PLL3. Like PLL3, it will not effect the resolution since it is an offset. The selected PLL2 divided output is still determining the resolution and sweep width of the signal. PLL1 contains a 200 to 300 MHz VCO that will be locked such that its frequency will be exactly N1*10 MHz above the PLL3 output, where N1 is a number programmed between 3.60 and 13.97.

The output of the PLL1 VCO is divided by 10 to become the output of the 20-30 Loop for configuration 2 and 3. By dividing by 10, the PLL1 200-300 MHz VCO is reduced to the 20 to 30 MHz range and the PLL2 MHz resolution is increased by another factor of 10.

Refer to Figure 8C-7, 20-30 Loop Block Diagram, or Figure 8C-1, 20-30 Loop Simplified Block Diagram, for further information.

The three configurations are summarized in Table 8C-1.

Table 8C-1. 20-30 Loop Parameters

8340 SWEEP WIDTH (YO)	Loops Used: PLL1	PLL2	PLL3	PLL2 VCO divided by:	Divide by 10 (PLL1)	Total divide number	20-30 output resolution
5 MHz to >100 kHz	-	X	-	5	--	5	1 kHz
100 kHz to >5 kHz	X	X	X	25	10	250	20 Hz
5 kHz to 100 Hz and CW Mode	X	X	X	500	10	5000	1 Hz

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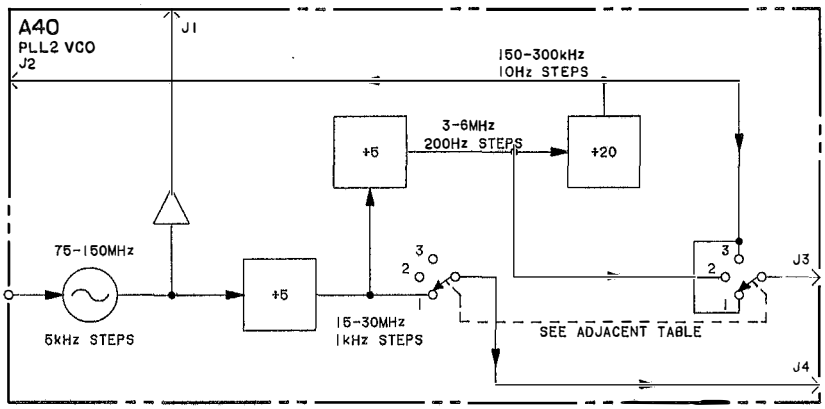

P/O Figure 8C-1. 20/30 Loop Simplified Block Diagram

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FOR ΔF ≤6MHz, BAND I (n X 1)

ΔF:	6MHz TO >.1MHz	100kHz TO >5kHz	5kHz TO 100kHz AND CW MODE
STEP SIZE: OUT OF 20-30MHz	1kHz	20Hz	1Hz
SWITCH POSITION: (CONFIGURATION)	1	2	3

WHERE n = HARMONIC MIXING NUMBER OF SYTM (1 TO 4)

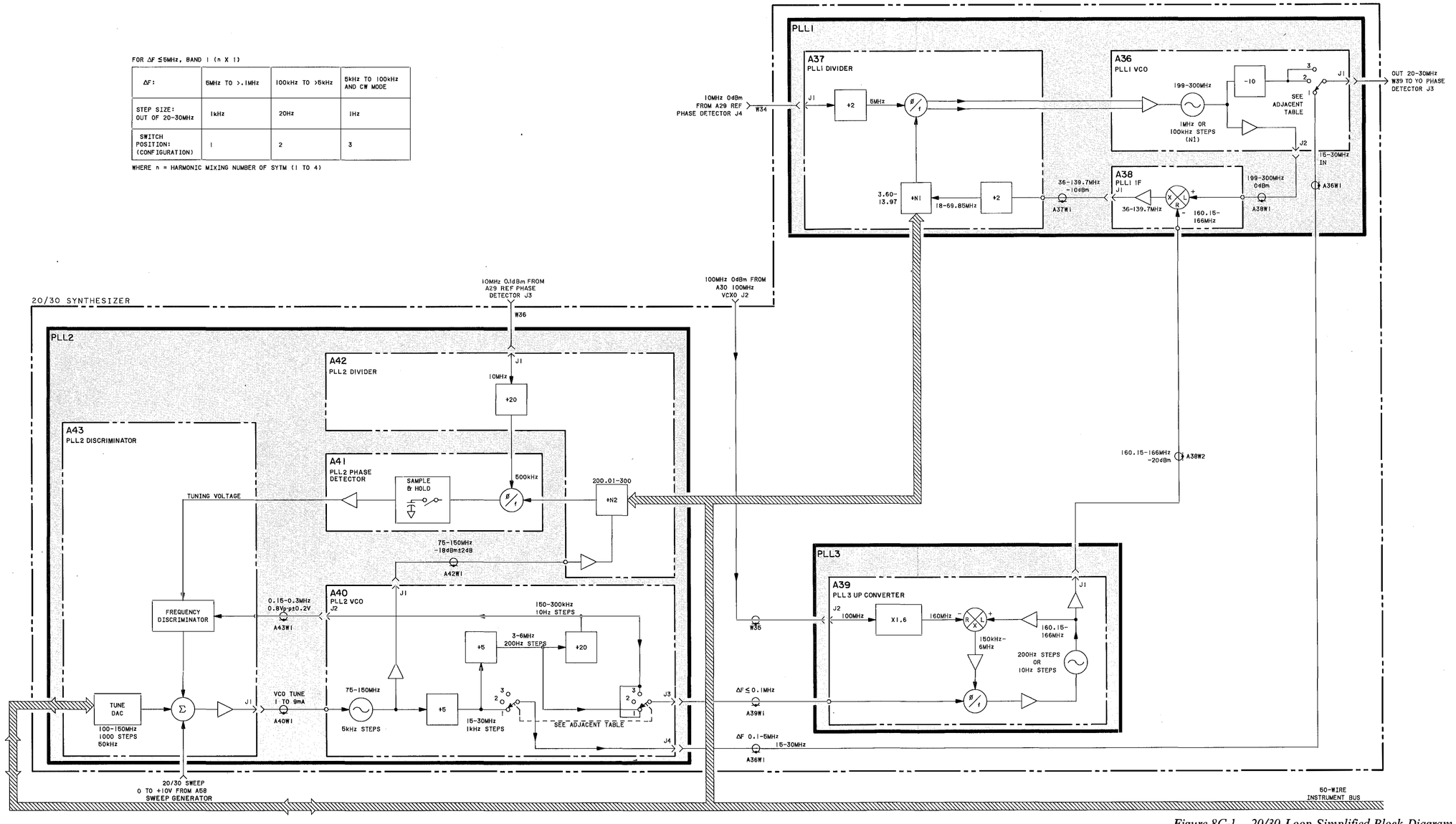

Figure 8C-1. 20/30 Loop Simplified Block Diagram

PLL2 OVERALL DESCRIPTION

INTRODUCTION

PLL2 (Phase Lock Loop 2) is part of the 20-30 Loop Synthesizer. It consists of the following assemblies:

- A40 PLL2 VCO
- A41 PLL2 PHASE DETECTOR
- A42 PLL2 DIVIDER
- A43 PLL2 DISCRIMINATOR

Unlike the PLL3 and PLL1 Loops, the PLL2 Loop is always used. PLL2 provides the 20-30 Loop output directly in swept frequency modes when YO sweep width is 100kHz to 5 MHz. During YO sweep widths of 100 Hz to <100 kHz, the output of PLL2 is divided to produce a higher resolution output. The frequency, however, is also reduced such that it is no longer in the 20 to 30 MHz range. PLL3 and PLL1 Loops are used to translate the high resolution, low frequency PLL2 output back up to the proper frequency range. The PLL3 and PLL1 Loops are phase-locked to PLL2 and will track if PLL2 is swept. PLL2, PLL3, and PLL1 operate together to produce high resolution tuning in CW Mode.

DISCRIMINATOR FEEDBACK

In narrow sweeps, ≤5 MHz, it is the 20-30 Loop that is being swept. Since PLL2 is the loop that PLL1, PLL3, and the YO Loop track, its sweep accuracy will determine the instrument's sweep accuracy. To improve the accuracy of the sweeps, a discriminator is used in a feedback loop around PLL2 VCO. The discriminator is a very accurate frequency-to-current converter. Its frequency-to-current ratio is much more linear than the VCO tuning characteristics, so using the discriminator as the feedback element will produce the equivalent of an extremely linear VCO. This is diagrammed in Figure 8C-2. The tuning linearity of this VCO/Discriminator combination is primarily a function of the discriminator and not of the VCO.

PHASE-LOCK OPERATION

There are two feedback paths around the PLL2 VCO; one is the discriminator described above, and the other is the phase-lock loop path. If one considers the discriminator to be a part of a linearized VCO, then there is only the one phase-lock loop feedback path to consider. This is shown in Figure 8C-3.

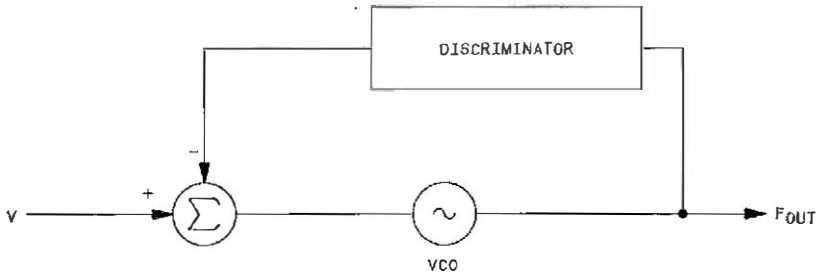

Figure 8C-2. PLL2 Discriminator Feedback

The phase lock loop path is closed during the pre-sweep interval in swept modes, and is closed at all times in CW mode of operation. While the loop is locked, the sweep ramp input is zero volts and the phase detector output tunes the VCO by changing the frequency-to-current ratio of the discriminator. After phase-lock has been established, the phase-lock loop path is opened and the error voltage (ie. tune voltage to discriminator) is stored in a sample-and-hold circuit. In this way, the start frequency of the sweep is established with phase-locked precision and the discriminator frequency-to- current ratio is calibrated to remove any warmup or drift effects. To sweep the VCO, a precision voltage ramp is summed into the input of the discriminator/VCO combination. Since the discriminator feedback loop is still intact and the phase lock loop is now opened, any voltage introduced at the input to the discriminator/VCO will be cancelled through negative feedback. The result is a ramp in the VCO frequency that will cause the discriminator output to exactly cancel the sweep ramp at the input.

SAMPLE-AND-HOLD CIRCUIT

The sample-and-hold circuit that retains the discriminator tuning voltage during the sweep must have extremely low drift to maintain the sweep accuracy over a 200 second sweep. This is accomplished by using an analog integrator to store a small portion of the error voltage, and storing the most significant portion in a digital form. The analog integrator may drift but the effect on the sweep accuracy is slight since the significant portion of the error voltage is in digital form, and will remain stable during the sweep. A simplified diagram of the sample-and-hold is shown in Figure 8C-4.

Whenever the voltage stored on the integrator capacitor exceeds

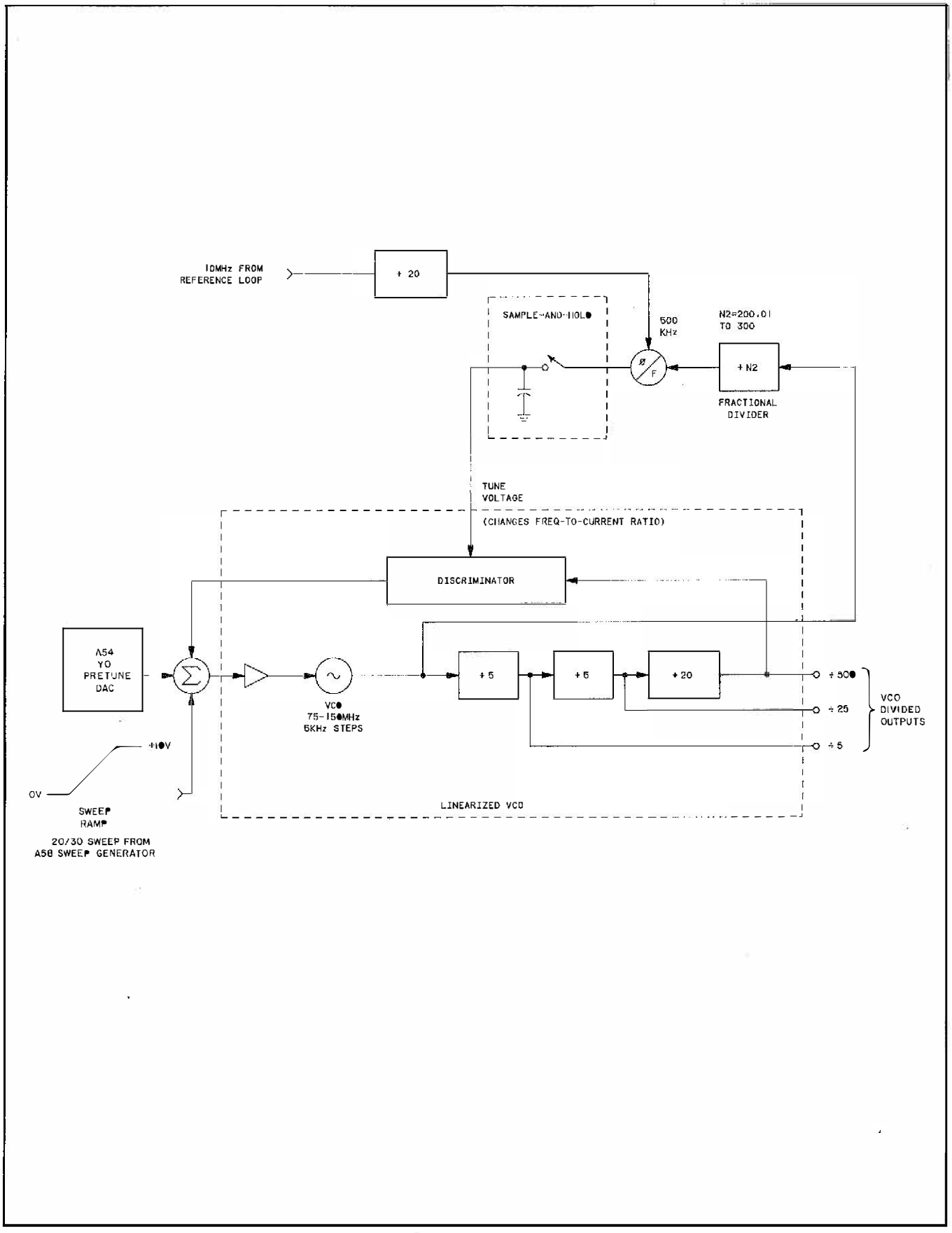

Figure 8C-3. Phase Lock Loop 2 Operation

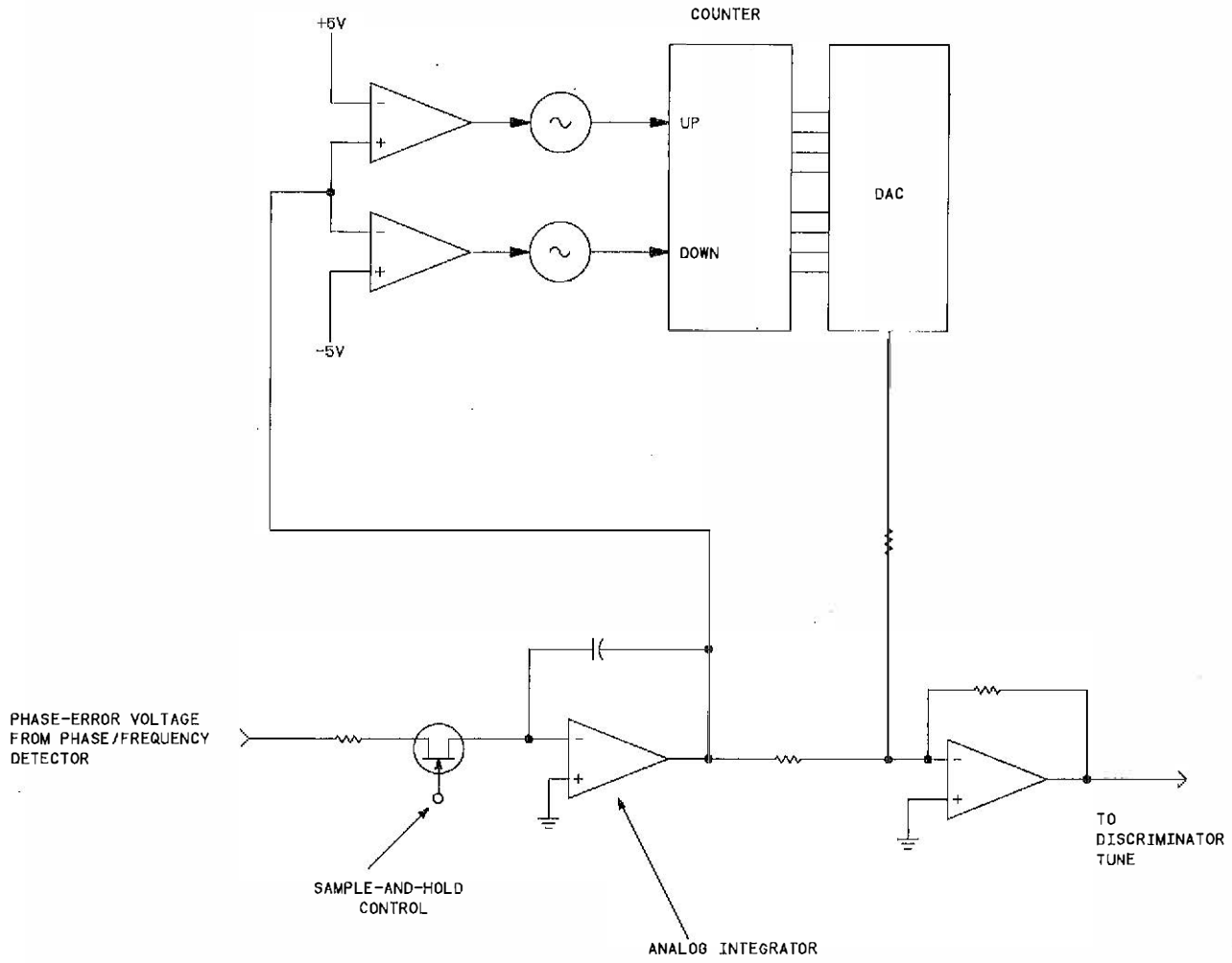

Figure 8C-4. PLL2 Simplified Sample and Hold Circuit

approximately ± 5V, one of the two comparators will turn on its associated clock. The clock will either increment or decrement the counter which will increase or decrease the current out of the DAC. The DAC output will further correct the tuning voltage for the discriminator, thereby reducing the voltage on the integrator capacitor to within the ±5V window. To hold the discriminator tuning voltage during the sweep, the FET is turned off.

VCO RANGE AND STEP-SIZE

The PLL2 VCO is a varactor-tuned transistor oscillator with a tuning range of 75-150 MHz. The phase-lock loop allows it to be programmed in 5 kHz steps between 100-150 MHz. The sweep width can be as wide as 25 MHz (PLL2 VCO sweeps down in frequency) and as narrow as 500 kHz. The output of the VCO is divided by several digital frequency dividers to be sent to various destinations. These divided outputs are shown in Table 8C-2:

Table 8C-2. 20-30 Loop Frequency Range vs. Divider Configuration

OUTPUT OF PLL2 VCO	FREQ RANGE	DESTINATION
Direct output of VCO	75-150 MHz	PLL2 FRACTIONAL DIVIDER
Divided by 5	15-30 MHz	Used as a 20-30 output
Divided by 25	3-6 MHz	Sent to PLL3 Upconverter
Divided by 500	150-300 kHz	Sent to PLL3 Upconverter

DIVIDER

There are two digital frequency dividers used in the A42 PLL2 DIVIDER. One is a fixed divide-by-20 that is used to create a 500 kHz signal from a 10 MHz reference (the 10 MHz reference is from the A29 Reference Phase Detector). This 500 kHz signal is the reference signal for the PLL2 loop and is used as one input to the phase-detector.

The second divider is a fractional divider that uses pulse-swallowing techniques to divide the PLL2 VCO output by numbers between 200.01 and 300.00.

Refer to the "Frequency Range and CW Mode Accuracy" Performance Test for use as a troubleshooting aid.

PLL3 OVERALL DESCRIPTION

The PLL3 (Phase Lock Loop 3) is part of the 20-30 Loop Synthesizer. It consists of only the A39 Upconverter Assembly.

The PLL3 and PLL1 phase-lock loops are only used when in CW Mode or in swept frequency modes with YO sweep widths less than 100 kHz.

Refer to Figure 8C-1, 20-30 Simplified Block Diagram, and Figure 8C-5, PLL3 Phase Lock Loop 3 Operation.

During sweeps of 100 kHz to 5 MHz, the output of the PLL2 VCO (75 to 150 MHz) is divided by 5 to provide a 15 to 30 MHz output, which is sent directly to the 20-30 Loop output. For sweep widths less than 100 kHz, this configuration provides insufficient resolution (1 kHz) to set the start frequency to closer than 0.5% of the sweep width.

To provide for finer resolution, the output of the PLL2 VCO is divided down even further (either by 25 for YO sweep widths of 5 kHz to 100 kHz or by 500 for YO sweep widths less than 5 kHz). The frequency, however, is also reduced such that it is no longer in the 20 to 30 MHz range. PLL1 and PLL3 Loops are used to translate the high resolution, low frequency PLL2 output up to a 200 to 300 MHz range. Since a translation is a fixed offset in frequency, it will not change the resolution or sweep width as does dividing or multiplying. After the frequency translation, the output of PLL1 is divided by 10 to reduce the phase-lock range from 200-300 MHz to 20-30 MHz. This also increases the output resolution by a factor of 10.

The function of the A39 PLL3 Assembly is to mix 160 MHz with the output of the A40 PLL2 VCO and output the sum of the two frequencies. This is done using a phase-lock loop having a closed loop bandwidth of approximately 10 kHz. PLL3 uses a reference signal from the 100 MHz VCXO reference to generate the 160 MHz offsetting frequency. As the PLL2 output changes frequency, the PLL3 output will also change frequency with the same resolution and sweep width, but at a higher operating frequency.

FREQUENCY MULTIPLIER X 1.6

In order to offset the PLL2 output by 160 MHz, a 160 MHz reference signal must be generated. The FREQUENCY MULTIPLIER X 1.6 generates 160 MHz by dividing the 100 MHz input reference signal by five and then selecting the eighth harmonic.

MIXER

The output of the MIXER is amplified, filtered, and sent to the PHASE/FREQUENCY DETECTOR. The desired MIXER output is the difference frequency and lies between 150 kHz and 6 Mhz.

PHASE/FREQUENCY DETECTOR

The PHASE/FREQUENCY DETECTOR generates a differential output signal that is used by the LOOP AMPLIFIER as well as the PHASE LOCK INDICATOR.

LOOP AMPLIFIER

The phase detector differential outputs are the inputs to the LOOP AMPLIFIER. Each of the differential inputs is passed through identical low-pass filters and a voltage divider/filter. The output of the voltage divider is sent to a varactor diode that tunes the VCO.

160 to 166 MHz VCO

The 160 to 166 MHz VCO is a varactor-tuned, Colpitts transistor oscillator. A buffer transistor output provides a 160 to 166 MHz signal that drives the MIXER.

PHASE LOCK INDICATOR

The PHASE LOCK INDICATOR senses the outputs of the phase detector to determine when the loop is locked. The ON=LOCKED LED indicates that a phase locked condition exists.

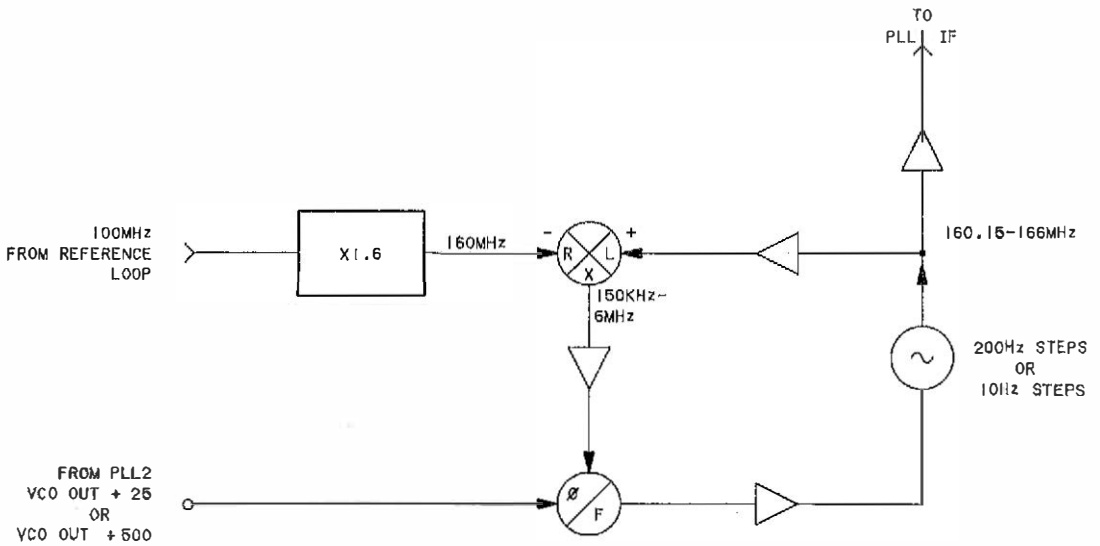

Figure 8C-5. Phase Lock Loop 3 Operation

PLL1 OVERALL DESCRIPTION

INTRODUCTION

PLL1 (Phase Locked Loop 1) is part of the 20-30 Loop Synthesizer. It consists of the following assemblies:

- A36 PLL1 VCO
- A37 PLL1 DIVIDER
- A38 PLL1 IF

DESCRIPTION

The PLL1 and PLL3 phase-lock loops are only used when in CW Mode or in swept frequency modes with YO sweep widths less than 100 kHz.

PLL1 functions as a programmable frequency translator. The input to the translator is the PLL3 output (160.15 to 166 MHz). The PLL1 VCO frequency is offset by a programmable amount from the PLL3 output. As the PLL3 output changes frequency (ie. as it tracks a sweeping PLL2) the offset frequency between the PLL3 output and the PLL1 VCO output will remain constant. The offset frequency, PLL1 IF output, is determined by the value of programmable divider N1 and is constant throughout the sweep. The result is that the precision sweeps and high resolution of the PLL2 Loop are effectively transferred up in frequency to the PLL1 VCO.

A simplified diagram of the PLL1 Loop is shown in Figure 8C-6.

The phase/frequency detector for PLL1, which resides on the A37 PLL1 DIVIDER assembly, operates at 5 MHz. One of the phase detector inputs comes from a 10 MHz (A29 Reference Phase Detector) reference which is divided by two on the A37 assembly. The second phase detector input is the PLL1 IF output, after passing through a divide-by-two and a fractional divider. The fractional divider uses pulse-swallowing techniques to divide by numbers between 3.60 and 13.97.

When the loop is locked, both phase detector inputs will be equal in frequency. The PLL1 IF output is then described by; F1 = N1 * 10 MHz, where F1 is the PLL1 IF output frequency MHz and N1 is the fractional divide number (3.60 to 13.97).

The A38 PLL1 IF assembly's primary function is to mix the output of PLL1 VCO with the output of the PLL3 Loop (Fpll3). The frequency relationships at the mixer are; F1 = F2 - Fpll3, where

F1 is the PLL1 IF frequency and F2 is the PLL1 VCO frequency. The PLL1 VCO frequency can be shown to be; F2 = Fpll3 + 10*N1 MHz. This shows that the PLL1 VCO frequency will be offset by 10*N1 MHz from the PLL3 output frequency.

PLL1 VCO operates from 200 to 300 MHz. The output of the VCO is divided by ten to place it in the 20 to 30 MHz range.

After the final divide-by-ten, the output frequency of the 20-30 loop becomes; Fout = (Fpll3)/10 + N1 MHz. Fpll3 can be determined from the 8340A diagnostics by pressing [SHIFT] [M3] and reading the right-hand "FREQUENCY MHz" display. If this display reads "0.0000" then the PLL3/PLL1 path is not being used in this mode, and PLL2 is used by itself. Fout, the 20-30 output frequency, can be determined by pressing [SHIFT] [M1] and reading the right "FREQUENCY MHz" display. N1 can be calculated from these two frequencies using the above equation.

As the N1 divide number changes, the gain of the loop amplifier is adjusted to maintain an approximately constant loop gain. This is done through FET switches on the A36 PLL1 VCO assembly.

The PLL1 VCO assembly also contains an output switch to select from one of two possible 20-30 Loop paths;

1. The PLL1 VCO divided-by-ten is used as the 20-30 Output. PLL2 is translated up through PLL3 and PLL1.

2. The PLL2 VCO divided output is used directly. PLL1 and PLL3 are not used.

The switch positions are defined for the different 8340 operating modes in the table in Figure 8C-6.

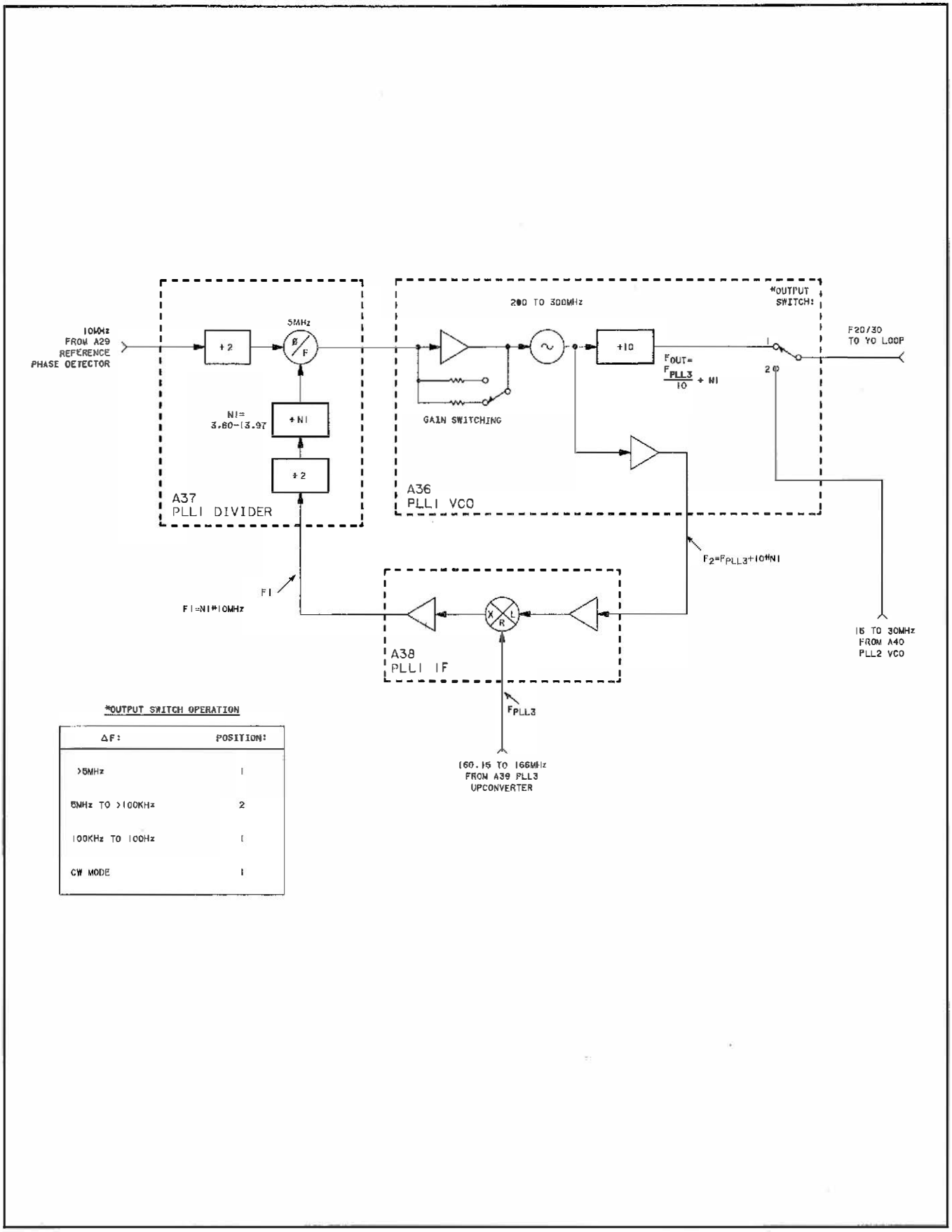

Figure 8C-6. PLL1 Simplified Diagram

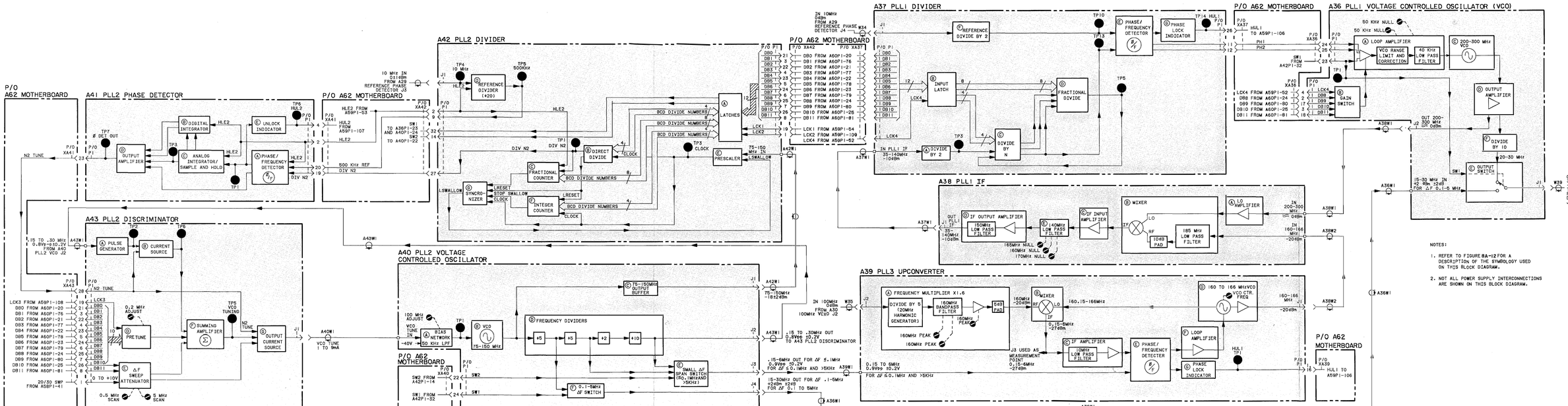

Figure 8C-7. 20-30 Loop Block Diagram

TROUBLESHOOTING TO ASSEMBLY LEVEL

Refer to **"OVERALL INSTRUMENT TROUBLESHOOTING"** in the Service Introduction.

REPAIR PROCEDURES

Refer to the **"REPAIR PROCEDURES"** description in the Service Introduction.

A36 PHASE LOCK LOOP 1 (PLL1) VOLTAGE-CONTROLLED OSCILLATOR (VCO), CIRCUIT DESCRIPTION

DESCRIPTION

The output of the 20-30 loop to be fed to the YO Loop is always taken from A36 (PLL1 VCO). If the sweep width is such that the PLL2 VCO's divided output is required as the 20-30 output, a switch on this board selects the proper source.

A36 contains the loop amplifier and voltage-controlled oscillator for the PLL1 phase lock loop. The oscillator tunes from 200 to 300 MHz for a range of about 4 to 16 volts tuning of the varactor. The oscillator drives a counter which divides the frequency by 10. The counter output goes through a switch and a filter to the 20-30 output. To prevent spurious responses, the oscillator is turned off for sweeps that are greater than 100kHz but less than or equal to 5MHz.

LOOP AMPLIFIER A

A diagram of the equivalent circuit of the loop amplifier is shown in Figure 8C-8. It functions as a differential integrator, due to the feedback presented by R30,C33, and R29,C34. The gain block shown in Figure 8C-8 is achieved by the low-noise differential pair, Q9 and Q10, in addition to operational amplifer U6A. Compensation for this high open-loop gain circuit is provided by C32 and R26. Since there is no dc feedback path in this circuit, it exhibits extremely high low frequency gain.

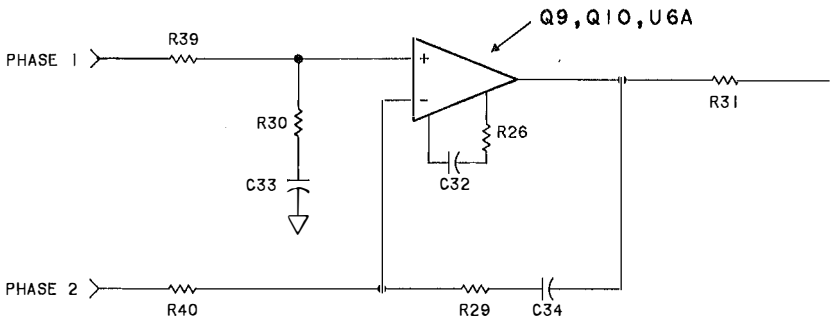

Figure 8C-8. Loop Amplifier Equivalent Circuit

The output of the differential integrator is fed through a programmable ac voltage divider formed by R31, R32, R33, R34, R35 with R36 and C36. Following this is a 40kHz low pass filter which has two notches that are tuned to reject 50kHz generated by the fractional division used in PLL1 divider.

VR1 and R37 conduct when large currents are required to charge C22. During locked conditions, VR1 should always be off.

Since there are upper AND lower sidebands generated by the PLL1 IF mixer, it is possible that the VCO could be disturbed by the presence of both sidebands. While it is impossible for the loop to actually lock onto the wrong sideband, due to the inversion in loop gain, the VCO would be tuned to an endpoint. The out of range corrector prevents this from happening by monitoring the dc tune voltage and forcing the VCO in the opposite direction should it attempt to exceed its normal range. U6B compares the dc tune voltage across C36 to +17.5V. If the tune voltage exceeds this, U6B output goes LOW, turning on CR5, and pulling the non-inverting input to the differential integrator LOW. This forces the VCO tune voltage to decrease until it reaches about +5V, at which point the hysteresis around U6B (due to R24) causes U6B to return to its inactive HIGH state.

A mode exists where the VCO may be OFF, and when programmed ON will remain disabled due to noise driving the phase detector and loop amplifier such that the VCO is continually driven to its OFF state. To ensure that the VCO will always oscillate, the VCO range limiter clamps the lower end of the tune voltage to about +3V. This should always be lower than the minimum tuned voltage in normal operation, so Q2 should never be on when phase-locked. Q2 functions as a clamp due to its base being biased at about +4.4V by R10 and R7. If the tune voltage drops to a low enough voltage, Q2 and CR7 will conduct, and clamp the tune line to two diode drops below +4.4V (+3V).

GAIN SWITCH B

U5 latches the four most significant bits of the programming of PLL1 divider (N=3 to 13). These are level translated by U4 which drives four FET switches. By activating combinations of FET's, a programmable resistance is placed in parallel with R31, changing the amount of attenuation. As the digital divider changes numbers, the loop gain directly follows it. By increasing the amount of gain in the loop amplifier, switching the FETs in or out, a constant loop bandwidth of 5 kHz is approximated. A table of the states of the FET's is shown in Table 8C-3.

200 to 300 MHz VCO C
OUTPUT AMPLIFIER D

The VCO consists of Q11 which operates in the grounded-base mode. The resonator is principally CR3, CR4, and L4. Feedback is accomplished with L5, R16, and C17. The output, taken at C14, is coupled through R42 and C12 to common base buffer amplifier Q5. See Figure 8C-9 for a simplified block diagram. The capacitor C14 actually behaves as a small inductor over the frequency range of interest (200-300 MHz). This characteristic allows a signal to be developed across the capacitor and then coupled out whereas an ideal capacitor would short the signal to ground. The VCO is turned off in sweeps greater than 100 kHz and less than or equal to 5 MHz by forward biasing the varactor diodes CR3 and CR4. A low input on SW1 causes CR2 (in Block A) to conduct and pull the base of Q2 to about 0.7V. This sets the clamp voltage at the cathode of CR7 to about -0.7V. This maximum voltage of -0.7V guarantees that the diodes will be biased on, disabling the VCO. The output of Q5 is applied to Q4 where it is amplified and sent to A38 PLL1 IF and to Block F DIVIDE BY 10.

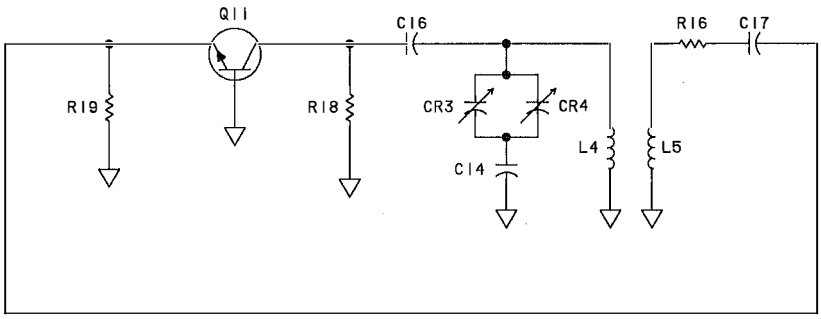

Figure 8C-9. 200-300 MHz VCO Simplified Block Diagram

OUTPUT SWITCH E

The output switch is U2, a quad ECL NOR gate. For sweep widths greater than 100 kHz and less than or equal to 5 MHz the SW1 line is a TTL low. This low disables the LOOP AMPLIFIER by causing CR6 (Block A) to conduct and pull the base of Q9 low. A low input on Q9 causes the output of U6A to go negative which causes the varactor diodes CR3 and CR4 to be biased on, disabling the VCO. The low on SW1 also disables U2D by causing U2C to go to a high output level. U2B is enabled in this condition and so routes the

15-30 MHz input from PLL2 VCO to the output. For all other sweep conditions the SW1 line is high and the loop is enabled. The output is then taken from U1D which has the divided by 10 VCO frequency as its input.

DIVIDE BY 10 F

Q3 is a common-emitter amplifier which drives U3 through a high-pass filter. U3 is an ECL divide by 10 counter which generates the necessary 20 to 30 MHz from the VCO output.

Table 8C-3. FET Switch Programming Table

Divide Number	Active FET			
	Q1	Q7	Q8	Q6
3	X	X		
4				X
5		X		X
6	X			X
7	X	X		X
8			X	
9		X	X	
10	X		X	
11	X	X	X	
12			X	X
13		X	X	X

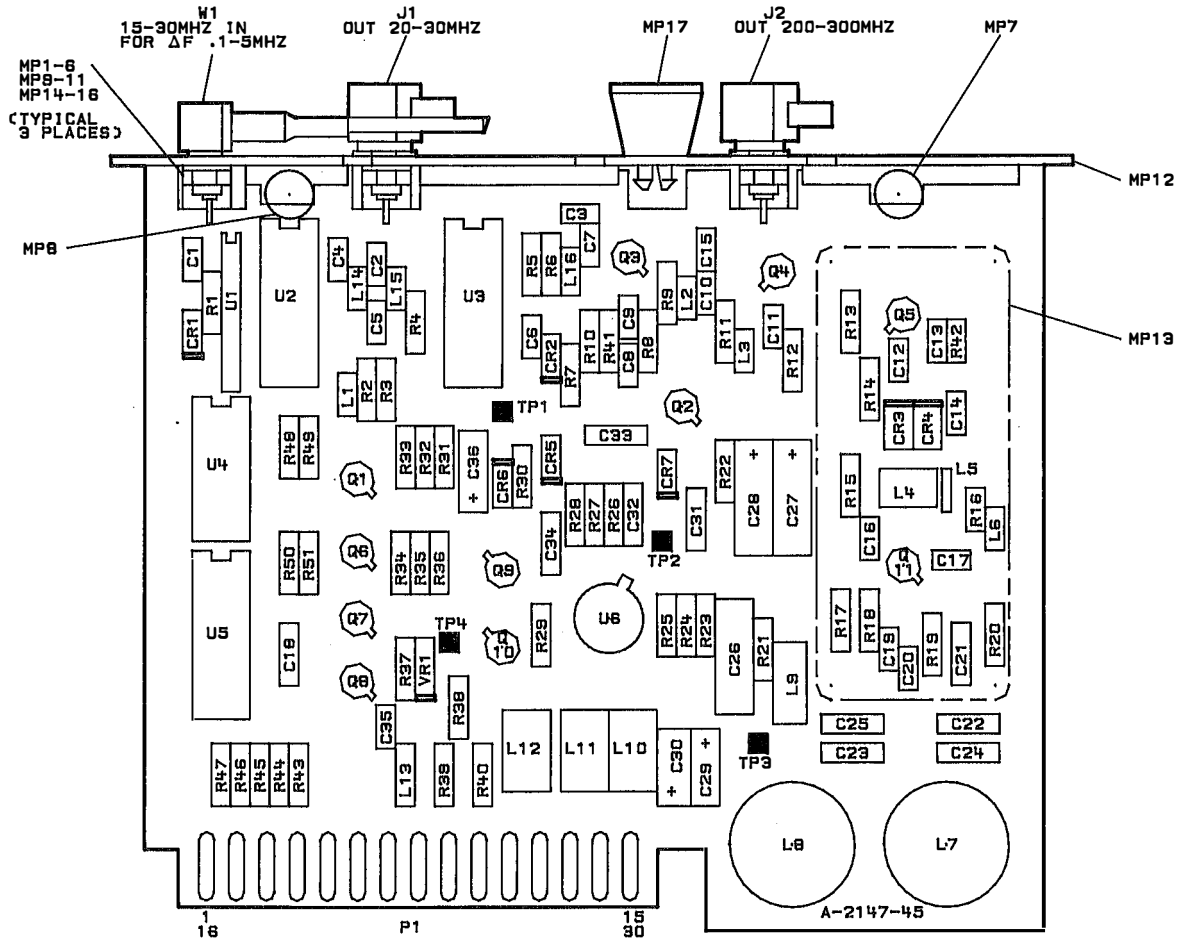

Figure 8C-10. A36 PLL1 VCO, Component Location Diagram

A36 PLL1 VCO, Pin I/O

A36

Pin	Mnemonic	Levels	Source	Destination
1	GND	0V	A62 STAR GND	*G
16	GND	0V	A62 STAR GND	*G
2	DB8	TTL	*	*THRU A62R7 TO B
17	DB9	TTL	*	*THRU A62R8 TO B
3	DB10	TTL	*	*THRU A62R9 TO B
18	DB11	TTL	*	*THRU A62R10 TO B
4	LCK4	TTL (LOW TRUE)	XA59P1-52	*THRU A62R11 TO B
19	GND	0V	A62 STAR GND	*G
5	GND	0V	A62 STAR GND	*G
20	GND	0V	A62 STAR GND	*G
6	GND	0V	A62 STAR GND	*G
21	GND	0V	A62 STAR GND	*G
7	GND	0V	A62 STAR GND	*G
22	GND	0V	A62 STAR GND	*G
8	GND	0V	A62 STAR GND	*G
23	SW1	TTL	XA42P1-32	*E
9				
24	PH1	0 TO +5V	A62R12	A
10	GND	0V	A62 STAR GND	*G
25	PH2	0 TO +5V	A62R13	A
11	GND	0V	A62 STAR GND	*G
26	GND	0V	A62 STAR GND	*G
12	−10V	−10V	XA53P1-12, 13, 31, 32	*THRU A62L8 TO G
27	−10V	−10V	XA53P1-12, 13, 31, 32	*THRU A62L8 TO G
13	+12V UI ADJ	+10.5V	XA52P1-10	*THRU A62L2 TO G
28	+12V UI ADJ	+10.5V	XA52P1-10	*THRU A62L2 TO G
14	GND	0V	A62 STAR GND	*G
29	GND	0V	A62 STAR GND	*G
15	+5.2V	+5.2V	XA52P1-17, 18, 41, 42	*THRU A62L1 TO G
30	+5.2V	+5.2V	XA52P1-17, 18, 41, 42	*THRU A62L1 TO G

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A36 PHASE LOCK LOOP 1 (PLL1)
VOLTAGE CONTROLLED
OSCILLATOR (VCO)
08340-60042

NOTES:
1. REFER TO THE SERVICE SECTION INTRODUCTION FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES SHOWN ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. J1,J2 AND A36W1 CENTER CONDUCTORS ARE ELECTRICALLY CONNECTED TO THE PC BOARD THROUGH SOLDERED 24 GAUGE FINE WIRES. THEIR OUTER CONDUCTORS ARE ELECTRICALLY CONNECTED TO PC BOARD GROUND THROUGH MECHANICAL SCREW CONNECTIONS IN THE ASSEMBLY COVER PLATE.

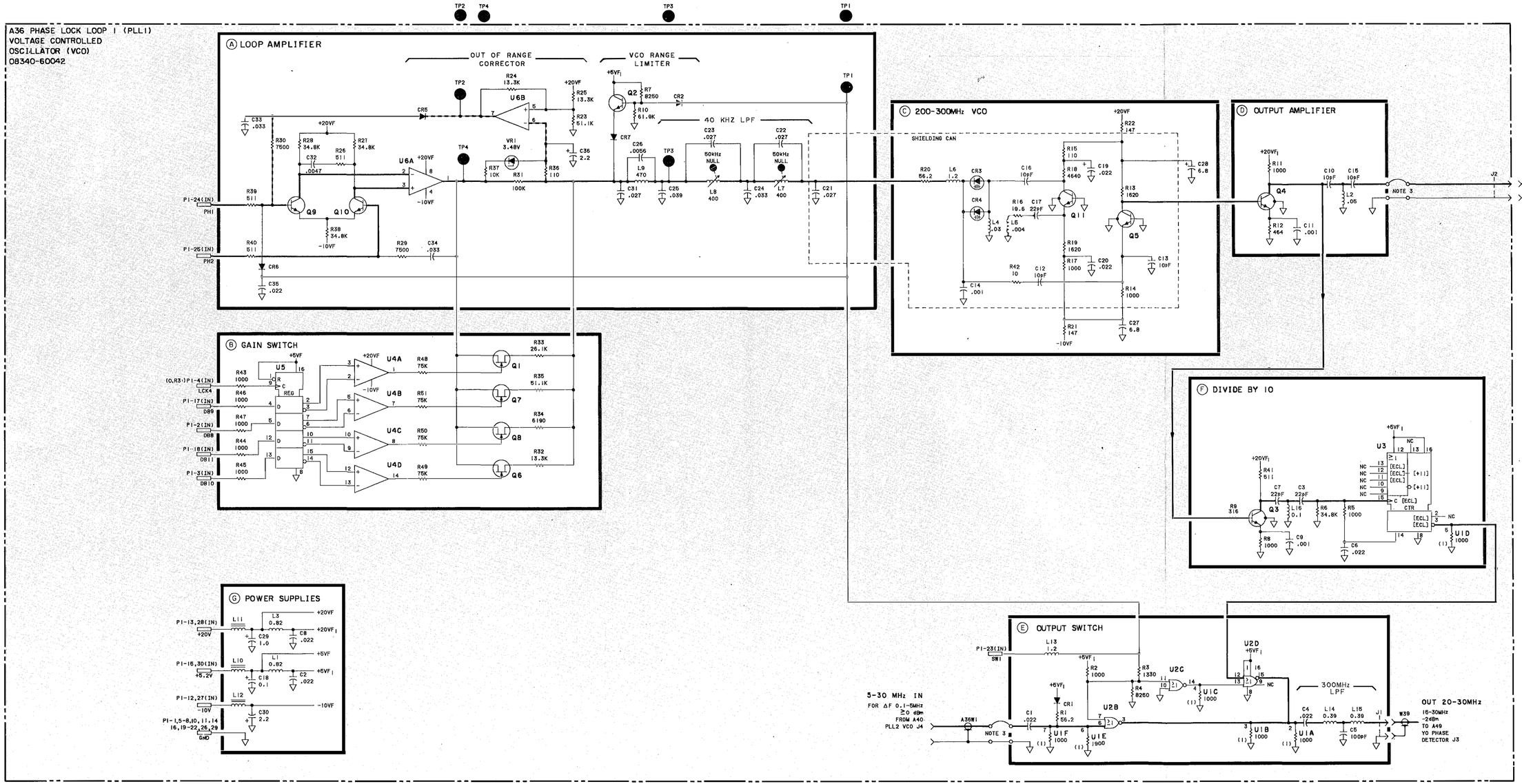

Figure 8C-11. A36 PLL1 VCO, Schematic Diagram

A37 PHASE LOCK LOOP 1 (PLL1) DIVIDER, CIRCUIT DESCRIPTION

INTRODUCTION

A37 functions as a programmable frequency divider and a phase/frequency detector.

DESCRIPTION

The divider is programmed by the A60 Processor to divide the input frequency down to 5 MHz. This is then compared with a 5 MHz reference in the phase/frequency detector. The detector output, after amplification, controls the frequency of the PLL1 voltage-controlled oscillator.

The divide number is always between 3.60 and 13.97. The integer part is coded in binary while the fractional part is coded in BCD.

The PLL1 Divider works on the pulse swallowing technique. Figure 8C-12 shows the basic diagram of a pulse swallowing divider.

The rate multiplier is formed by 2 TTL decade rate multiplier IC`s. The input to the rate multplier is the output of the overall divider. For 100 divider output pulses, the rate multiplier will output X pulses where X is a two digit BCD number that is between 0 and 99. The pulses out of the rate multiplier are not necessarily evenly spaced, but will always be X/100 times the number of input pulses to the rate multiplier. Each time the rate multiplier outputs a pulse, the input signal in the DIVIDE-BY-N block is effectively ignored for one entire input pulse. This means that N+1 input pulses will transpire before the next output pulse will occur; or the integer divide number is effectively N+1 for this particular output pulse. If the rate multiplier does not output a pulse, then the DIVIDE-BY-N continues to divide by N normally.

The result of this is that for 100 output pulses, the integer counter was dividing by N+1 for X output pulses, and dividing by N for the remaining 100-X output pulses. The total number of input pulses that occurred was : (N+1)*X + N*(100-X) = 100*N + X . The divide number (input pulses divided by output pulses) is (100*N + X)/100 = N + X/100. So N becomes the integer portion of the overall divide number, and X becomes fractional part. For example: to divide by 8.57, the DIVIDE-BY-N would be set to 8 and the rate multiplier would be programmed to 57.

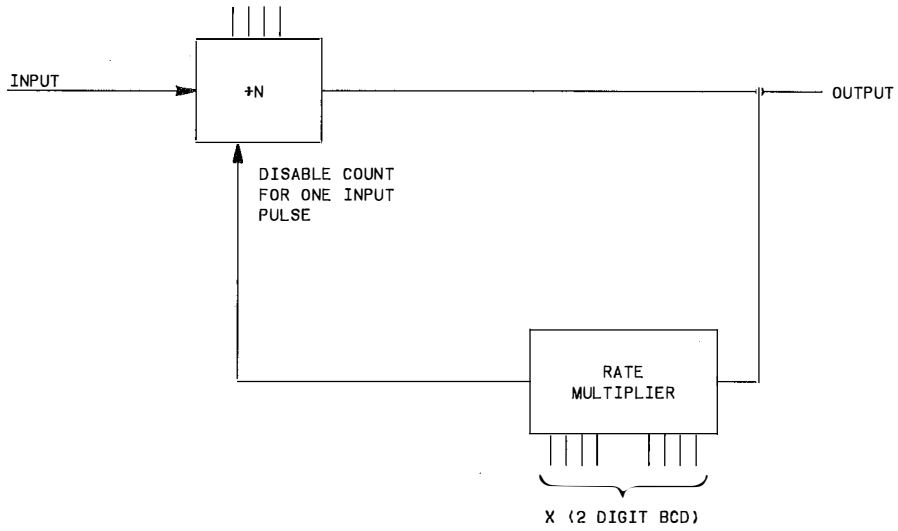

Figure 8C-12. Fractional Division Using Pulse Swallowing

Refer to the "Frequency Range and CW Mode Accuracy" Performance Test for use as a troubleshooting aid.

DIVIDE-BY-2 A

U5 constitutes a 3-stage limiting amplifier. U5 is an ECL triple line receiver which changes the input to the proper amplitude and and dc level (approximately +3 volts LOW and +4 volts HIGH) for driving the subsequent divider. U4A is a D-type flip flop which divides the limiting amplifier output by 2.

INPUT LATCH B

U9 and U10 are latches which store the divider programming number. The number is clocked into the latches with LCK4.

DIVIDE-BY-N C

U12 is a 4-bit binary counter which is programmed with the integer part (3 to 13) of the divide number. It is an ECL device which is in one of three states at all times : counting down, loading, or in a hold state. The state of U12 is determined by the status of TP6 LNLOAD [Low N LOAD] and TP5 HSWALLOW (HIGH SWALLOW input pulse). The input clock is the output of the DIVIDE-BY-2 (Block **A**). This output is also the clock for U14A,B and U4B. The divider is loaded with the integer portion of the divide number, and then decrements at each clock pulse until the count of 2 is reached. At this time, the wire-OR`d bits (TP8) will be 0 and U14B pin 15 will be set up to be clocked LOW on the following clock pulse. U14B pin 15 is LNLOAD, so the counter will be loaded with the integer divide number synchronously with the next rising clock edge. This operation repeats every N clock pulses unless the SWALLOW CONTROL causes HSWALLOW to go HIGH. Figure 8C-13 shows the operation of the DIVIDE-BY-N without a HSWALLOW pulse. U4B is a synchrously cleared, asynchronously set flip-flop, due to its D and S inputs tied together. Its relationship to TP6 LNLOAD is also shown in Figure 8C-13. The asynchronous clear is necessary to widen the width of the output pulse for timing purposes in the SWALLOW CONTROL (Block **D**).

FRACTIONAL DIVIDER D

The Fractional Divider determines whether or not to cause the Divide-By-N to ignore an input pulse and divide by N+1. It does this by controlling the state of HSWALLOW. U1 and U2 are the actual TTL decade rate multipliers, with U3B and Q1 used to translate the ECL levels to TTL. Each time there is an output pulse (TP13) from the Divide By N, U1 and U2 may or may not output a pulse, depending upon what they are programmed to. If they do output a pulse, it will cause TP7 to go low and then high

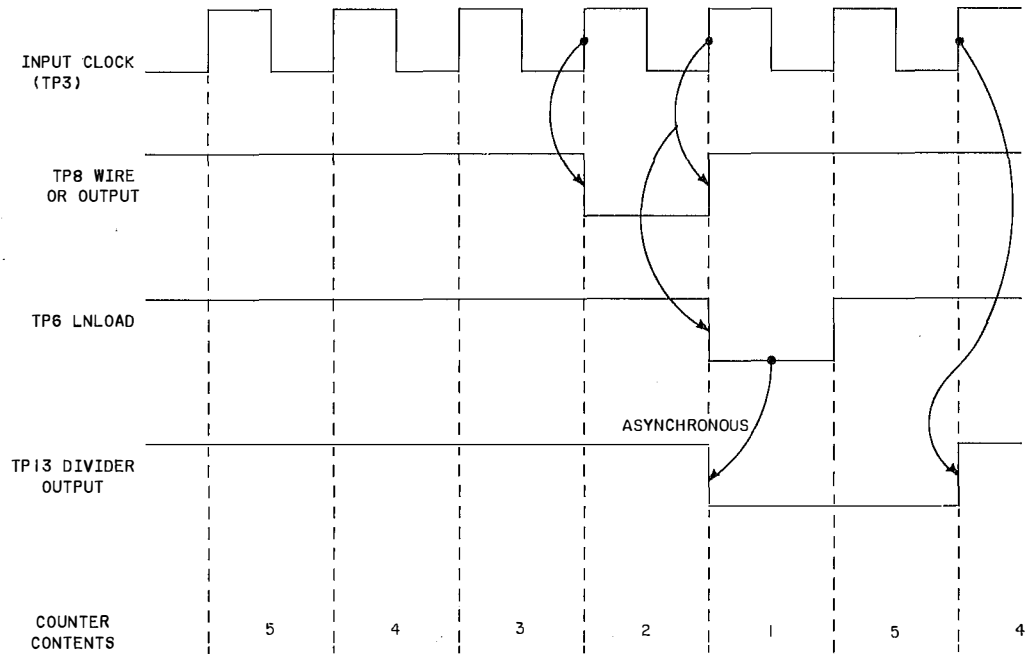

Figure 8C-13. N-Divider Operation; N = 5 (HSWALLOW not used)

in synch with the output pulse (TP13). The low-to-high transition of TP7 will clock U15B and leave it in the RESET state. U15B pin 15, LOW SWALLOW ENABLE is connected to the reset of U14B. As long as LOW SWALLOW ENABLE is HIGH, HSWALLOW will be forced LOW independently of its clock changing. But if the rate multipliers U1 and U2 cause a pulse on TP7, LOW SWALLOW ENABLE will be left LOW, and HSWALLOW will be allowed to go HIGH when the next output pulse (TP13) occurs.

The only time that states can potentially change in the Swallow Control is when there is an output pulse. The Swallow Control must decide to do one of two things for the subsequent output pulse (TP13); either divide by N or N+1. To divide by N+1, the HSWALLOW line is clocked HIGH for only one input clock pulse. To divide by N, the Divide-By-N block is left uninterrupted. The decision to swallow an input pulse is made by considering two things; whether the rate multipliers U1 and U2 output a pulse, and the state of LOW SWALLOW ENABLE prior to the output pulse (TP13). All four possible combinations are diagrammed in Figure 8C-14.

The things to notice in Figure 8C-14 are:

- Whenever LOW SWALLOW ENABLE was HIGH prior to the output pulse (TP13), HSWALLOW always remained LOW throughout the sequence, and no input pulse was swallowed.

- Whenever the rate multipliers U1 and U2 did output a pulse, LOW SWALLOW ENABLE was left in the LOW state, regardless of the previous state of the line.

The definition of these lines can then be stated:

- LOW SWALLOW ENABLE - When LOW, an input pulse will be swallowed during the next output pulse (TP13) sequence.

- HSWALLOW - When HIGH, causes U12 to hold its count. This will only be HIGH for a period of 1 input clock pulse, and will be timed such that the counter is never loading and holding at the same time.

R10 and C11 are important for the proper operation of State # 2 as shown in Figure 8C-14. Since the rate multipliers U1 and U2 did NOT output a pulse in this state, the LOW SWALLOW ENABLE line must be left in the HIGH state after the sequence is over to prevent a pulse from being swallowed next time. There would be a potential race condition occurring at the inputs to U15B if it were not for R10 and C11. U14A pin 2 HSWALLOW is going LOW, and is also clocking U15B through U3A NOR gate. U15B pin 10 is also changing and an illegal setup violation would occur. Instead, R10

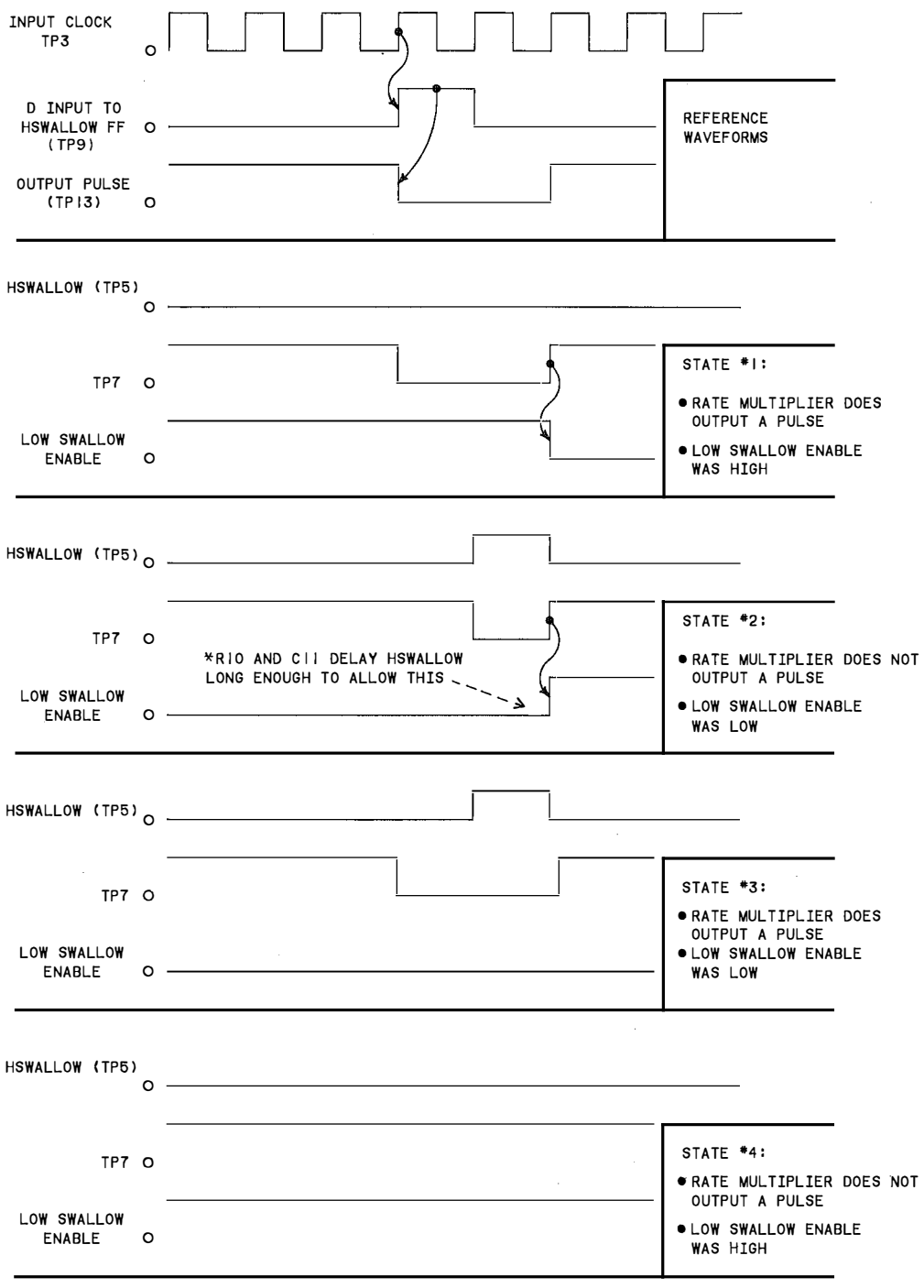

Figure 8C-14. Possible Fractional Divider Sequences

and C11 will delay the HIGH-to-LOW transition at U15B pin 10 by several nanoseconds to allow the clock to reach U15B before the HIGH on pin 10 input goes away. This leaves U15B set, as desired.

If there is a rate multiplier output, as in State # 3, then R10 and C11 are not nearly as important. In this case there are two things that are forcing TP7 LOW through U3A; the rate multiplier(s) U1/U2 and HSWALLOW. Since the rising edge of the signal at TP7 will clock U15B, then the last signal to be removed from forcing TP7 LOW will be the signal that clocks U15B. As shown in Figure 8C-14, STATE # 3, the rising edge of the signal at TP7 occurs after HSWALLOW has gone LOW. The reason is that both the signals that are forcing TP7 LOW are beginning to be removed at the same input clock pulse. HSWALLOW will be removed much sooner than the rate multiplier U1/U2 since it is an ECL device, so U1/U2 are actually clocking U15B. Since U1 and U2 have very long TTL delays compared to ECL, the effect of the R10 and C11 time delay on HSWALLOW is insignificant. The U15B pin 10 input will still go low before the clock pulse from U1/U2 arrives.

PHASE/FREQUENCY DETECTOR E

The Phase/Frequency Detector compares the divider output with a 5 MHz reference frequency. When the two inputs are in phase, the outputs are ECL HIGH, approximately +4 volts, with very narrow pulses at a 5 MHz rate. When the inputs are the same frequency but different in phase, one output line is a pulse with a width corresponding to the phase difference; the other output is HIGH with very narrow pulses. For a difference in input frequencies, the outputs are pulses of varying widths, but average dc voltage levels will be different. The sign of this dc voltage is set by which frequency is higher.

REFERENCE DIVIDE BY 2 F

U7C is an input buffer amplifier which generates the proper level for ECL (approximately +3 volts LOW and +4 volts HIGH). R5,R6, and C4 provide dc feedback around U7C to enable it to operate as a linear amplifier. U15A divides the 10 MHz input by 2 and applies this 5 MHz to the phase/frequency detector.

PHASE LOCK INDICATOR G

The input to the Phase Lock Indicator is the wire OR outputs of the phase/frequency detector (A16B pin 14 and A16A pin 3). This input is ECL LOW (approximately 3 volts) when the loop is locked; in this condition, the dc voltage at the base of Q3 is lower than that at the base of Q2 so Q3 is ON and Q2 is OFF. If the loop unlocks, the input to the phase lock indicator consists of varying width pulses, the average dc value of which is about half way between a logic LOW and HIGH. The voltage divider consisting of R35 and R15 causes the voltage at Q2 base to be lower than that at Q3 base, so Q2 turns ON indicating an unlock condition.

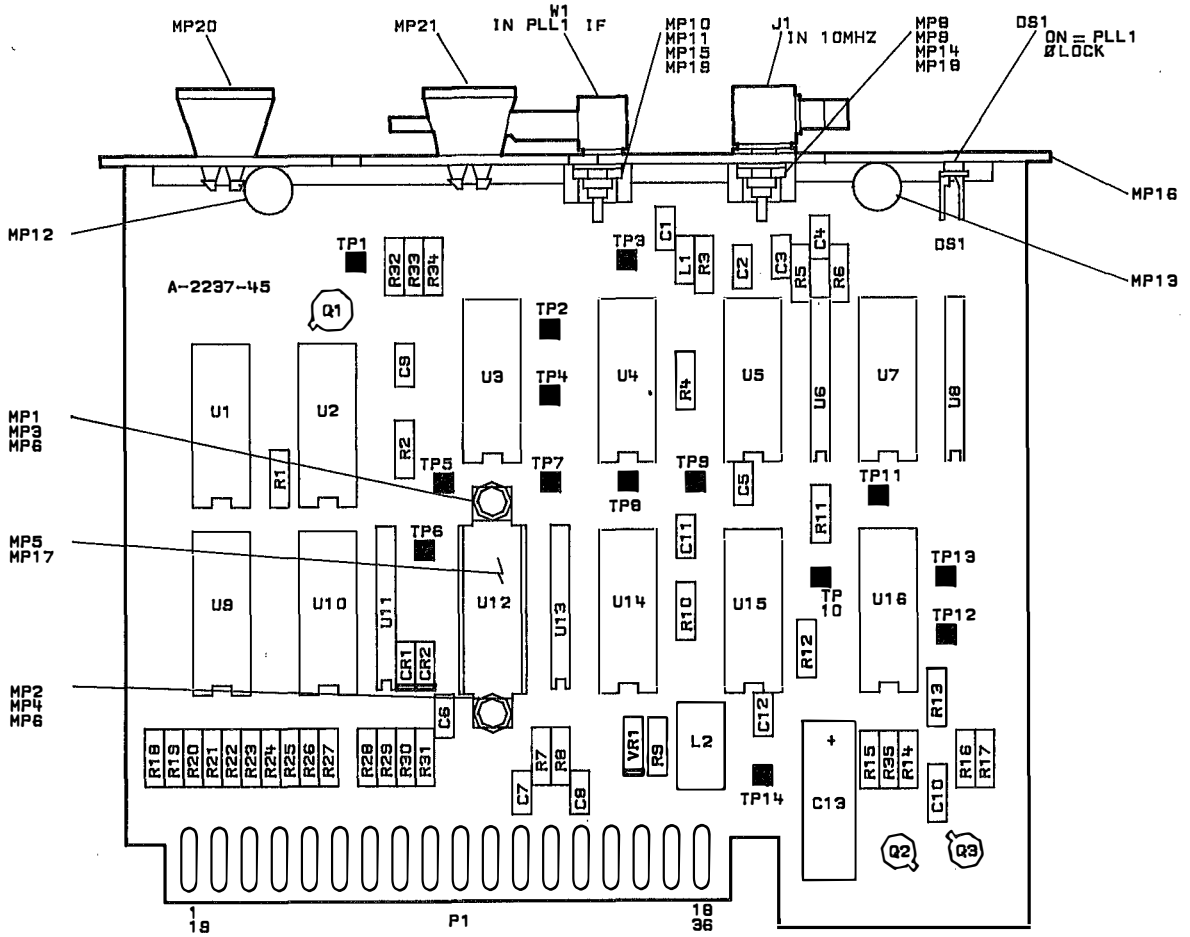

Figure 8C-15. A37 PLL1 Divider, Component Location Diagram

A37 PLL1 Divider, Pin I/O

A37

Pin	Mnemonic	Levels	Source	Destination
1 19	DB0 DB1	TTL TTL	XA60P1-20 XA60P1-76	*B *B
2 20	DB2 DB3	TTL TTL	XA60P1-21 XA60P1-77	*B *B
3 21	DB4 DB5	TTL TTL	XA60P1-22 XA60P1-78	*B *B
4 22	DB6 DB7	TTL TTL	XA60P1-23 XA60P1-79	*B *B
5 23	DB8 DB9	TTL TTL	* *	*B *B
6 24	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
7 25	DB10 DB11	TTL TTL	* *	*B *B
8 26	LCK4 HULI	TTL (LOW TRUE) TTL (HIGH TRUE)	XA59P1-52 *G	*B XA59P1-106
9 27	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
10 28	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
11 29	PH1 GND	0 TO +5V 0V	E A62 STAR GND	XA36P1-24 *H
12 30	PH2 GND	0 TO +5V 0V	E A62 STAR GND	XA36P1-25 *H
13 31	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
14 32	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
15 33	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
16 34	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
17 35	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
18 36	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*THRU A62L3 TO H *THRU A62L3 TO H

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

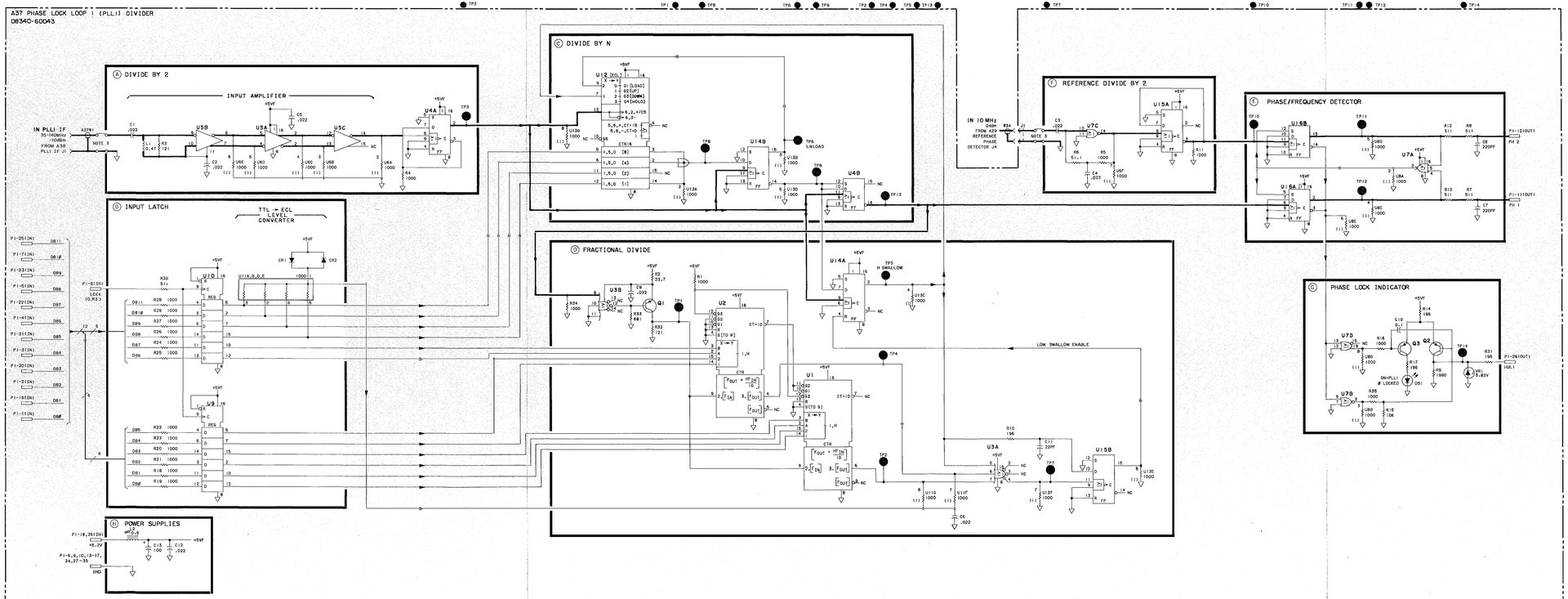

Figure 8C-16. A37 PLL1 Divider, Schematic Diagram

A38 PHASE LOCK LOOP 1 (PLL1) IF, CIRCUIT DESCRIPTION

INTRODUCTION

The function of the A38 Phase Lock Loop 1 is basically to mix the output of the A39 PLL3 Up Converter (160.15 to 166 MHz) with the LO output from the A36 PLL1 VCO (200 to 300 MHz). The output of this assembly is the difference frequency suitably filtered and amplified to about -10 dBm.

LO AMPLIFIER A

The LO Amplifier consists of common-emitter amplifiers Q1 and Q2. CR1 and CR2 provide limiting to prevent overdriving Q2 near 200 MHz where Q1 has more gain.

MIXER B

The double-balanced mixer U1 operates with about +7 dBm LO drive and with approximately -30 dBm RF signal input. The IF output is about -36 dBm and covers 30 MHz to 140 MHz. The 185 MHz Low-Pass Filter attenuates the harmonics of the RF signal input. The 10 dB pad, R10, R11, and R12 reduces the RF signal input from approximately -20 dBm to approximately -30 dBm.

IF INPUT AMPLIFIER C

The IF INPUT AMPLIFIER has an input filter to partially filter the RF and LO signals from the mixer. The amplifier Q3 has emitter degeneration R17 to reduce distortion.

IF OUTPUT AMPLIFIER D

The IF OUTPUT AMPLIFIER consists of two common emitter stages and an output low-pass filter. The two stages are coupled by C14 and L17 which provide high frequency peaking.

140 MHZ LOW-PASS FILTER E

The 140 MHz LOW-PASS FILTER is a modified elliptic filter which must pass 140 MHz while rejecting 160 to 166 MHz by at least 60 dB. The three adjustable coils optimize the stop band by providing nulls at the frequencies shown on the schematic (Figure 8C-18). This filter also filters the LO frequencies (200-300 MHz).

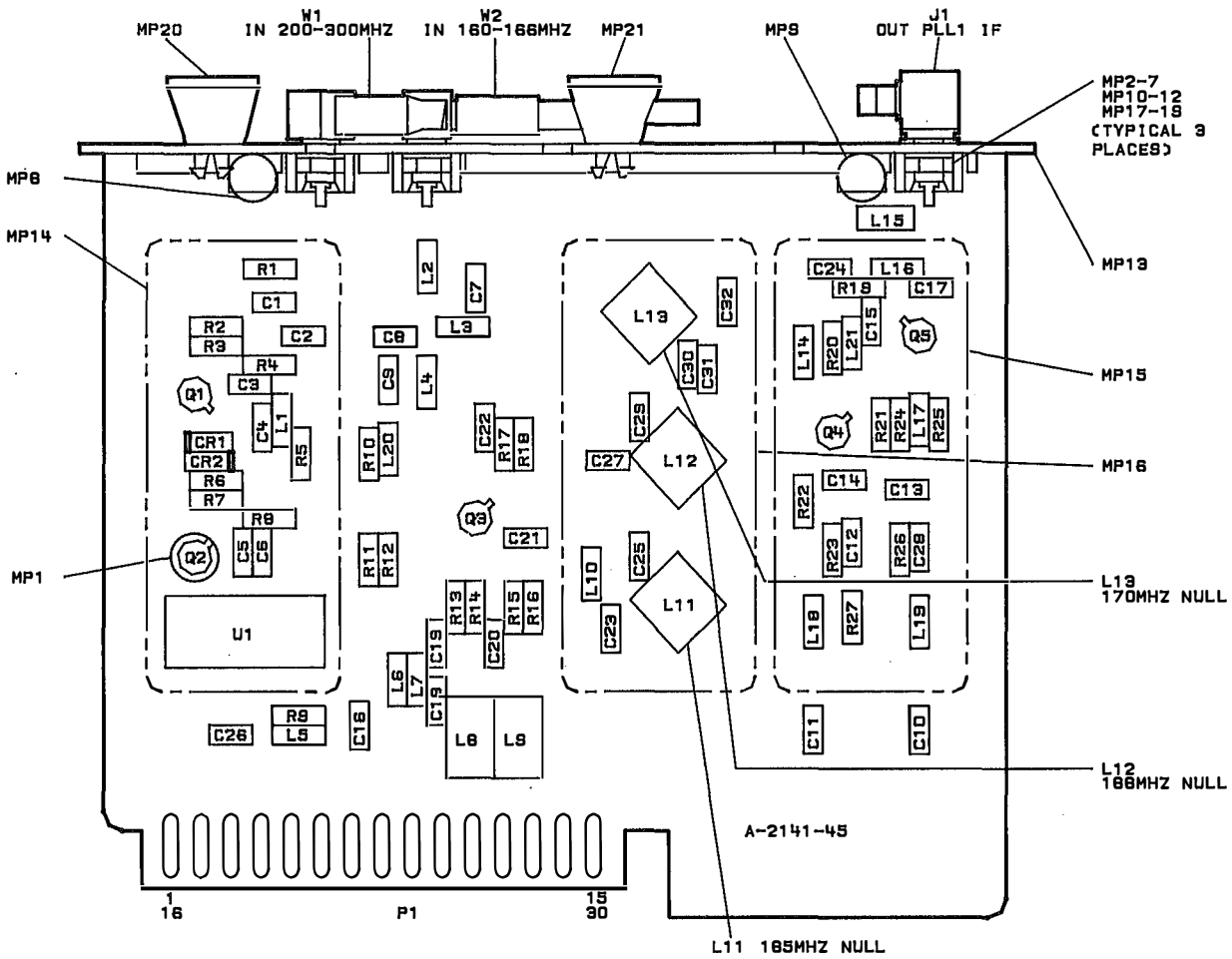

Figure 8C-17. A38 PLL1 IF, Component Location Diagram

A38 PLL1 IF, Pin I/O

A38

Pin	Mnemonic	Levels	Source	Destination
1	GND	0V	A62 STAR GND	*F
16	GND	0V	A62 STAR GND	*F
2	GND	0V	A62 STAR GND	*F
17	GND	0V	A62 STAR GND	*F
3	GND	0V	A62 STAR GND	*F
18	GND	0V	A62 STAR GND	*F
4	GND	0V	A62 STAR GND	*F
19	GND	0V	A62 STAR GND	*F
5	GND	0V	A62 STAR GND	*F
20	GND	0V	A62 STAR GND	*F
6	GND	0V	A62 STAR GND	*F
21	GND	0V	A62 STAR GND	*F
7	GND	0V	A62 STAR GND	*F
22	GND	0V	A62 STAR GND	*F
8	GND	0V	A62 STAR GND	*F
23	GND	0V	A62 STAR GND	*F
9	GND	0V	A62 STAR GND	*F
24	GND	0V	A62 STAR GND	*F
10	GND	0V	A62 STAR GND	*F
25	GND	0V	A62 STAR GND	*F
11	GND	0V	A62 STAR GND	*F
26	GND	0V	A62 STAR GND	*F
12	−10V	−10V	XA53P1-12, 13, 31, 32	*THRU A62L8 TD F
27	−10V	−10V	XA53P1-12, 13, 31, 32	*THRU A62L8 TD F
13	+12V UI ADJ	+10.5V	XA52P1-10	*THRU A62L5 TD F
28	+12V UI ADJ	+10.5V	XA52P1-10	*THRU A62L5 TO F
14	GND	0V	A62 STAR GND	*F
29	GND	0V	A62 STAR GND	*F
15	GND	0V	A62 STAR GND	*F
30	GND	0V	A62 STAR GND	*F

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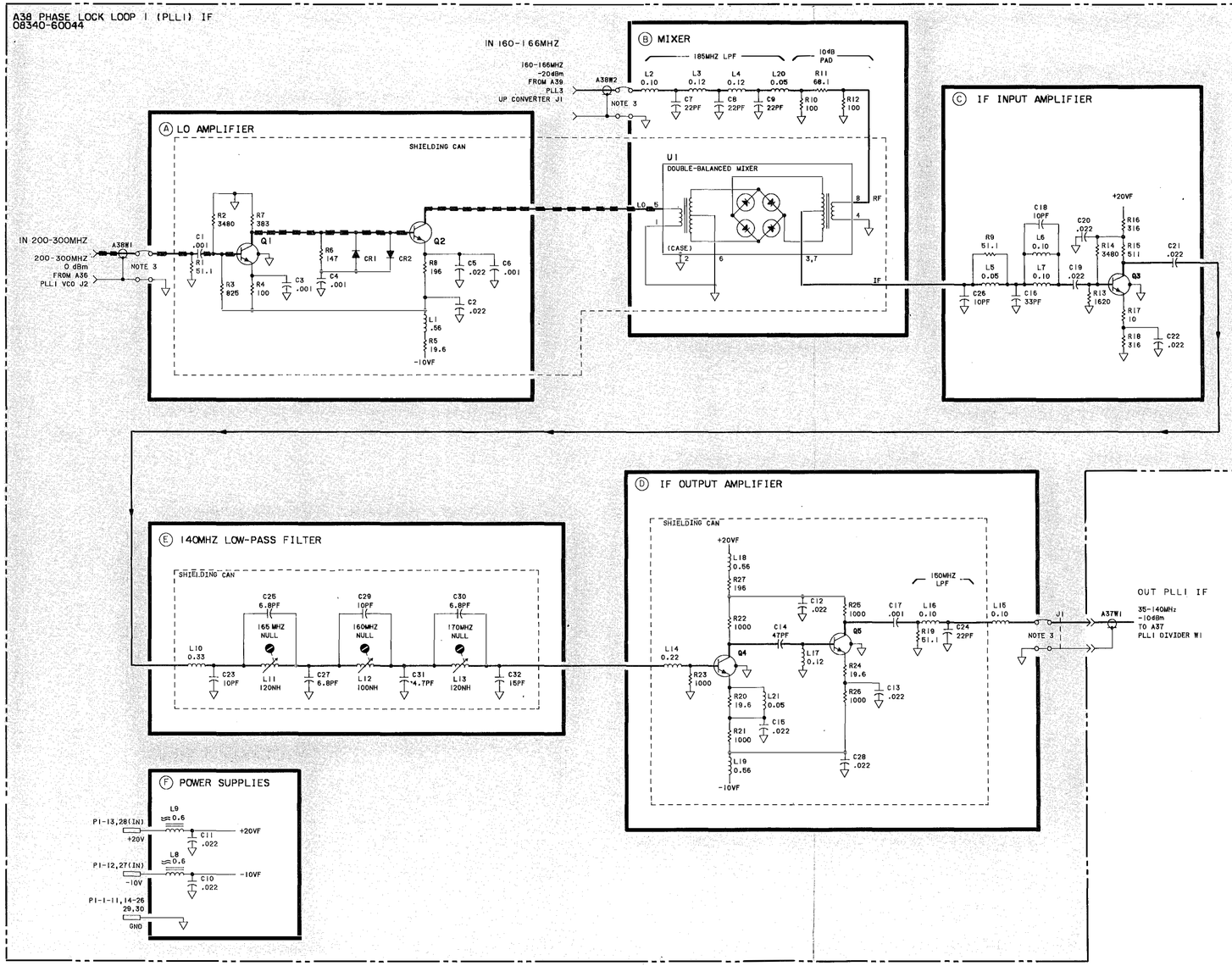


NOTES:

1. REFER TO THE SERVICE SECTION INTRODUCTION FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES SHOWN ARE IN OHMS,CAPACITANCE IN MICROFARADS,AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. J1,A38W1,AND A38W2 CENTER CONDUCTORS ARE ELECTRICALLY CONNECTED TO THE PC BOARD THROUGH SOLDERED 24 GUAGE FINE WIRES. THEIR OUTER CONDUCTORS ARE CONNECTED TO PC BOARD GROUND THROUGH MECHANICAL SCREW CONNECTIONS TO THE ASSEMBLY COVER PLATE.

Figure 8C-18. A38 PLL1 IF, Schematic Diagram

A39 PHASE LOCK LOOP 3 (PLL3) UPCONVERTER, CIRCUIT DESCRIPTION

INTRODUCTION

The function of the A39 Phase Lock Loop 3 Upconverter is to mix 160 MHz with the output of the A40 PLL 2 VCO (.15 to 6 MHz) and output the sum of the two frequencies. This is done using a phase-lock loop which has a closed loop bandwidth of approximately 10 kHz.

FREQUENCY MULTIPLIER (X 1.6) A

In order to offset the PLL2 output by 160 MHz, a 160 MHz reference signal must be generated. The frequency multiplier x 1.6 generates 160 MHz by dividing the 100 MHz input reference signal by five and then selecting the eighth harmonic.

U3 is an ECL bi-qinary counter that is connected so that the output skips one pulse every five input counts as can be seen from the waveforms in Figure 8C-19.

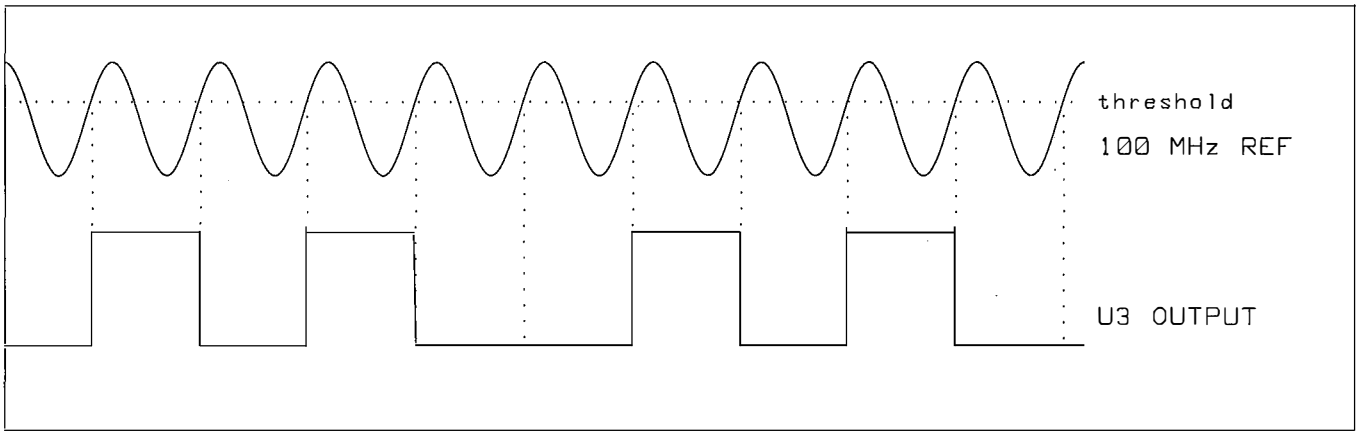


Figure 8C-19. A39 PLL3 Frequency Multiplier Waveforms

The net effect of the pulse skipping is to produce a double narrow pulse (refer to Q3 output in figure 8C-19) at a 20 MHz rate. This gives better results than simply dividing the 100 MHz reference by 5 to obtain a 20 MHz pulse train because the narrower pulses generate stronger harmonics than a 20 MHz pulse train would.

The 160 MHz bandpass filter selects the 160 MHz signal that is amplified by Q5. L18, C49 and C50 form a tank circuit that is tuned to 160 MHz which also helps to reject unwanted frequency components from the output of U3.

R46, R47 and R48 form a 5 dB pad keeping the distortion down in the mixer by providing a better 50 ohm match to the mixer input.

MIXER B

U7 is a double-balanced mixer which operates with about +7 dBm of LO power and approximately -20 dBm of RF signal power at 160 MHz. The desired output is the difference frequency and lies between 150 kHz and 6 MHz.

IF AMPLIFIER C

The output of the mixer U7 is filtered by an 8-section elliptic 10 MHz Low Pass filter which must reject 14 to 20 MHz, and other higher frequencies. The filter output is amplified by Q3.

160 TO 166 MHz VCO D

The 160 to 166 MHz VCO uses Q1 in a Colpitts configuration. The tank circuit is formed by L11, C33, C36, C37 and CR3 (a varactor diode). C33 and C36 provide a capacitive divider for the signal that is fed back into the emitter of Q1. L11 is adjustable allowing the center of the VCO tuning range to be varied.

Q2 is connected in a common base configuration and is used by PLL1 as a buffer amplifier for the 160-166 MHz output. Q4 is connected in a common emitter configuration and is used as a buffer amplifier for the 160-166 MHz signal that drives the LO port of the mixer.

PHASE/FREQUENCY DETECTOR E

The PHASE/FREQUENCY DETECTOR generates a differential output signal that is used by the LOOP AMPLIFIER (Block F) as well as the PHASE LOCK INDICATOR (Block G). The main components of the PHASE/FREQUENCY DETECTOR consist of two ECL flip-flops and three ECL NOR gates.

U6B and U6C generate ECL level inputs for the flip flops from the two frequencies to be compared. R25 and R26 center the input frequency signals to the midpoint of the ECL logic level thresholds so the PHASE/FREQUENCY DETECTOR will be less sensitive to amplitudes of the two comparison frequencies.

The SET inputs to both flip-flops are tied together and are driven by the output of the NOR gate U6A. Whenever the non-inverted outputs of the flip-flops are both low the SET lines on both flip-flops are asserted and the non-inverted outputs of the flip-flops will both go high.

As can be seen in Figure 8C-20, when one of the clock inputs goes high, the corresponding non-inverting output will go low and remain low until the other clock input goes high which sends the other non-inverting input low. Once both non-inverting outputs are low, the SET inputs will be asserted as previously described and both non-inverting outputs will go high until the next clock pulse is received.

When the inputs are out of phase the non-inverting outputs will differ. The non-inverting output with the longer negative going pulse corresponds to the input that is leading in phase. When the inputs are locked together the non-inverting outputs will both be high with low narrow pulses coincident with the input rising edge. The width of the narrow pulses correspond to the propogation delays of the NOR gate (U6A) and the flip-flops.

LOOP AMPLIFIER F

The phase detector differential outputs are the inputs to the LOOP AMPLIFIER. Each of the differential inputs is passed through identical low-pass filters (R5, R9, C2, R6, R10, and C3). C9, R16, C8, and R17 provide a large dc gain for the loop amplifier while insuring that each of the differential inputs see the same impedance over all frequencies. R14, R15 and C7 form an ac voltage divider which sets the loop bandwidth to about 10 KHz and limits the amount of noise introduced by U2.

The output of the divider goes to the varactor diode (CR3 in Block D) and tunes the VCO.

R18, CR4 and CR5 reduce the charging time of C7 whenever the frequency is abruptly changed.

If the VCO is tuned to a frequency that is lower than the 160 MHz reference frequency (Block A), the mixer output frequency still is equal to the difference of the two input frequencies but the loop will provide positive feedback instead of negative feedback and will drive the VCO to the low end of its frequency range. U1B prevents the VCO tune voltage from latching at a positive value by sensing when the voltage goes above 0 volts. When this occurs, the output of U1B pulls the tune voltage down to the proper lock range. R13 provides hysteresis to allow time for the loop to lock. CR2 prevents the output of U1B from interfering with the VCO when it is tuned to the correct side of 160 MHz.

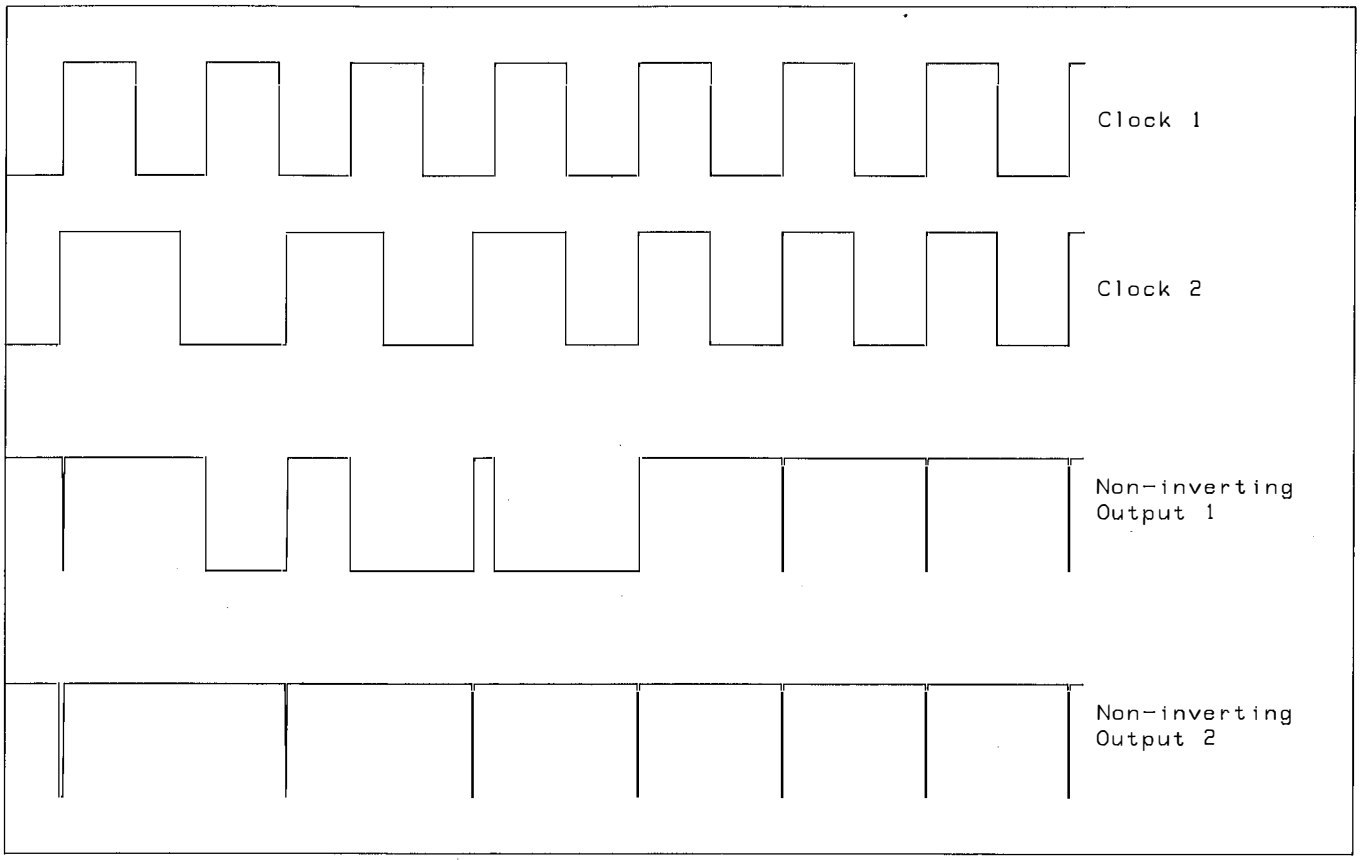


Figure 8C-20. A39 PLL3 Phase/Frequency Detector Waveforms

PHASE LOCK INDICATOR G

The PHASE LOCK INDICATOR senses the outputs of the PHASE DETECTOR to determine when the loop is locked. The non-inverting outputs of the phase detector flip-flops are attenuated by R23 and summed into the inverting input of U1A. The inverted outputs of the flip-flops are tied together (wire-or) and input to the non-inverting input of U1A. C1 filters out the high frequency components of the flip-flop outputs so the phase lock indicator is looking at the average voltages on each input. When the inverting input of U1A is more positive than the non-inverting input, the indicator will show that a phase locked condition occurs by lighting DS1 and outputting a TTL low level signal for HUL1.

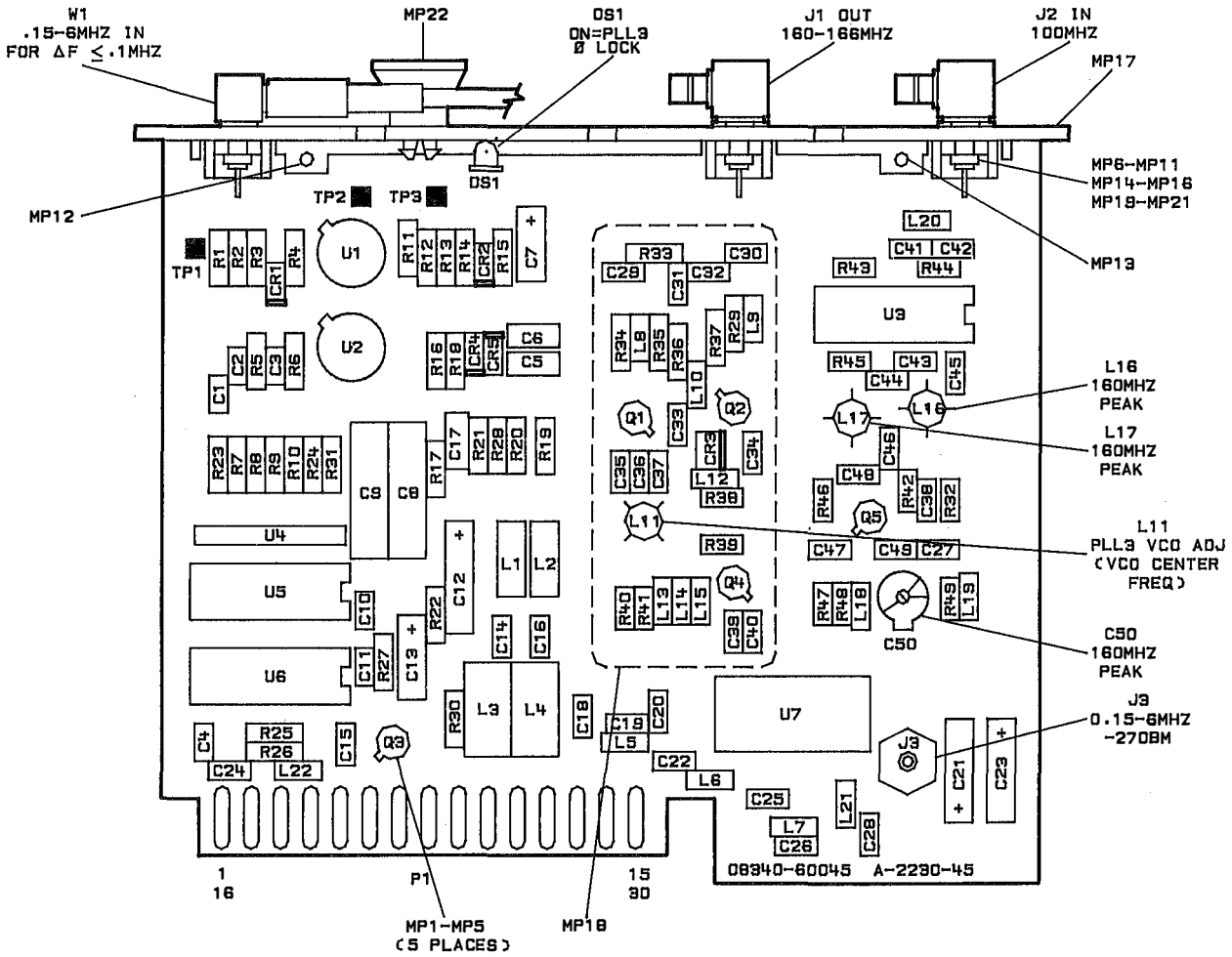


Figure 8C-21. A39 PLL3 Upconverter, Component Location Diagram

A39 PLL3 Upconverter, Pin I/O

A39

Pin	Mnemonic	Levels	Source	Destination
1 16	HUL1 HUL1	TTL (HIGH TRUE) TTL (HIGH TRUE)	*G *G	XA59P1-106 XA59P1-106
2 17	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
3 18	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
4 19	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
5 20	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
6 21	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
7 22	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
8 23	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
9 24	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
10 25	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
11 26	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
12 27	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32, XA53P1-12, 13, 31, 32	*THRU A62L4 TD H *THRU A62L4 TD H
13 28	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
14 29	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
15 30	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*THRU A62L3 TD H *THRU A62L3 TD H

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

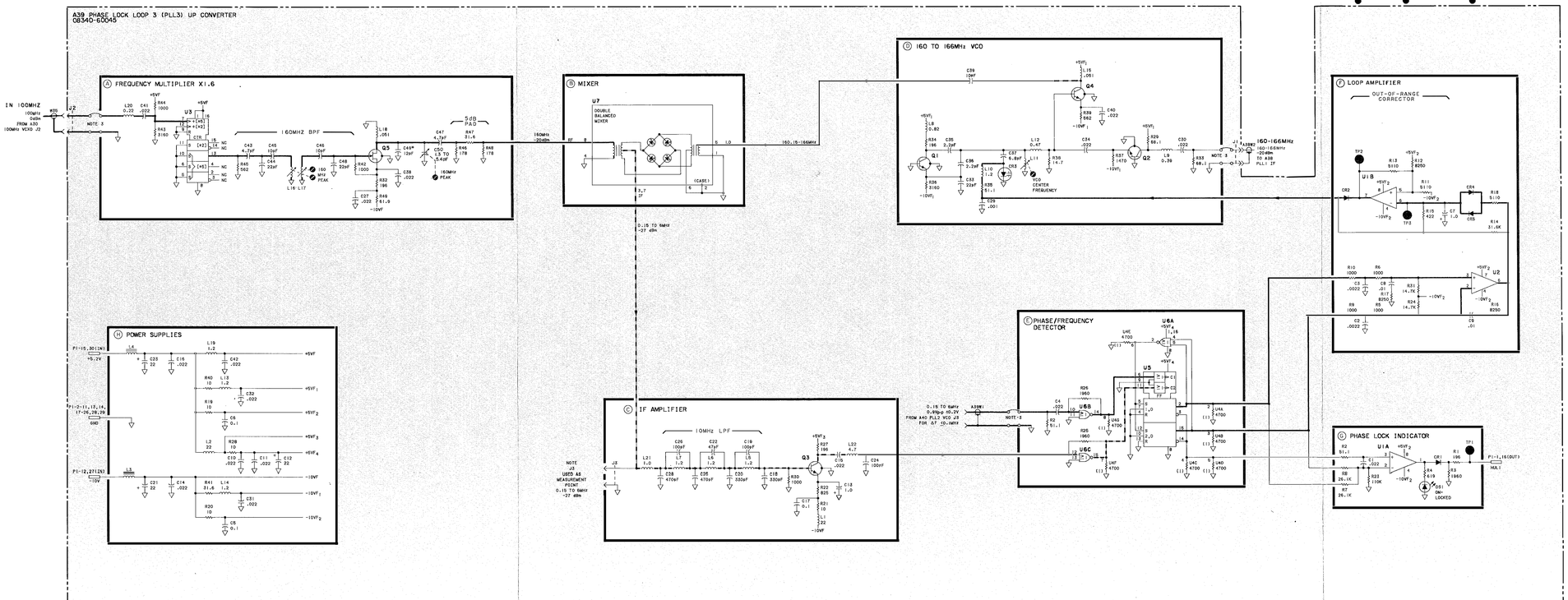


Figure 8C-22. A39 PLL3 Upconverter, Schematic Diagram

A40 PHASE LOCK LOOP 2 (PLL2) VCO, CIRCUIT DESCRIPTION

INTRODUCTION

The A40 Phase Lock Loop 2 VCO assembly accepts a tuning current from the A43 PLL 2 Discriminator board to adjust the VCO frequency between 150 and 75 MHz. The output of the VCO is sent to the A42 PLL2 Divider and also is divided by 500 and sent to the A43 PLL2 Discriminator. In addition an output is sent to the A39 PLL3 Up Converter that is divided by either 25 or 500, depending on the sweep width selected.

BIAS NETWORK/50 kHz LOW PASS FILTER A

C1, C2, C3, L1, and L2 form a low pass (Chebyshev) filter. Although the cut-off frequency is 50 kHz the input frequencies (from the A43 PLL2 Discriminator board) to be rejected will normally be between 150 kHz to 300 kHz. The input signal is a current (1 to 9 mA). The filter is in series with the tuning current to minimize the effects of hum. Any stray signals coupled to the filter inductors will appear as a series voltage signal. Since the tuning current comes from a current source on the A43 Discriminator, it will be unaffected by any voltage fluctuations on the inductors.

The VCO tuning voltage at TP1 in VCO (Block B) is a function of the current from the A43 PLL2 Discriminator flowing through the equivalent resistance of R1-R5, which is essentially a current to to voltage converter. The tuning current passes through the 50kHz filter and into R1-R5. Since the varactors CR1-CR4 are reverse biased, negligible current is flowing through L3.

At the minimum tuning current, the varactor bias is set by R2 (150 MHz ADJUST). This functions as a VCO offset adjustment. As tuning current from the A43 PLL2 Discriminator increases, it forces the tune voltage in a positive direction, proportional to the setting of R4 (100 MHz ADJUST). This functions as the VCO gain adjustment, which is set to yield about -10 MHz/mA sensitivity. These adjustments are normally made with the loop phase-locked. When phase-locked, the VCO frequency will exactly equal the programmed frequency, so rather than adjusting for a frequency indication, the adjustments are made by monitoring the tuning voltage on the A43 PLL2 Discriminator and setting the end points to the appropriate voltages.

Transistors Q5 and Q6 and associated components form a low

impedance filtered -32V source to bias the VCO varactor tuning diodes. Q5 and Q6, in a darlington configuration, minimize the fluctuations in base drive requirements as the tuning current is varied. Any fluctuations in base current cause a long time-constant change in the -32V output level due to the large resistors and capacitors in the base circuit.

VCO B

The VCO is a varactor tuned oscillator which tunes from 75 to 150 MHz. Varactors CR1, CR2, CR3, and CR4 form a series resonant circuit with L4 and L5. Figure 8C-23 shows the oscillators equivalent circuit. This series circuit connects the emitters of Q1 and Q2. Q2 is a common-base amplifier whose load impedance is made up primarily of L9, R14, and R15. The voltage across the load is coupled to the base of emitter-follower Q1, which drives the series resonant circuit. There is no phase inversion through Q2 emitter-to-collector or through Q1 base-to-emitter; therefore, the feedback signal is in phase with the input signal.

The load for the VCO is dependent upon Q4 in 75-150 MHz Output Buffer (Block **C**) and Q3 in Frequency Dividers (Block **D**) providing low input impedances. In the normal case, R14 and R15 dominate. If Q3 or Q4 are defective, the VCO may not oscillate since its load will no longer be dominated by R14 and R15.

75-150 MHz OUTPUT BUFFER C

Q4 is a grounded-base amplifier which isolates the VCO from the load circuits. The output of Q4 is filtered, attenuated, and used to drive the A42 PLL2 Divider.

A 13 dB attenuator (R20, R21, and R22) is used to reduce the output signal level and thus reduce the possibility of coupling this signal into other circuits. A pre-amplifier on the A42 PLL2 Divider returns the signal to the appropriate level. This signal path is used during phase-locking only, so its response below 100 MHz is not important since PLL2 is only programmable to phase-lock frequencies between 100 MHz and 150 MHz.

FREQUENCY DIVIDERS D

Q3 isolates the VCO from the dividers and develops the required drive voltage. All of the dividers and gates are ECL with Vcc connected to +5V and Vee grounded. As shown in Figure 8C-24, U3 divides the VCO frequency by 5 to obtain 15 to 30 MHz. U6C provides isolation. U2 divides by 5 to obtain 3 to 6 MHz. U2 then further divides by 2 and U1 divides by 10, so the output of U1 is 0.15 to 0.30 MHz. The output of U1 is fed to the A43 PLL2 Discriminator.

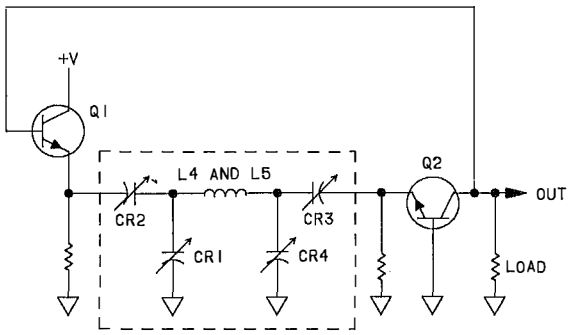


Figure 8C-23. Equivalent VCO Resonant Circuit

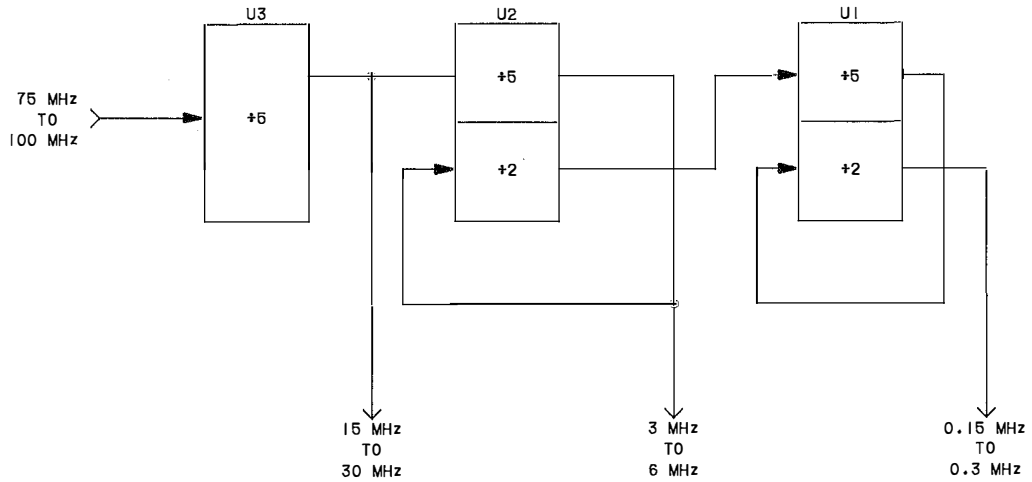


Figure 8C-24. Simplified Divider Circuit

SMALL DELTA F SWITCH E

U5 functions as a single-pole double-throw switch, routing either 3 to 6 MHz from U2 or 0.15 to 0.30 MHz from U1, to the A39 PLL3 Up Converter. The required range is selected by a TTL signal (SW2 from the A42 PLL2 Divider) on P1-22. R33 and R34 shift the TTL levels to ECL levels.

For 20-30 loop sweeps between 5 kHz and 100 kHz, SW2 is a TTL HIGH and the 3 to 6 MHz divider output is routed to the A39 PLL3 Up Converter. For sweeps less than 5 kHz, SW2 is a TTL LOW, selecting the 0.15 to 0.30 MHz output.

0.1-5 MHz DELTA F SWITCH F

For delta F or sweep widths of 0.1 to 5 MHz, the 15 to 30 MHz output is used. The output of U3 in Frequency Dividers (Block **D**) is routed through U6D, U7D, and T1. This combination serves as a switch with 90 dB of isolation in the off state. The TTL signal (SW1 from the A42 PLL2 Divider) on P1-24 controls this switch.

For maximum isolation, the two gates (U6D, U7D) are contained in separate packages. Any stray signals that do reach the output will be a common-mode input to transformer T1. Since T1 will only respond to differential mode signals from U7D, these common-mode signals will be rejected.

C25 and L14 filter the output to reduce spurious responses.

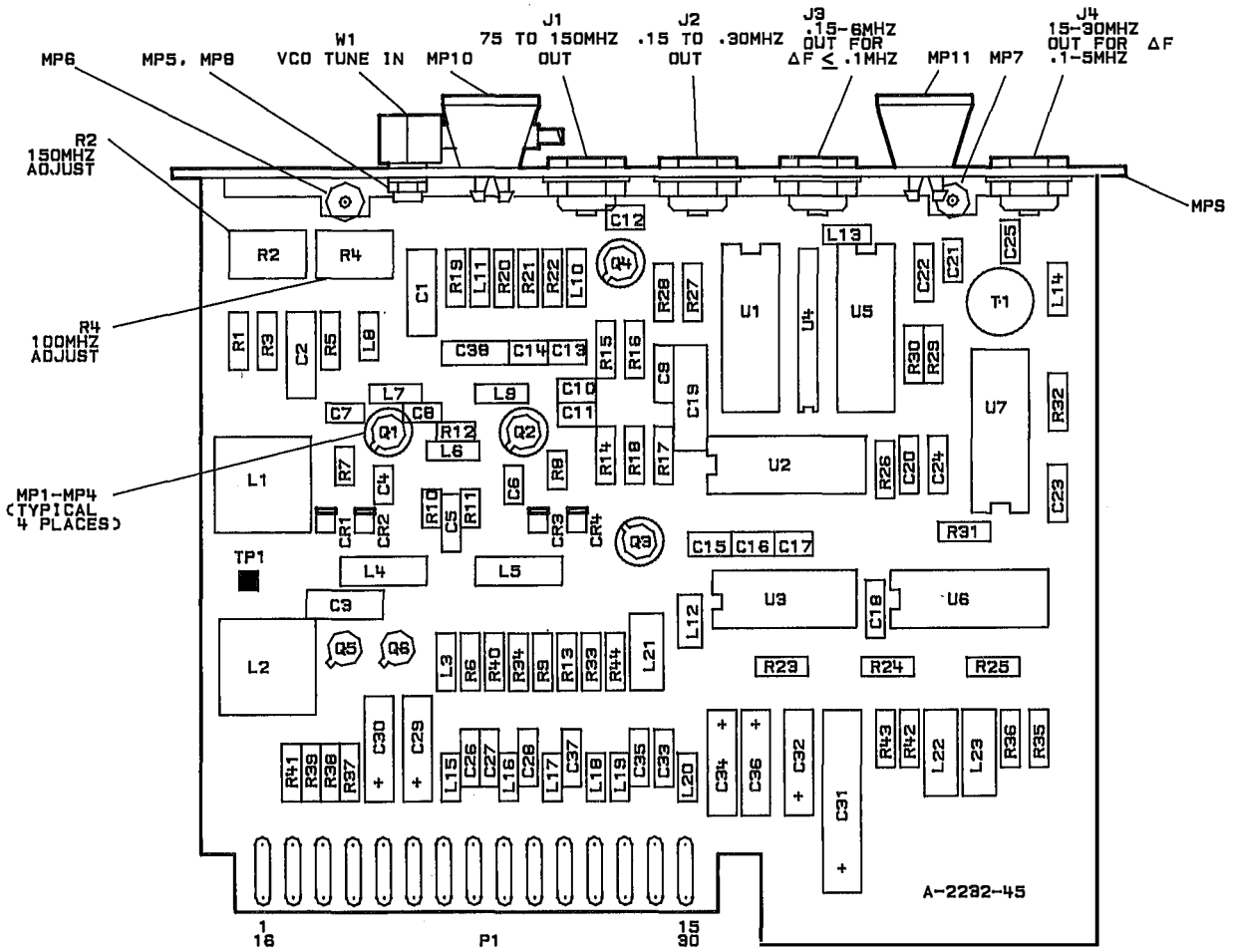


Figure 8C-25. A40 PLL2 VCO, Component Location Diagram

A40 PLL2 VCO, Pin I/O

A40

Pin	Mnemonic	Levels	Source	Destination
1 16				
2 17	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
3 18	GND	0V	A62 STAR GND A62 STAR GND	*G
4 19	GND	0V	A62 STAR GND A62 STAR GND	*G
5 20	GND	0V	A62 STAR GND A62 STAR GND	*G
6 21	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
7 22	SW2	TTL	XA42P1-14	E
8 23				
9 24	SW1	TTL	XA42P1-32	*F
10 25	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
11 26	−40V/−40V SENSE (−) −40V/−40V SENSE (−)	−40V −40V	XA53P1-11, 30/XA53P1-23 XA53P1-11, 30/XA53P1-23	*A *A
12 27	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*G *G
13 28	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*G *G
14 29	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
15 30	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*G *G

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

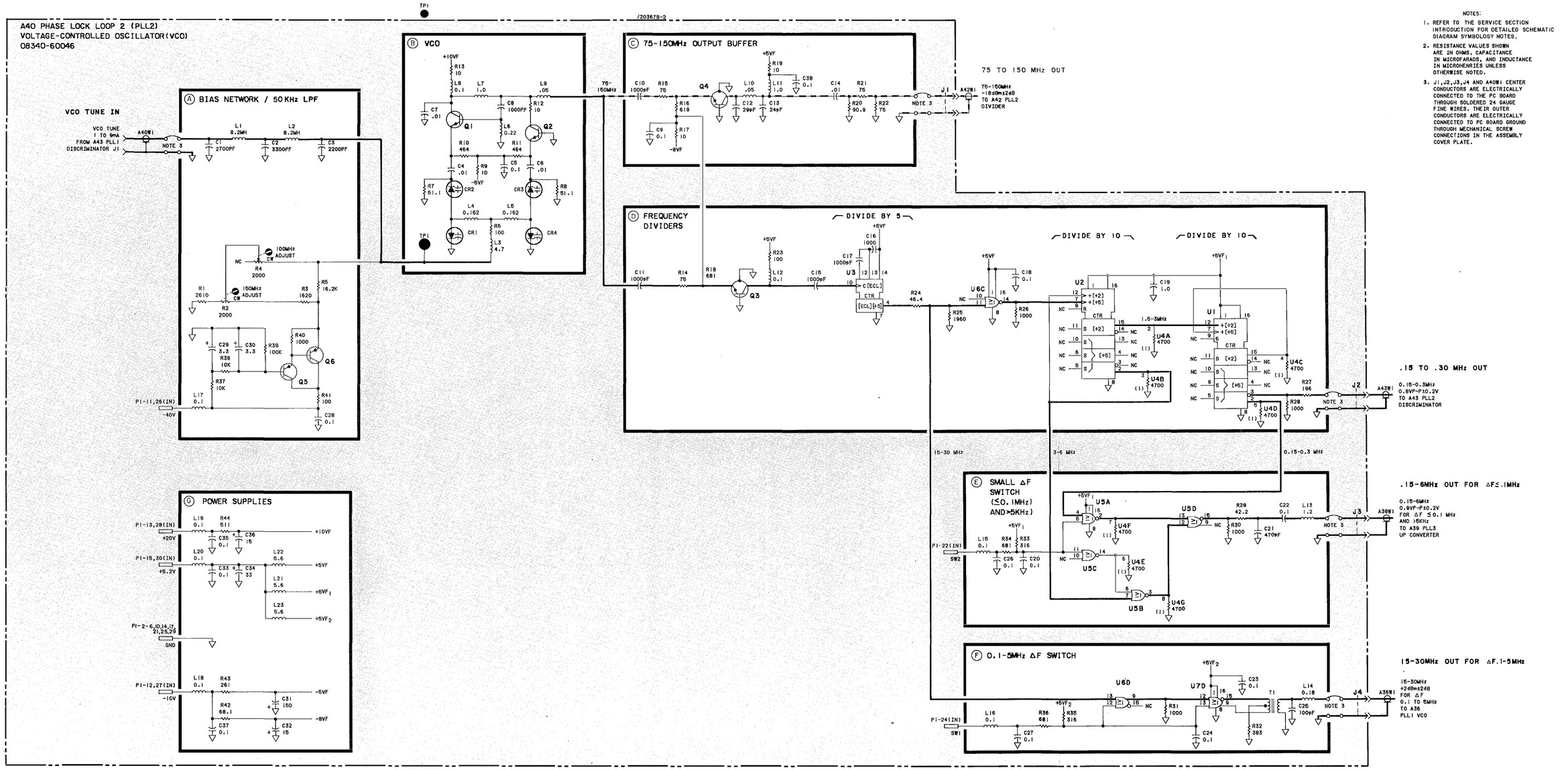


Figure 8C-26. A40 PLL2 VCO, Schematic Diagram

A41 PHASE LOCK LOOP 2 (PLL2) PHASE DETECTOR, CIRCUIT DESCRIPTION

INTRODUCTION

The purpose of the A41 PLL2 Phase Detector is to compare the phase of the A40 PLL2 VCO output signal (after division by N2 on the A42 PLL2 Divider) to a 500 kHz Reference signal (10 MHz from the A29 Reference Phase Detector divided by 20 on the A42 PLL2 Divider). The phase difference is converted to an error voltage used to fine-tune the sensitivity of the PLL2 Discriminator thereby correcting the PLL2 VCO frequency.

PHASE-FREQUENCY DETECTOR A

The Phase-Frequency Detector responds to the difference in phase between the 500 kHz reference input, P1 pin 20 (10 MHz from the A29 Reference Phase Detector divided by 20 on the A42 PLL2 Divider) and the 75 to 150 MHz from the A40 PLL2 VCO divided by N2 on the A42 PLL2 Divider board (P1 pin 19). Assuming both flip-flops U6A and U6B have been cleared, Q9 is ON and Q10 is OFF. Q9 supplies about 3 ma current which is sunk by current source Q8, resulting in approximately zero current flow through the 50 kHz low-pass filter (LPF) consisting of C2, L1, and C3. C4 is used to stabilize the two grounds between the sample and the hold modes.

Q8 is ON when High Lock Enable (HLE2) is HIGH.

A pulse from the PLL2 Divider, on P1 pin 19 clocks the Q output of U6A pin 5 HIGH turning Q9 off. With both Q9 and Q10 off, Q8 will sink current out of the 50 kHz LPF. A subsequent reference pulse on P1 pin 20 clocks the Q output of U6B pin 9 HIGH which immediately resets both flip-flops through U7A. Thus the effect of a pulse at P1 pin 19 leading one at P1 pin 20 is to route current from the 50 kHz LPF into Q8, momentarily reducing the current flow into the 50 kHz LPF.

Similarly, if the reference phase leads the divided input phase, Q9 current will be sunk by Q8 and Q10 current will be routed through the 50 kHz LPF, momentarily increasing the current flowing into the 50 kHz LPF. A net current flow into the LPF will cause the voltage at TP1 to decrease.

If the two inputs have different frequencies, the pulse relationships become complicated, but the net effect is a negative voltage at TP1 if the divided output frequency (P1 pin

19) is higher than the 500 kHz Reference (P1 pin 20).

U3 serves as an amplifier to provide the high currents necessary to rapidly charge the integrating capacitor C7 in the following stage in the ANALOG INTEGRATOR/SAMPLE AND HOLD (Block **C**). VR2 and VR3 serve as clamps, limiting the output swing to ±5.8V.

HLE2 (P1 pin 2) controls U6A and Q8. During sweep mode Q8 is OFF, U6A is set, shutting OFF Q9. HLE2 also goes to the A42 PLL2 Divider shutting OFF the 500 kHz input to U6B. With the 500 kHz input OFF , U7A forces U6B to reset which causes Q10 to shut OFF. With Q8, Q9, and Q10 all OFF, the voltage at TP1 during a sweep is forced to zero volts. This prevents any negative voltage from turning Q3 ON, and changing the charge stored on C7.

DIGITAL INTEGRATOR B

The error voltage necessary to phase-lock the loop must be sampled, and then held very constant during a sweep to preserve frequency accuracy at the end of sweep. If the entire error correction were to be retained in the analog integrator, it would require very low-leakage components to avoid a droop at the end of sweeps. Instead, the digital integrator is used to store the majority of the error voltage, and the analog integrator is left with a much less significant portion.

When the analog error voltage (TP3 in ANALOG INTEGRATOR/SAMPLE AND HOLD, Block **C**) goes below -4.7V, Q5 is turned ON and its collector voltage is pulled down to -1.4V. At this point, CR4 and CR3 become forward biased, clamping U2 and preventing further negative movement of TP3. Simultaneously, the input of U7B will have been pulled LOW, which turns ON a 2 kHz oscillator made up of U7C, R20, and C11. This clocks the count up input of counters U8 and U9, which drives DAC U10. U10 sources negative current to the summing junction of U4 in OUTPUT AMPLIFIER (Block **D**) and this current increases in magnitude as U8 and U9 count up. When the current reaches a value which tunes the VCO to the proper frequency the voltage at TP3 moves positive, shutting OFF the oscillator. An analogous sequence occurs when the analog error voltage (TP3) rises above +6.4V. This occurs during the phase-lock interval, before the sweep begins. During the sweep, any drop in the remaining analog error voltage is insignificant, since the UP-DOWN counters, U8 and U9, contain the majority of the error correction in digital form.

ANALOG INTEGRATOR-SAMPLE AND HOLD C

U2 and C7 form an integrator which integrates current flowing from U3 in Phase/Frequency Detector (Block **A**) through R8. The

output of the integrator is summed with other signals in U4 of OUTPUT AMPLIFIER (Block **D**) and ultimately controls the VCO frequency. In steady state conditions, TP3 will settle to a constant voltage which tunes the VCO to the correct frequency. If the voltage at TP3 is constant, the integrator's input current must be zero, so opening the Sample and Hold FET switch Q3 will not change the voltage at TP3. When PLL2 is being used in its swept mode, the loop is locked to a start frequency set by A42 PLL2 Divider, then Q3 is opened. This breaks the lock loop, permitting a sweep to be executed.

Q3 is closed with zero gate voltage, and open with -7V on the gate. The gate drive comes from Q6 and Q7, which translates the TTL HLE2 signal level on P1 pin 2 to the 0/-7V levels. P1 pin 2 also controls U6A and Q8 in the Phase/Frequency Detector (Block **A**).

OUTPUT AMPLIFIER D

U4 serves to sum signals from the analog integrator, the digital integrator, and R11. R11 is a high frequency signal path that bypasses the slow responding integrators, and speeds up the phase locking process. U4, C8, C9, R12, and the internal 10K ohm resistor in U10 of DIGITAL INTEGRATOR (Block **B** between pins 1 and 16) form an active 3kHz low-pass filter.

The output of U4 is the tuning voltage that goes to the A43 PLL2 Discriminator board, and effectively changes the gain of the discriminator to tune the PLL2 VCO frequency.

UNLOCK INDICATOR E

When the phase lock loop is in a steady state condition (locked), the voltage at TP1 in the PHASE/FREQUENCY DETECTOR (Block **A**) is zero. If unlocked, the voltage will not be zero except for transients passing through zero. When the voltage exceeds $\pm$3V, either Q1 or Q2 is turned ON, discharging C15 or C14 respectively and tripping comparator U1 (notice opposite polarity voltage on C14 and C15). When the voltage settles to less than $\pm$ 3V, the appropriate capacitor must recharge before the comparator is reset , essentially holding the unlocked condition. Recharging takes about 1 ms so the unlocked condition is held long enough for the processor to recognize it. Comparator U1 output is a TTL HIGH for an unlock condition.

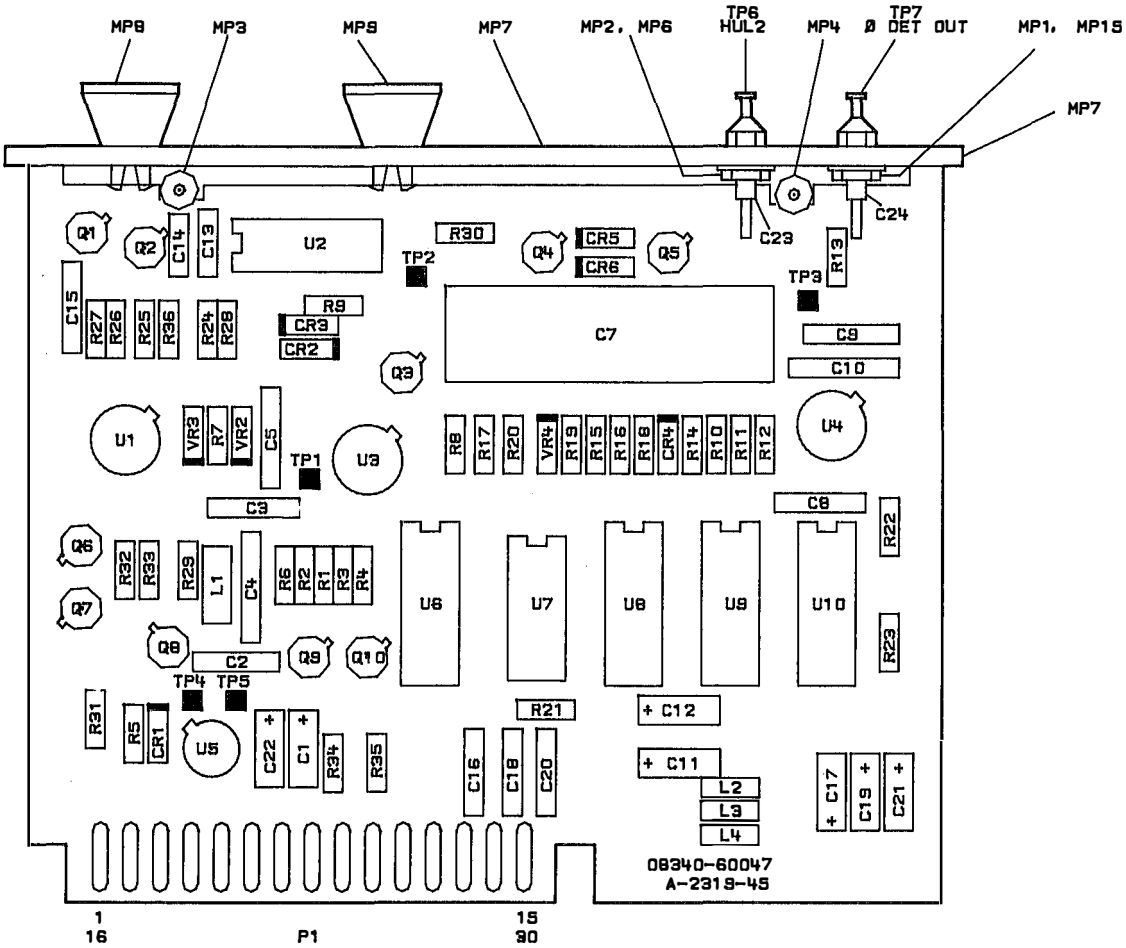


Figure 8C-27. A41 PLL2 Phase Detector, Component Location Diagram

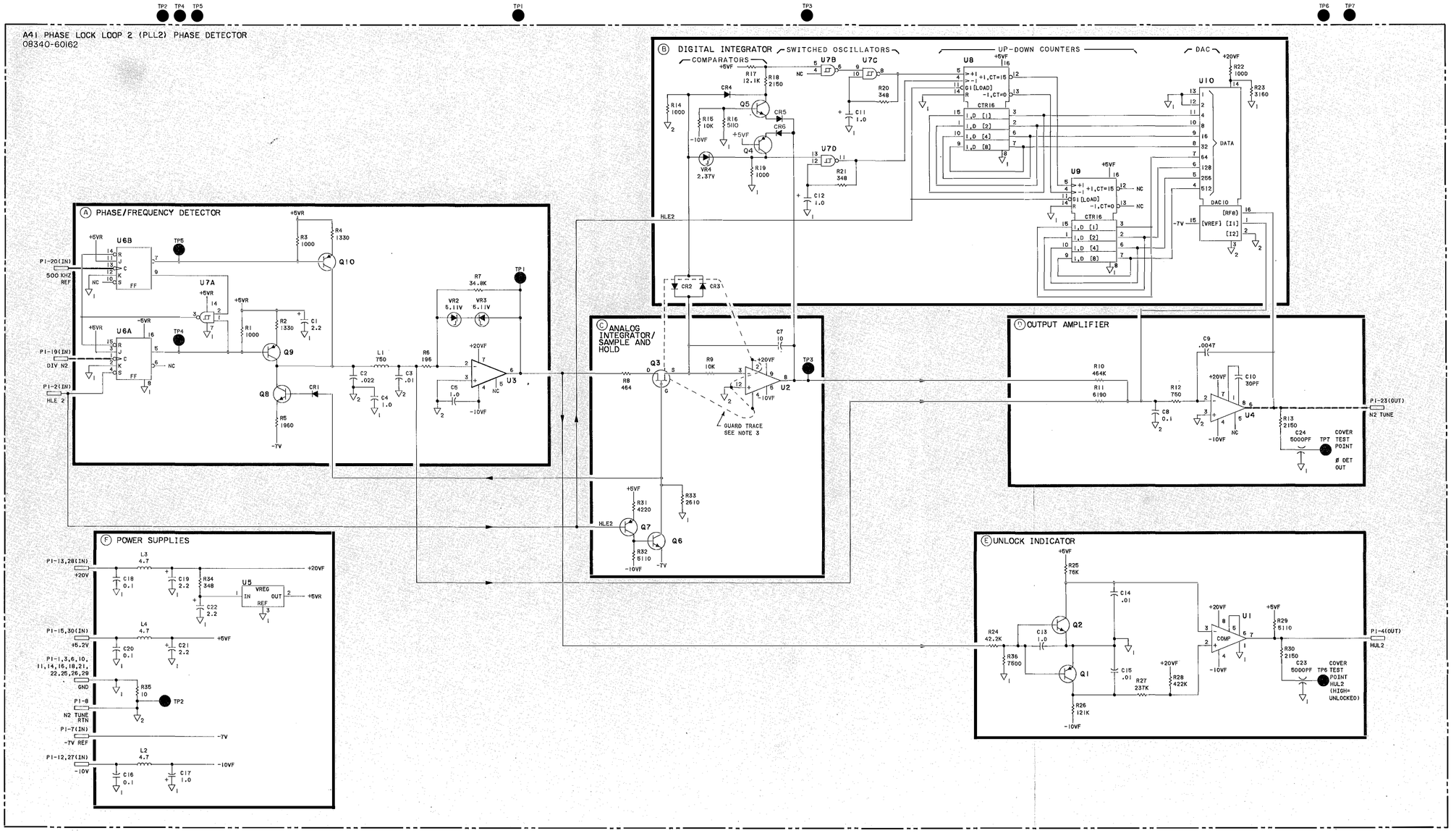
A41 PLL2 Phase Detector, Pin I/O

A41

Pin	Mnemonic	Levels	Source	Destination
1 16	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
2 17	HLE2	TTL (HIGH TRUE)	XA59P1-53	*A B C
3 18	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
4 19	HUL2 DIV N2	TTL (HIGH TRUE) TTL (LOW TRUE)	E XA42P1-27	XA59P1-107 A
5 20	500 KHZ REF	TTL	XA42P1-9	A
6 21	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
7 22	−7V REF GND	−7V 0V	XA43P1-9 A62 STAR GND	F *F
8 23	N2 TUNE RTN N2 TUNE	0V 0 TO +7 VOLTS	F D	XA43P1-10 XA43P1-28
9 24				
10 25	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
11 26	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
12 27	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*F *F
13 28	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*F *F
14 29	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
15 30	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*F *F

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.



NOTES:
1. REFER TO THE BEGINNING OF SECTION VIII FOR DETAILED SCHEMATIC DIAGRAM NOTES.
2. RESISTANCE VALUES ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. PINS 2 AND 4 OF OP AMP PACKAGE U2 HAVE NO INTERNAL CONNECTION TO THE OP AMP CIRCUIT. THE GUARD TRACE IS ELECTRICALLY CONNECTED TO U2 PINS 2, 4, AND 12.

Figure 8C-28. A41 PLL2 Phase Detector, Schematic Diagram

A42 PHASE LOCK LOOP 2 (PLL2) DIVIDER, CIRCUIT DESCRIPTION

INTRODUCTION

The PLL2 Divider Board has two functions:

- Generate the 500 kHz reference signal which is used by the PLL2 Phase Detector Board. This is accomplished by dividing the 10MHz quartz crystal reference oscillator by 20.

- Divide the PLL2 VCO output signal A42W1 (which can range from 100 to 150 MHz when not sweeping) by some number between 200.01 and 300 so that the resulting frequency is 500 kHz.

The two signals above are sent to the PLL2 Phase Detector board so that phase lock can be achieved.

The circuit which performs the first function is explained in REFERENCE DIVIDER (Block **D**). The remaining circuitry on the PLL2 Divider board performs the second function. Refer to Figure 8C-29 for a simplified block diagram of this section of the PLL2 DIVIDER.

Refer to the "Frequency Range and CW Mode Accuracy" Performance Test for use as a troubleshooting aid.

LATCHES A

Latches U12, U13, and U14 store the BCD numbers used to preset the various counters on the PLL2 Divider board. The schematic (Figure 8C-32) shows the relationship of each output line to the frequency of the PLL2 VCO. The frequency of the VCO can be determined by adding the total of each individual output's contribution (if the output is HIGH) and subtracting that total from 150 MHz. For example, if U14 pin 10 and U14 pin 2 are both HIGH and all the other outputs of U14 as well as U2 and U13 were LOW the total contribution would be 40 MHz + 5 MHz = 45 MHz. The frequency of the PLL2 VCO would then be 150-45 = 105 MHz.

U14 pin 12 and U14 pin 15, SW1 and SW2 respectively, are routed to the PLL2 VCO board and are used for control.

REFERENCE DIVIDER D

A 10 MHz signal derived from the quartz crystal reference oscillator is amplified by Q2 and used to drive divider U4. The

divide by 10 output of U4 drives U16, whose divide by 2 output goes to the A41 PLL2 Phase Detector. This 500 kHz signal is used as a reference to which the programmable divide output of the PLL2 Divider is compared. The TTL input on P1-2 (HLE2) disables the reference divider during sweeps.

There are five main blocks to the programmable fractional divider which divides the output of PLL2 VCO. They are:

- PRESCALER
- DIRECT DIVIDER
- INTEGER COUNTER
- FRACTIONAL COUNTER
- SYNCHRONIZER

PRESCALER E

The -18 dBm, 75-150 Mhz input from A40 PLL2 VCO, is amplified by Q1 and used to drive prescaler U1A. The prescaler is a selectable divide by 10 or divide by 11 device. In terms of pulses, if the LSWALLOW line is LOW the device is in the divide by 11 mode; that is it takes 11 input pulses to produce 1 output pulse. If the LSWALLOW line is HIGH (divide by 10 mode) then it requires 10 input pulses to produce 1 output pulse. The divide by 11 mode can be thought of as a ``pulse swallowing'' mode since it requires one more pulse than the divide by 10 mode to produce the same output pulse. The output of the prescaler after being converted to TTL signal levels by U1B and buffered by U9C becomes the clock signal for all the other circuits of the fractional divider. Everything is referenced to this clock signal.

DIRECT DIVIDE B

The direct divide block contains two presettable counters U8 and U15 followed by two flip flops U10A and U10B. The direct divide block determines the number of clock pulses in a cycle. A cycle being the time from one LRESET pulse to the next. The Q and Q not outputs of U10A (pin 5 and 6) are the divided output signal and LRESET signal respectively. It should be noted that the frequency of the divided output signal (and the LRESET pulse) is always 500 kHz (when the PLL2 loop is locked) because it is this signal that is phase locked to the 500 kHz Reference signal. The frequency of the input signal (PLL2 VCO output) will change with changes in divide number.

The number of clock pulses in a cycle is determined by the number

sent to the presettable counter U8. U15 is also presettable but is always preset to 0 (U15 is most significant digit). U9B produces a HIGH output at a U8 and U15 count of 25 but because four additional clock pulses are required for this signal to get through U10B and U10A the cycle lasts for four more clock pulses. So, if the counter was preset to 0 a cycle would be 29 clock pulses long; if preset to 9 a cycle would be 20 clock pulses long. Thus a cycle is (29-N) clock pulses long if N is the number preset in the counter.

INTEGER COUNTER F

The integer counter consists of a presettable counter U7 and NAND gate U9A. The purpose of the integer counter block is to control the number of clock cycles that the prescaler will be in the "pulse swallow" (divide by 11) mode. Suppose that U7 was preset to 5 via the LRESET pulse. The next clock pulse after LRESET goes HIGH, causes U7 to increment its count and after 4 clock pulses U7 reaches a count of 9 and the output of U9A, STOP SWALLOW, goes HIGH. This HIGH output is clocked into U3A at the next clock pulse, thereby forcing U3B pin 9 (LSWALLOW) HIGH. Summarizing, it took 6 clock pulses after LRESET went HIGH before LSWALLOW was asserted HIGH. However it should be mentioned that LSWALLOW is not forced LOW until one clock pulse after LRESET. Thus with the integer counter preset to 5 the LSWALLOW line was LOW for 5 clock pulses which means the prescaler was in divide by 11 mode for 5 clock pulses. If the counter had been preset to 4 one additional clock pulse would have been required so that the divide by 11 mode would have lasted for 6 clock pulses. Thus if the integer counter is preset to some number N, then the prescaler will divide by 11 for (10-N) clock pulses.

Ignoring the fractional counter block for the moment a general description of the circit can now be given. Suppose the direct divider is preset to 21 and the integer counter is preset to 5. Using previous discussions it is known that there will be 21 clock pulses in a cycle and that (10-5) or 5 of them will be in the divide by 11 mode and (21-5) or 16 of them will be in the divide by 10 mode. Since it requires 55 input pulses to produce 5 clock pulses when in divide by 11 mode and 160 input pulses to produce 16 clock pulses in the divide by 10 mode we have the following relationship:

55 + 160 = 215 input pulses produces 21 clock pulses or 1 output pulse. We are therefore dividing the input signals frequency by 215.

FRACTIONAL COUNTER C

The FRACTIONAL COUNTER block is the section that provides

non-integer divide numbers. The fractional counter block contains rate multipliers U5 and U6 and one shot multivibrator U11. The rate multipliers produce M1 M2 pulses (M1 M2 is a two digit BCD number) for 100 pulses input, or the frequency out is (M1 M2 / 100) times the frequency in. So if M1=3 and M2=2 then 32 pulses will come out for every 100 pulses input. The rate multipliers are enabled through U2D and the control line HLE2. A HIGH on HLE2 causes the rate multipliers to be enabled. The rate multipliers have as their clock inputs the Divided Output signal. The output of this block is the STOP SWALLOW EARLY line which when HIGH causes the SYNCHRONIZER to bypass the normal routing of the integer counter output and forces the LSWALLOW line HIGH one clock pulse earlier than it normally would have. So for the particular cycle that STOP SWALLOW EARLY is HIGH one less input pulse is required to produce the same output pulse. The one shot U11 holds the STOP SWALLOW EARLY line HIGH for about 1.6 microseconds (when triggered by rate multiplier U5) so that the SYNCHRONIZER will properly respond to it. Assume the rate multipliers have been set to 32. Therefore 32 output pulses are produced for every 100 input pulses. So 32 out of 100 cycles the prescaler is ``swallowing'' one less pulse than it normally would have, causing the input frequency to decrease (the output frequency is fixed because of phase lock). In fact the amount of decrease is (32/100) X 500 kHz or 160 kHz. In terms of pulses and using the previous example of divide by 215 we would have 32 cycles of divide by 214 and 100-32 or 68 cycles of divide by 215. Adding things up we have:

32 X 214 + 68 X 215 = 21,468

So we have 21,468 input pulses for 100 output pulses or a divide number of 21,468/100= 214.68 and the input frequency should be 500 kHz X 214.68 = 107.34 MHz because of phase lock.

SYNCHRONIZER G

The SYNCHRONIZER controls the state of the LSWALLOW line based on two inputs, the STOP SWALLOW line and the STOP SWALLOW EARLY line. The LRESET line going LOW causes U3A pin 6 to go HIGH and U3B pin 9 (LSWALLOW) to go HIGH forcing the prescaler to the divide by 10 mode. The next CLOCK pulse after LRESET goes HIGH (LRESET is LOW for 2 CLOCK pulses) causes the U3A pin 6 output through U2B to change the state of U3B , forcing the LSWALLOW line LOW. Thus every cycle starts (one CLOCK pulse after LRESET) with LSWALLOW LOW and the prescaler in the divide by 11 mode. U2A and U2B serve to route the STOP SWALLOW signal around U3A when the STOP SWALLOW EARLY line is HIGH thereby causing U3B pin 9 to go HIGH one clock pulse earlier than normal.

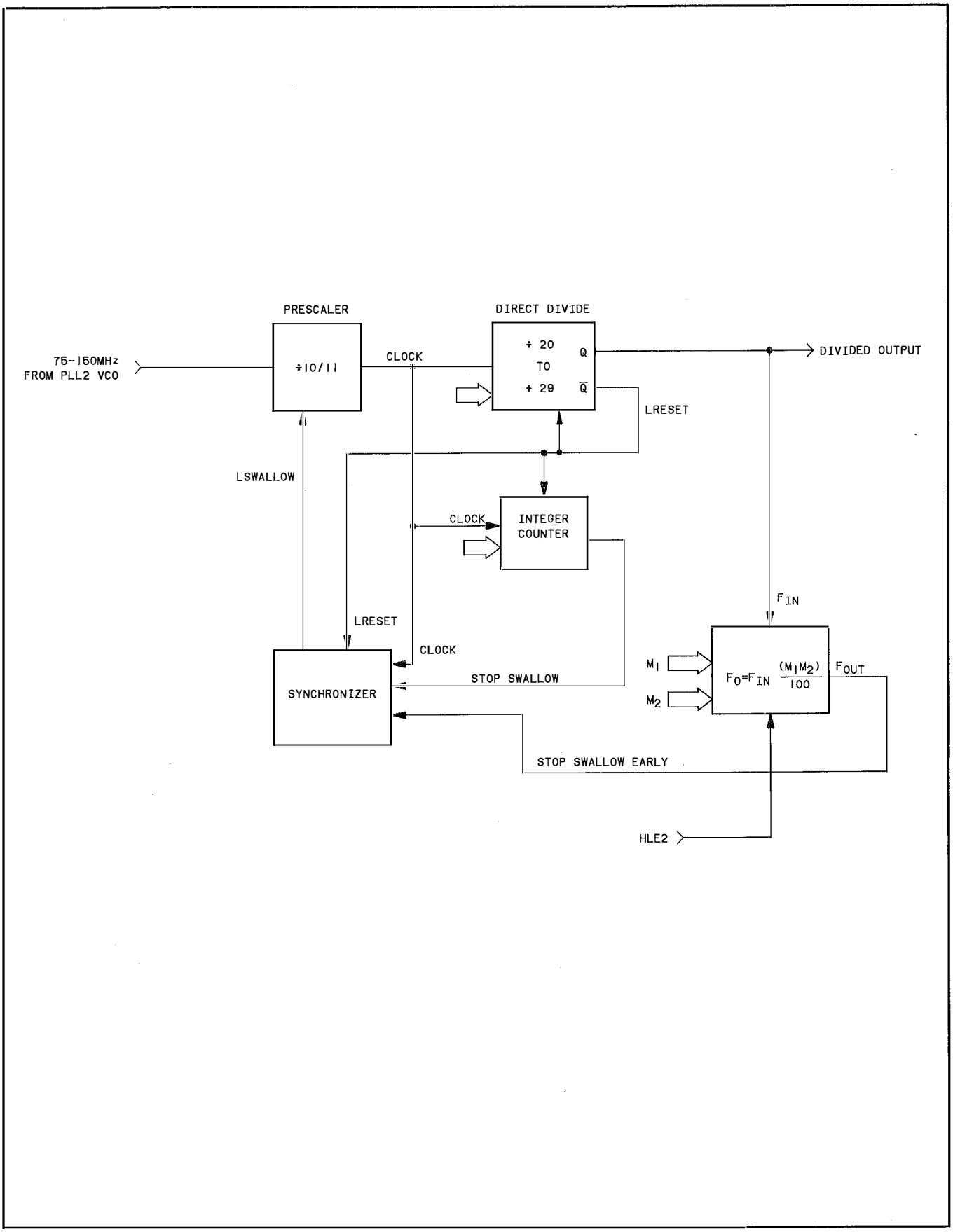


Figure 8C-29. PLL2 Divider Simplified Block Diagram

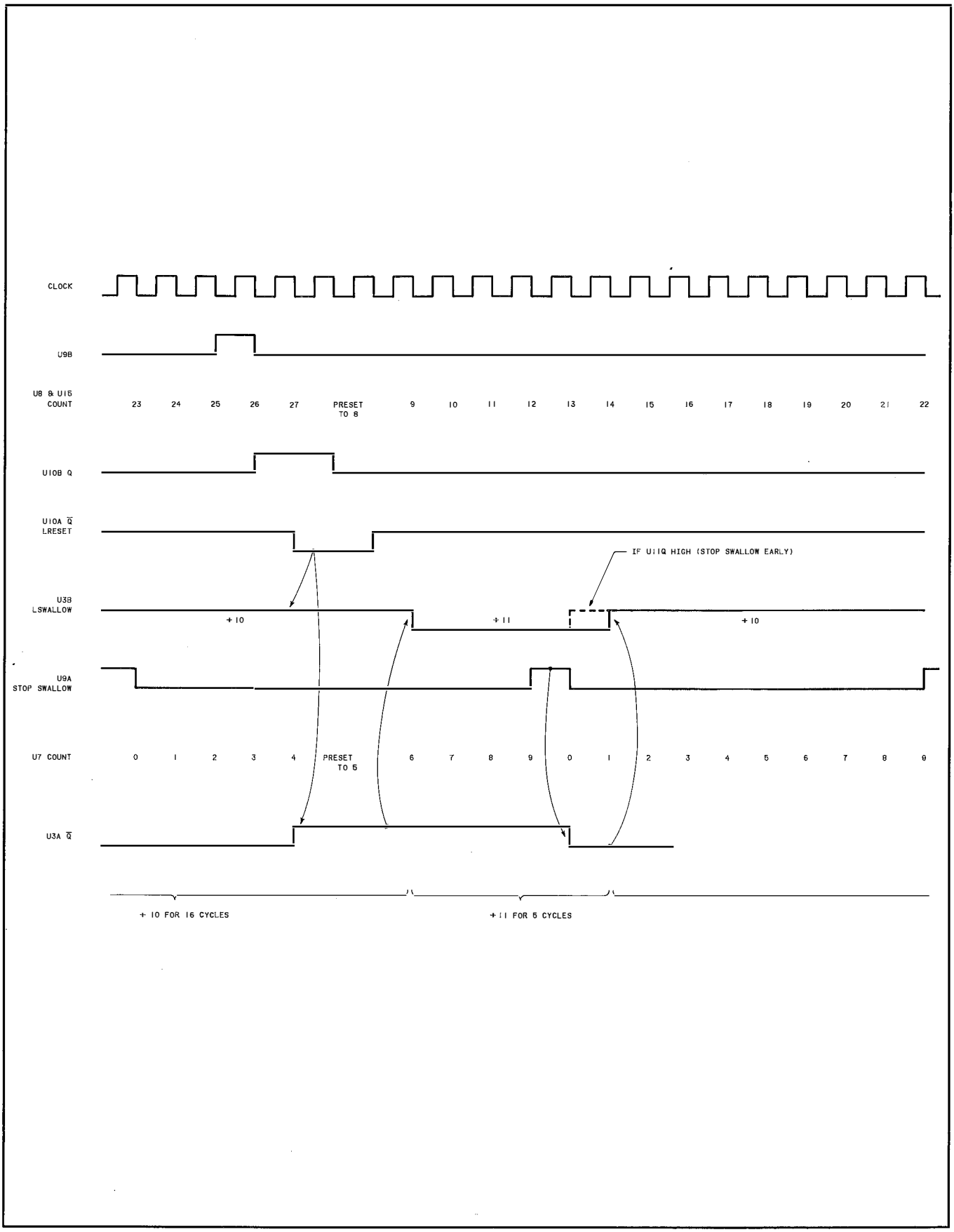


Figure 8C-30. Partial Circuit Timing for ÷ 215 Example

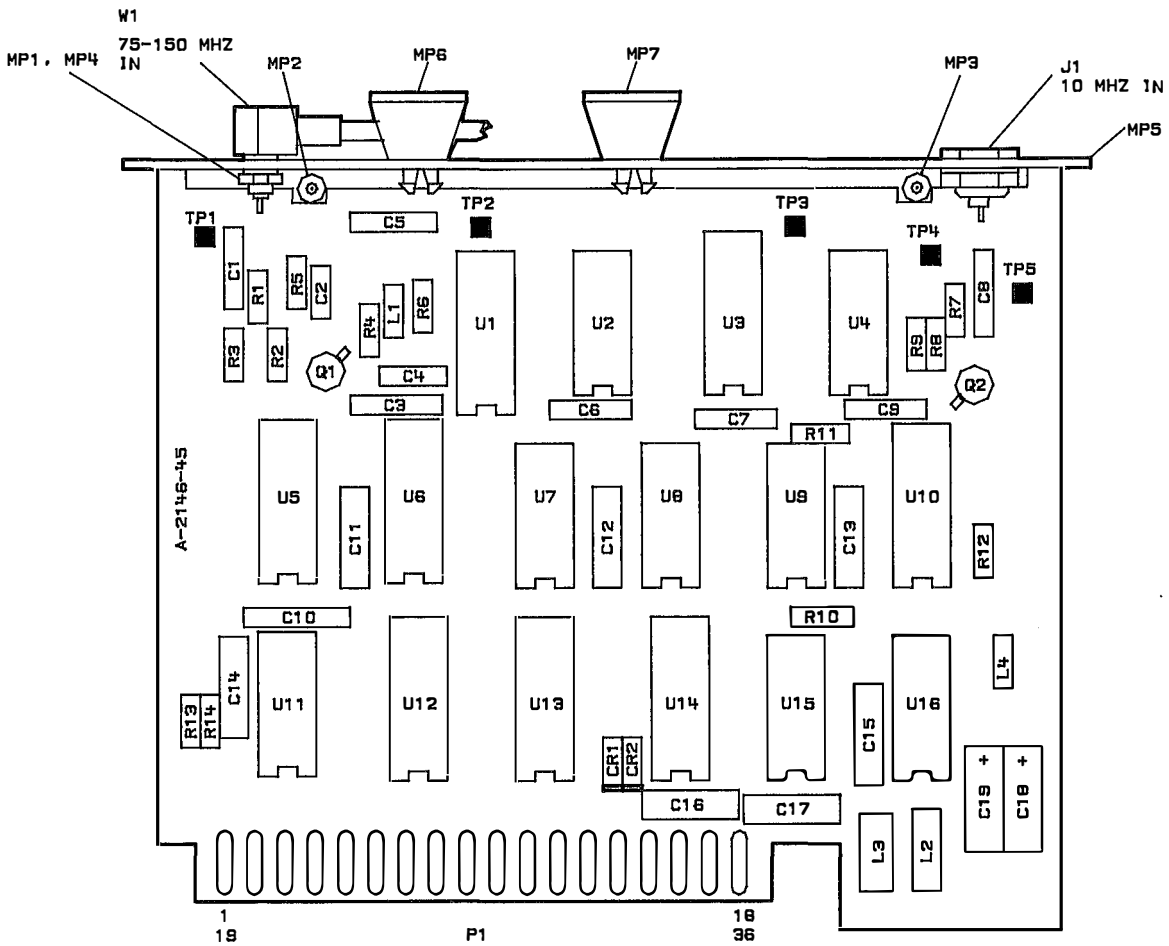


Figure 8C-31. A42 PLL2 Divider, Component Location Diagram

A42 PLL2 Divider, Pin I/O

A42

Pin	Mnemonic	Levels	Source	Destination
1 19	LCK2 LCK1	TTL (LOW TRUE) TTL (LOW TRUE)	XA59P1-109 XA59P1-54	A A
2 20	HLE2 GND	TTL (HIGH TRUE) 0V	XA59P1-53 A62 STAR GND	*C D *H
3 21	DB1 DB0	TTL TTL	XA60P1-76 XA60P1-20	*A *A
4 22	DB3 DB2	TTL TTL	XA60P1-77 XA60P1-21	*A *A
5 23	DB5 DB4	TTL TTL	XA60P1-78 XA60P1-22	*A *A
6 24	DB7 DB6	TTL TTL	XA60P1-79 XA60P1-23	*A *A
7 25	DB9 DB8	TTL TTL	* *	*A *A
8 26	DB11 DB10	TTL TTL	* *	*A *A
9 27	500 KHZ REF DIV N2	TTL TTL (LOW TRUE)	D B	XA41P1-20 *C
10 28	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
11 29				
12 30				
13 31				
14 32	SW2 SW1	TTL TTL	A A	XA40P1-22 *
15 33	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*NOT USED *NOT USED
16 34	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*NOT USED *NOT USED
17 35	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
18 36	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*H *H

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

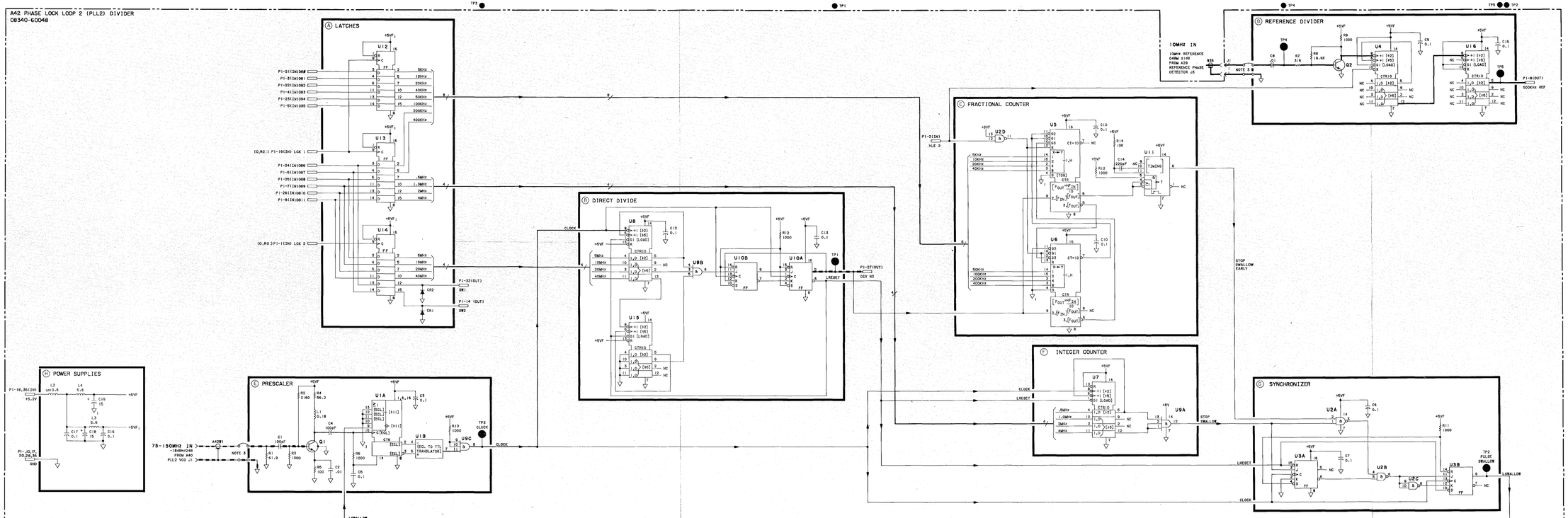


Figure 8C-32. A42 PLL2 Divider, Schematic Diagram

A43 PHASE LOCK LOOP 2 (PLL2) DISCRIMINATOR, CIRCUIT DESCRIPTION

INTRODUCTION

The A43 PLL2 Discriminator Assembly contains the discriminator used to control the PLL2 VCO. The sensitivity of the discriminator is adjusted by control signal N2 Tune into CURRENT SOURCE (Block **B**) from A41 PLL2 Phase Detector. In addition, the A43 Phase Lock Loop 2 Discriminator assembly contains the summing circuitry to combine the 0 to 10V 20-30 sweep ramp signal into P1 pin 1 of the DELTA F SWEEP ATTENUATOR (Block **E**) from the A58 Sweep Generator, the PRETUNE (Block **D**) from the A60 Processor, and the discriminator output to produce a 1 to 9mA current to tune the A40 PLL2 VCO.

The method used to combine these signals is to mix all three input currents together at the input to an integrator (junction of R43 in SUMMING AMPLIFIER (Block **F**) and R40 in PRETUNE Block **D**). If the voltage at this node is not zero, then the integrator output will change, and force the PLL2 VCO to a different frequency. The frequency continues to change until the discriminator's output current to the summing node is at a level to produce zero volts at the summing node. This forms a frequency-locked loop, with the discriminator as the feedback element. The result is the equivalent of having a very linear VCO. (See Figure 8C-33).

This "discriminator-linearized-VCO" is used inside a phase lock loop. In this configuration the phase lock loop tunes the VCO indirectly, by changing the gain of the discriminator. This provides the capability to establish an accurate, synthesized start frequency by using the phase lock loop to fine tune the discriminator during pre-sweep phase locking. To sweep the loop, the discriminator's fine tune voltage is stored in a sample and hold circuit, and the phase-locked loop is opened. This establishes an accurate, synthesized start frequency for the sweep and calibrates the discriminator gain. The current summing node is still forced to zero volts, so if a ramp of current is injected into the node, the discriminator/VCO loop causes the VCO to ramp in frequency and exactly cancel the injected current by a reduction in discriminator output current. Since the discriminator remains active at all times, the sweep linearity is primarily a function of the discriminator, and not the PLL2 VCO.

The discriminator itself is formed by two of the blocks of the A43 circuit; the PULSE GENERATOR (Block **A**) and the CURRENT SOURCE

(Block **B**). The input to the discriminator is used to trigger a very stable 1.6 microsecond pulse. The current source is activated by this pulse, and outputs a fixed amount of current for 1.6 microseconds. These current pulses are averaged to yield some net current flow that is proportional to the frequency of the input to the discriminator; the higher the frequency, the more frequent the 1.6 microsecond pulses, and the greater the average current. The gain of the discriminator (current out/frequency in) can be adjusted by changing the magnitude of the current pulses, but the width will always be a constant 1.6 microsecconds.

PULSE GENERATOR A

The PULSE GENERATOR functions as a one shot multivibrator. However, in a standard multivibrator the pulse width is determined by an RC time constant and the trigger point may vary with circuit components and also with noise. In this case, pulse width (about 1.6 microseconds) repeatability is critical. The signal at TP2 then is a 1.6 microsecond pulse, with a repetition rate equivalent to the input frequency. This signal will be integrated in the Current Source (Block **B**) to produce an average current related to the input frequency. The 150 to 300 kHz (ECL level) input from the A40 PLL2 VCO assembly is amplified and level shifted by Q6 and Q7. At the begining of a cycle, both inputs to U7D are LOW. When Q7 collector goes HIGH, U7D output goes LOW saturating Q11 and causing resonator L4, C15, and C16 to ring at 5.2 MHz. This damped oscillation appears at Q9 collector, is clipped by Q10, and used to drive counter U6.

Q10 is a comparator. The signal appears across L5 driving the base of Q10A and Q10B in opposite directions. U6 is preset to a count of 6. When the count reaches 8, the "8" output of U6 goes high. This is fed back to U7D pin 11, holding its output LOW . After 1.6 microseconds, the count reaches 16, the 8 output goes LOW again, U7D output goes HIGH turning Q11 OFF resulting in the resonance being damped by R17. At the count of 16, U7C and U7B reset the counter to 5. Before the oscillation is fully damped, the counter gets clocked to 6. U6 should always be reset to either 5 or 6 depending upon how quickly Q11 can dampen the resonator. The actual number is not relevant, since the pulse output starts at the count of 8, effectively ignoring the first several pulses, and the width will always be a constant 1.6 microseconds.

U7D output going LOW starts the resonator ringing. If for some reason the counter did not reach an 8 count, U7D output would be held low causing a latch-up condition. When U7D output is HIGH, U7A output turns CR1 ON discharging C14. When U7D output goes LOW, CR1 is reversed biased and C14 starts to charge through U6

pin 14 towards Vcc until the U6 input circuit trips, reseting U6 and preventing a latch-up condition.

The pulse width at TP2 should be equivalant to eight pulses at TP3.

CURRENT SOURCE B

With the tuning voltage input (P1 pin 28) at zero volts, the voltage divider from -7V through R6, Q3A/B, R7 to +20V sets the input to U4 pin 3 at about +13V. U4 and Q4 form a voltage controlled current source, where the magnitude of the current flowing out of Q4 drain is proportional to the voltage on U4 pin 3. The ratio of current to voltage is calibrated by R9, .3 MHz Adjust. The output of the current source flows through Q5A when the "8" output of U6 is LOW. If an input pulse has triggered the pulse generator, the current is switched through Q5B for 1.6 microseconds. Since Q4 and its associated circuit is a constant current source, when Q5A is ON all the current flows through Q5A, leaving no current for Q5B. When Q5A is shut OFF all the current flows through Q5B. Q5B current is integrated by C20 and goes through a low-pass filter to the summing point of the discriminator loop. The average value of this current is directly proportional to the input frequency, being about 1.5 mA at 0.3 MHz. The 0.3 MHz Adjust (R9) in the U4 feedback loop adjusts the the discriminator gain by changing the amplitude of the 1.6 microsecond current pulses into the filter.

The tuning voltage input (N2 Tune) from the A41 PLL2 Phase Detector (P1 pin 28) is also able to adjust the gain of the discriminator by $\pm 1\%$ by changing the voltage at U4 pin 3, and thereby changing the amplitude of the 1.6 microsecond current pulses.

C21 is used to stabilize the two grounds when Q5A/B is switching.

-7V SUPPLY C

U13 maintains a constant current through reference diode CR1. R35 sets this current to approximately 7.7mA. The 6.3V reference is amplified due to the ratio of R33 and R34 to yield -7V. Q8 provides a low impedance, high current output.

PRETUNE D

The pre-tune circuit tunes the discriminator loop approximately to the desired frequency. The phase lock loop then applies small corrections to get the frequency exact. The A60 Processor outputs a 10-bit binary word representing the pretune frequency and then strobes the data into latches U9 and U12 by outputting address

0,R1: (channel 0, subchannel 1). The data programs DAC U11, whose output goes to U10. If the input is all zeros, the output of U10 is zero volts. The 1.5 mA into the summing node must then come entirely from the discriminator (sweep ramp =0). 1.5 mA out of the discriminator corresponds to 0.3 MHz into the discriminator. To pretune the input frequency to 200 kHz, a binary word representing decimal 1000 is programmed into the the DAC U11. This results in +6.84V at TP1 and a corresponding current into the summing node, through R41 and R42, of 0.5mA. Adding 0.5mA to the summing node causes the discriminator output current to equal 1.5-0.5 or 1.0 mA which corresponds to a discriminator input frequency of 0.2MHz. R41 (0.2 MHz Adjust) is used to adjust the VCO frequency to 100 MHz and thus the discriminator input frequency to 0.2 MHz (100 MHz/500). R41 (0.2 MHz Adjust) and R9 (0.3 MHz Adjust) function as slope and offset adjustments to calibrate the discriminator system to exactly 5mA/MHz.

DELTA F SWEEP ATTENUATOR E

The 0 to 10 volt A58 20-30 Sweep Generator sweep ramp (P1-1) is selected and attenuated depending upon the state of U12 pin 15 and U12 pin 2 (the latched outputs for data lines IOB10 and IOB11). The state of each switch of U1 and U2 is shown in a table on the schematic diagram (Figure 8C-35) for any combination of HIGHS and LOWS on these latched control lines. Switch U1A when closed passes the 0 to 10 volt ramp un-attenuated to the summing junction in SUMMING AMPLIFIER (Block **F**). Switch U1B and switch U1C are used for cancellation of the ON resistance of switch U1A. Cancellation is achieved by scaling the sweep ramp with R29 and switch U1C and then feeding it to the summing junction through R30 and U1B. When switch U1D is closed the sweep ramp is routed through R26 and R25 which results in one tenth of the current being summed in due to the ramp than in the previous case with U1A being closed. Refer to Figure 8C-34 for the simplified SWEEP ATTENUATOR circuit diagram.

U2 switch A and B route the sweep ramp directly to the OUTPUT CURRENT SOURCE (Block **G**) which directly tunes the PLL2 VCO. This "feed forward" path helps compensate for the rather slow response of the discriminator loop. U2 switches C and D perform logic functions. See the table on the schematic diagram for details.

SUMMING AMPLIFIER F

U3 is configured as a non-inverting integrator. The voltage at the input to the integrator (junction of R43, R50 in CURRENT SOURCE Block **B** and R40 in PRETUNE Block **D**, etc.) is forced to zero volts by the discriminator feedback through R50. With zero volts at the input, R40 will sink 1.5mA. Since no current is flowing into the integrator, the following condition applies:

Pretune current + Discriminator current + Sweep current = 1.5 mA

The sensitivity of this node is 5mA/MHz; that is, if 0.005mA of sweep current is added to the node, the input to the PULSE GENERATOR (Block **A**) will decrease by 0.001 MHz, causing the discriminator to reduce its output current by 0.005mA, exactly cancelling the sweep current.

OUTPUT CURRENT SOURCE G

The emitter of Q2 provides a virtual ground to sum error currents from U3 and feed-forward signals from the DELTA F SWEEP ATTENUATOR (Block **E**) and phase-lock inputs. The phase-lock feed-forward path reduces the lock time by feeding the discriminator tune voltage ahead to the output current source.

To achieve a low noise junction, there is an optimum input impedance to be presented by Q2. This requires a constant emitter current. Q1 is used to achieve a constant Q2 emitter-current of about 0.14 mA. Q2 will conduct only enough current to cause a 0.7 V drop across R47, at which point Q1 will turn on and conduct the remaining current. The changing tuning current of 1 to 9 mA will then flow through Q1, leaving Q2 with a constant current, hence a constant input impedance.

The output of the current source is a current of 1 to 9 mA sent to the A40 PLL2 VCO.

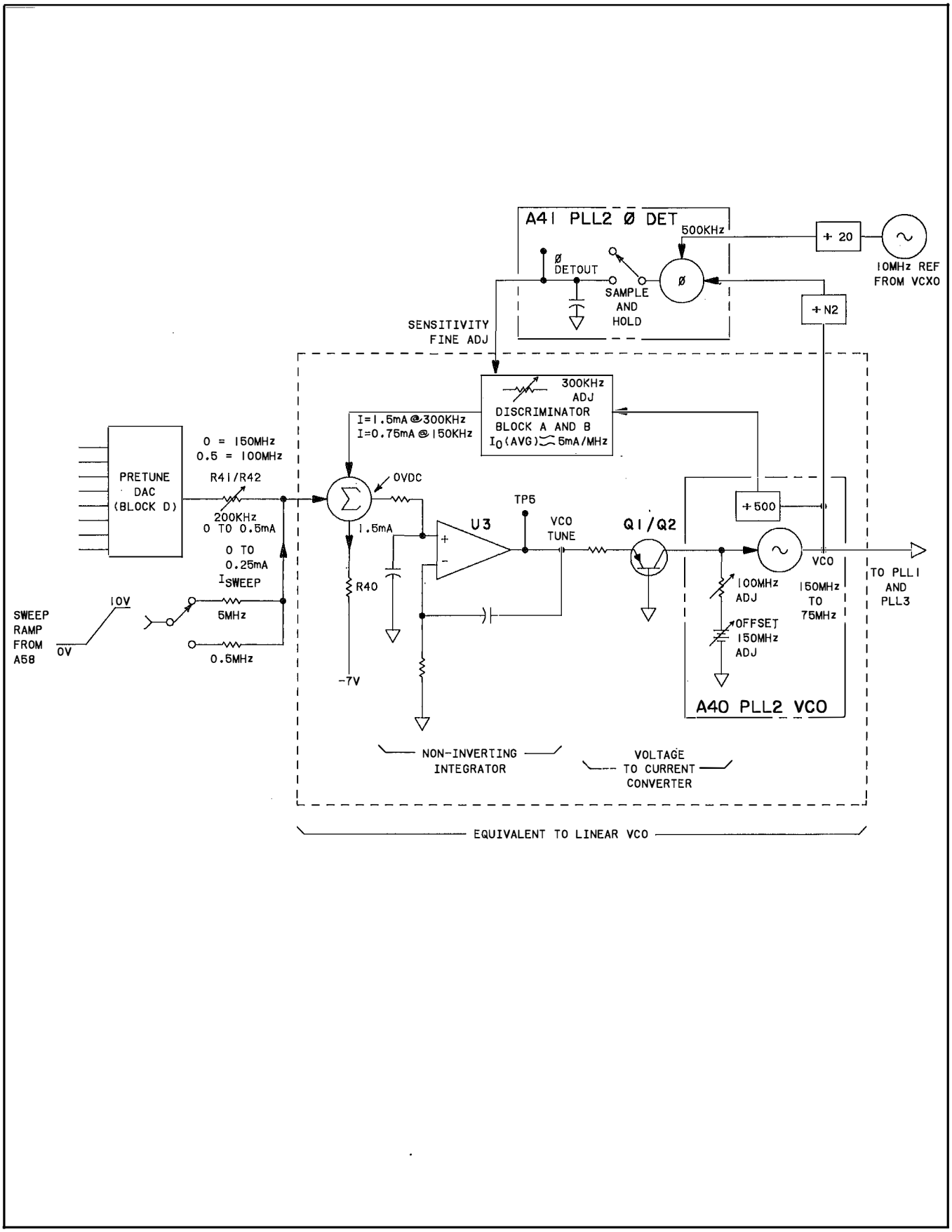


Figure 8C-33. Simplified A43 PLL2 Discriminator Diagram

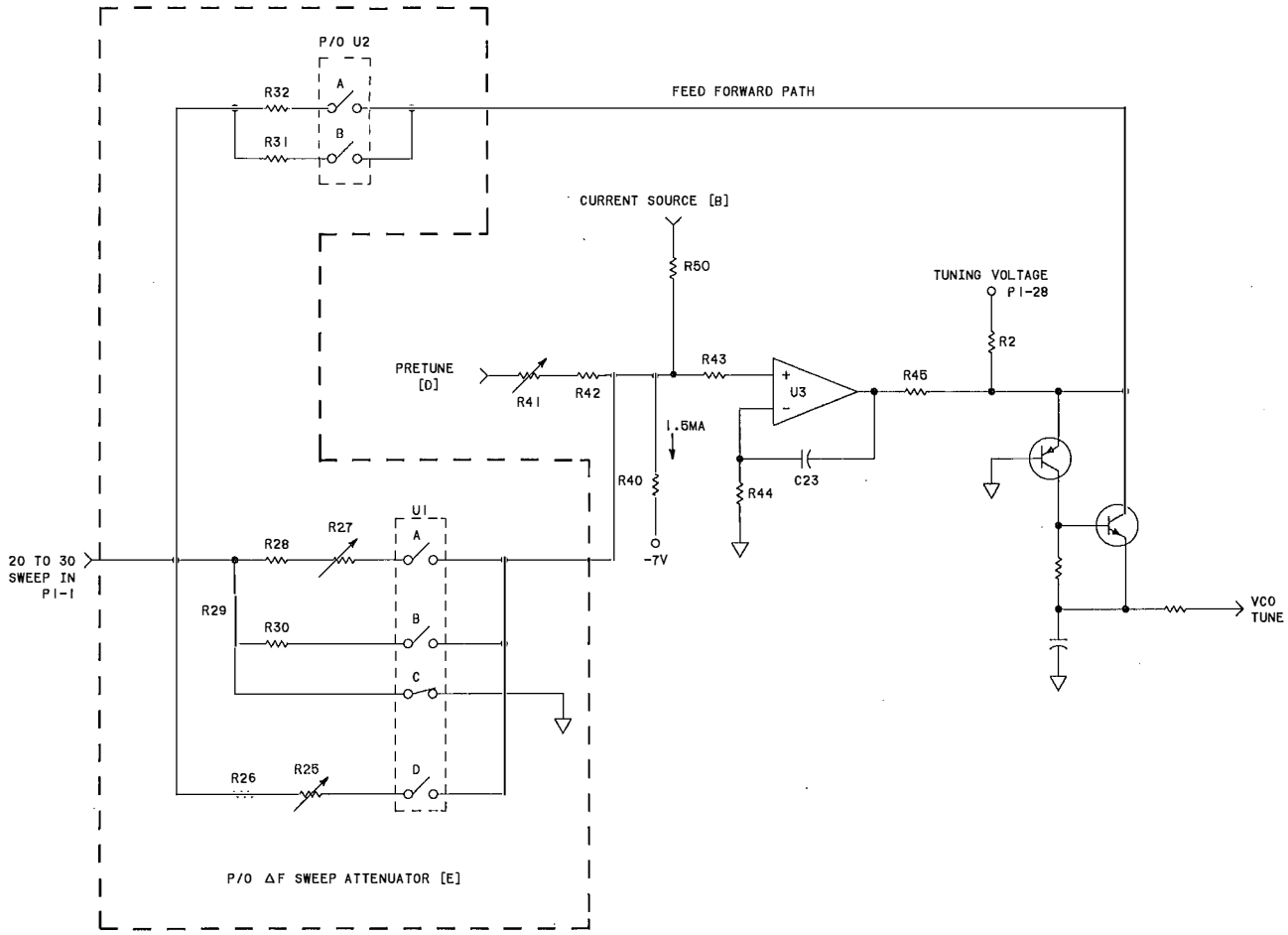


Figure 8C-34. Simplified ΔF Sweep Attenuator Circuit

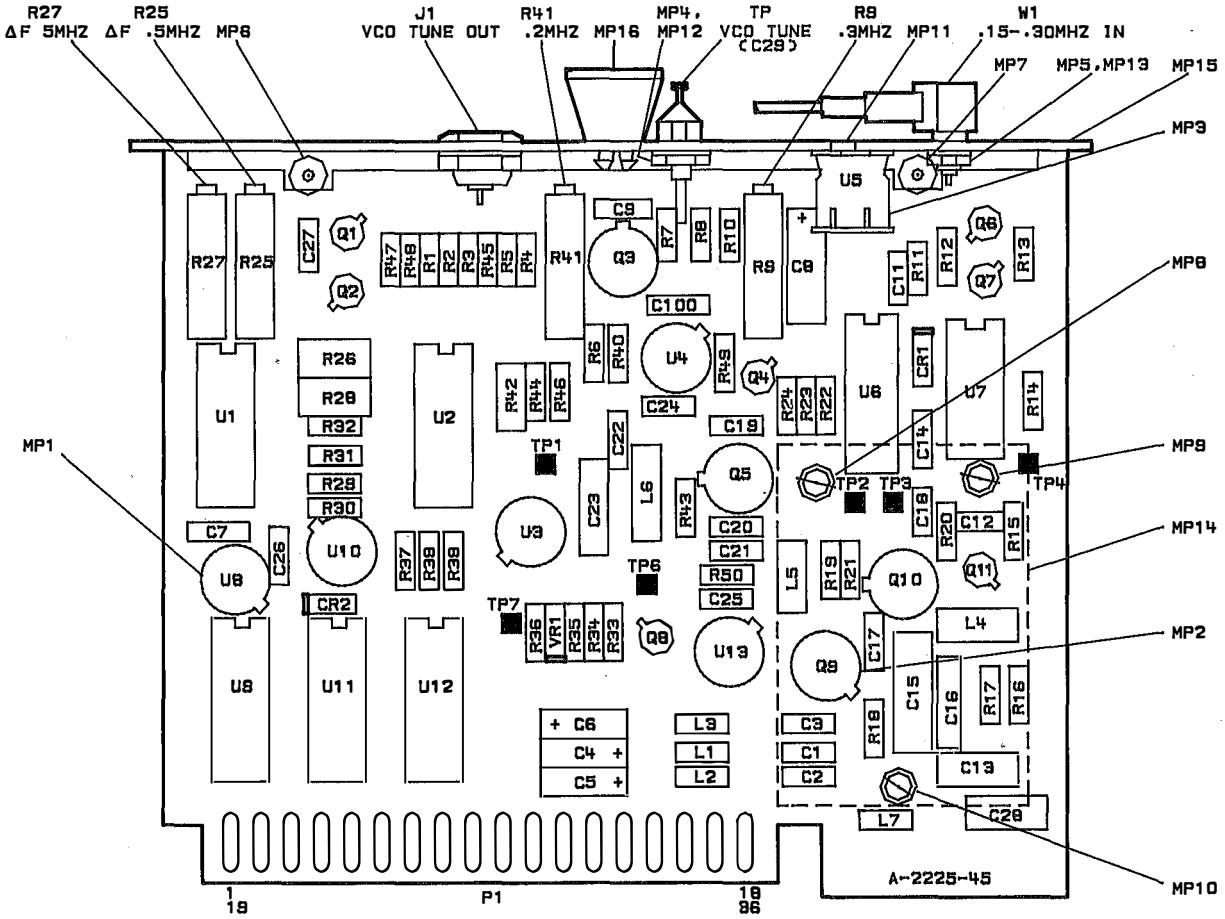


Figure 8C-35. A43 PLL2 Discriminator, Component Location Diagram

A43 PLL2 Discriminator, Pin I/O

A43

Pin	Mnemonic	Levels	Source	Destination
1 19	20/30 SWP LCK3	0 TO +10V TTL (LOW TRUE)	XA58P1-41 XA59P1-108	E D
2 20	HLE2 RGND	TTL (HIGH TRUE) 0V	XA59P1-53 A62 STAR GND	*NOT USED *H
3 21	DB1 DB0	TTL (LOW TRUE) TTL (LOW TRUE)	XA60P1-76 XA60P1-20	*D *D
4 22	DB3 DB2	TTL (LOW TRUE) TTL (LOW TRUE)	XA60P1-77 XA60P1-21	*D *D
5 23	DB5 DB4	TTL (LOW TRUE) TTL (LOW TRUE)	XA60P1-78 XA60P1-22	*D *D
6 24	DB7 DB6	TTL (LOW TRUE) TTL (LOW TRUE)	XA60P1-79 XA60P1-23	*D *D
7 25	DB9 DB8	TTL (LOW TRUE) TTL (LOW TRUE)	* *	*D *D
8 26	DB11 DB10	TTL (LOW TRUE) TTL (LOW TRUE)	* *	*D *D
9 27	−7V REF GND	−7V 0V	C A62 STAR GND	XA41P1-7 *H
10 28	N2 TUNE RTN N2 TUNE	0V 0 TO +7V	XA41P1-8 XA41P1-23	C B G
11 29	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
12 30	GND	0V	A62 STAR GND	*H
13 31	GND	0V	A62 STAR GND	*H
14 32	GND	0V	A62 STAR GND	*H
15 33	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*H *H
16 34	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*H *H
17 35	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
18 36	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*H *H

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

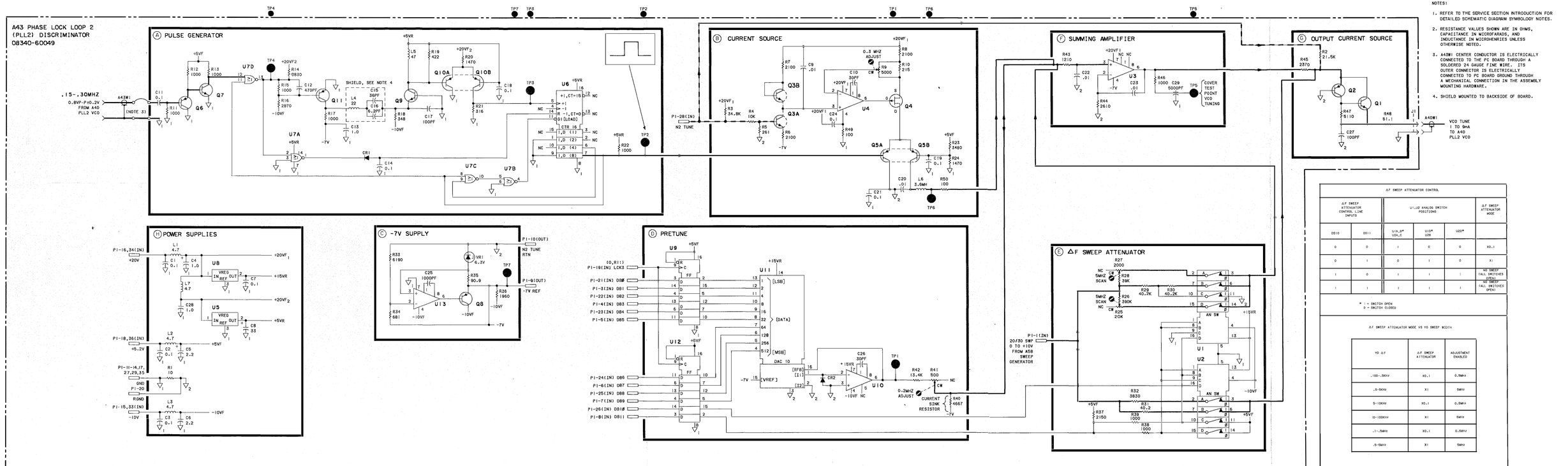
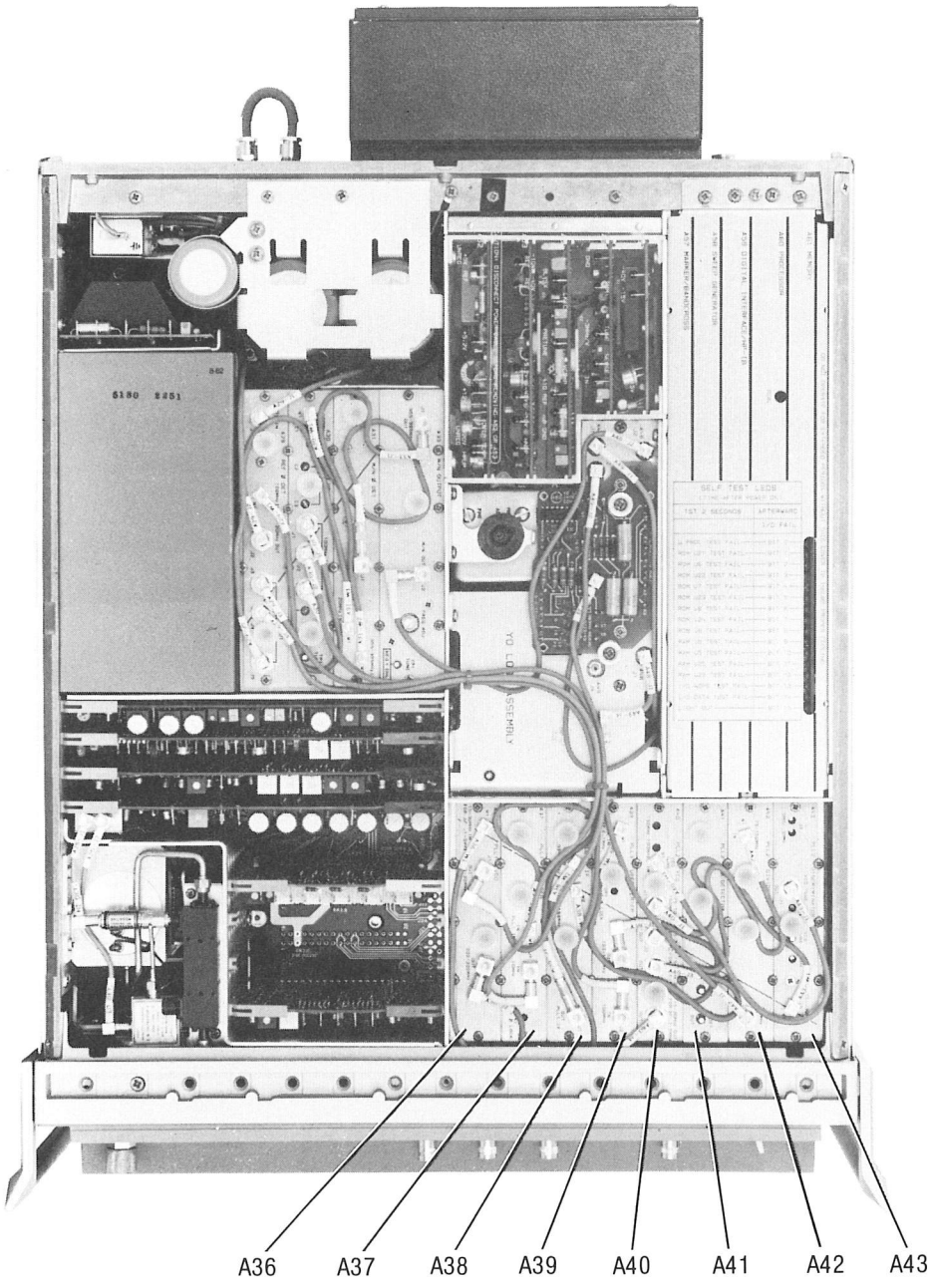


Figure 8C-36. A43 PLL2 Discriminator, Schematic Diagram



Bottom View (Bottom Cover Removed)

Figure 8C-37. 20-30 Loop Major Assembly Diagram

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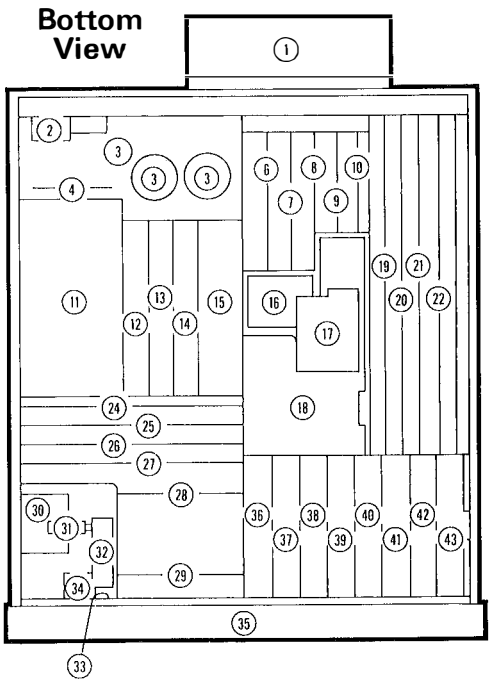
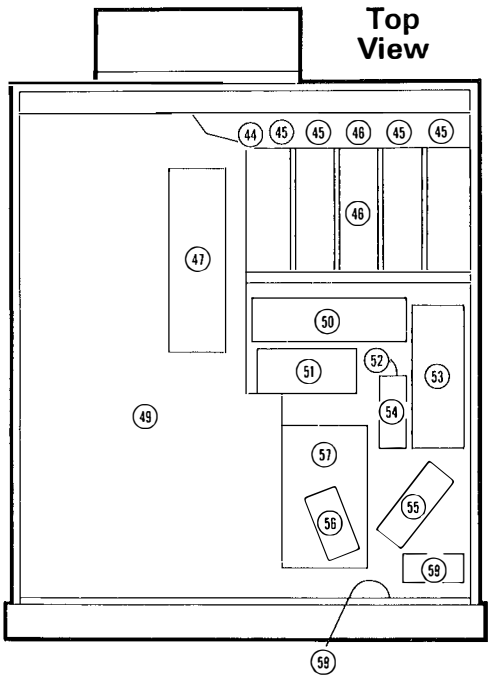




Assy./Ref. Des.	Description	Location	Volume 3					Volume 4		
			Ref.-M/N Loops	20-30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	33					●			
A2	Display Driver	33					●			
A3	Display Processor	33					●			
A4	Not Assigned	-								
A5	Keyboard	35					●			
A6	Keyboard Interface	35					●			
A7	Lower Keyboard	35					●			
A8	3.7 GHz Oscillator	57						●		
A9	Band 0 Pulse Modulator	56						●		
A10	Directional Coupler	32						●		
A11	Band 1-4 Detector	31						●		
A12	Band 0 Splitter/Detector	34						●		
A13	SYTM (Switched YIG Tuned Multiplier)	30						●		
A14	Band 1-4 Power Amplifier	53						●		
A15	Band 0 Low Pass Filter	52						●		
A16	Band 1-4 Modulator/Splitter	51						●		
A17	Band 0 Mixer	54						●		
A18	Band 0 Power Amplifier	55						●		
		60						●		
A19	Capacitor Assembly	48							●	
A20	RF Section Filter	50						●		
A21	Pulse Modulator Driver	29						●		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRO Bias	28						●		
A25	ALC Detector	27						●		
A26	Linear Modulator	26						●		
A27	Level Control	25						●		
A28	SYTM Driver	24						●		
A29	Reference Phase Detector	12	●							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	●							
A31	M/N Phase Detector	14	●							
A32	M/N VCO (Voltage Controlled Osc.)	15	●							
A33	M/N Output	15	●							
A34	Reference-M/N Motherboard	5	●							
A35	Rectifier	4							●	
A36	PLL1 VCO (Voltage Controlled Osc.)	36		●						
A37	PLL1 Divider	37		●						
A38	PLL1 IF	38		●						
A39	PLL3 Upconverter	39		●						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		●						
A41	PLL2 Phase Detector	41		●						
A42	PLL2 Divider	42		●						
A43	PLL2 Discriminator	43		●						
A44	YIG Oscillator (YO)	18			●					
A45	Directional Coupler	18			●					
A46	7 GHz Low Pass Filter	18			●					
A47	Sense Resistor Assembly (YO circuit)	47			●					
	(SYTM circuit)	47						●		
A48	YO Loop Sampler	18			●					
A49	YO Loop Phase/Detector	18			●					
A50	YO Loop Interconnect	17			●					
A51	Reference Oscillator	16	●							
A52	Positive Regulator	6							●	
A53	Negative Regulator	7							●	
A54	YO Pretune/Delay Compensation	8			●					
A55	YO Driver	9			●					
A56	−15V Regulator	10							●	
A57	Marker/Bandcross	19				●				
A58	Sweep Generator	20			●					
A59	Digital Interface	21				●				
A60	Processor	22				●				
A61	Not Assigned	23				●				
A62	Motherboard	49								
A63	90 dB RF Attenuator	59						●		
AT1	Peripheral Mode Isolator	58						●		
AT2	15 dB Attenuator	18			●					
B1	Fan Assembly	1							●	
A62C1-3	Power Supply Filter Capacitors	3							●	
FL1	AC Line Module	2							●	
A62Q1-4	Power Supply Regulating Transistors	45							●	
A62S1	Power Supply Thermal Switch	44							●	
T1	Power Supply Transformer	11							●	
A62U1	Power Supply Regulator	46							●	

SWEEP GENERATOR – YO LOOP D

SWEEP GENERATOR - YO LOOP
INTRODUCTION

This section provides information and instructions for troubleshooting, repairing, or replacing assemblies and components in the Sweep Generator and the YO Loop. Information includes circuit descriptions, troubleshooting procedures, block diagrams, schematics, and component location diagrams for each printed circuit board assembly.

The Sweep Generator and YO Loop circuitry generate the signals used to tune the YO according to the mode of operation selected.

The Sweep Generator consists of the following assemblies:

- A54 YO Pretune/Delay Compensation Assembly
- A55 YO Driver Assembly
- A58 Sweep Generator Assembly

The YO Loop phase-locks the YO at the appropriate frequency when the instrument is operated in the CW and Manual-Sweep modes.

The YO Loop consists of the following assemblies:

- A44 YO Assembly
- A45 Pre-Leveler Assembly
- A46 7 GHz Low-Pass Filter Assembly
- A48 YO Loop Sampler Assembly
- A49 YO Loop Phase Detector Assembly
- A50 YO Loop Interconnect Assembly
- A54 YO Pretune Delay Compensation Assembly
- A55 YO Driver Assembly

SWEEP GENERATOR/YO LOOP
THEORY OF OPERATION

SWEEP GENERATOR/YO LOOP - OVERALL DESCRIPTION

The Sweep Generator and YO Loop circuitry generate the signals used to tune the YO according to the mode of operation selected. The assemblies included in this section are the A44 YO, A45 Preleveler, A46 7 GHz Low Pass Filter, A47 Sense Resistor Assembly, A48 YO Loop Sampler, A49 YO Loop Phase Detector, A50 YO Loop Interconnect Board, A54 YO Pretune Delay Compensation board, A55 YO Driver Assembly, and A58 Sweep Generator board. A block diagram of the Sweep Generator/YO Loop is shown in Figure 8D-1.

The inputs to this section come from the instrument processor, the 20-30 Loop, and the M/N Loop. The main output is YO RF Output. Other important outputs are PRETUNE, used to tune the YO and the SYTM; BVSWP (Buffered Voltage SWeeP), used on the A27 Level Control board; 20-30 SWP, used to sweep the 20-30 Loop for sweep widths $\leq$5MHz; and MKR RAMP, used as the reference for all sweep events.

The operation of each block can best be described by considering the two main instrument modes of operation: CW/Manual, and Swept Frequency. The Swept mode can be in one of three conditions: single band sweep, multiband sweep, or narrow band sweep.

CW/MANUAL SWEEP OPERATION

When the CW mode is selected, the Sweep Generator/YO Loop Circuitry phase-locks the YO at the appropriate frequency. The processor addresses and sends a number to the A54 YO Pretune Delay Compensation board which is converted to a voltage, VDAC, and summed with the constant DC voltage, VREF. This produces the PRETUNE voltage, which tunes the YO to approximately the desired frequency (ie, to within the capture range of the YO Phase Locked Loop). VSWP and LKICK have no contribution to the Pretune voltage in CW operation.

The processor also sets the frequencies of the M/N and 20-30 Loops according to the CW frequency selected. The outputs of these two loops are used by the YO Loop to exactly tune and phase-lock the YO. The A45 Preleveler couples a portion of the YO RF Output back through a low-pass filter to the A48 Sampler, where it is mixed with the Nth harmonic of the M/N Output. This generates a difference signal, Sampler IF, in the range of 20-30 MHz which is input to the A49 YO Loop Phase Detector. There the phase is compared to the 20-30 MHz Output signal. The resultant error signal, YO TUNE, is used to phase-lock the YO. The high frequency portion of YO TUNE (>100 Hz) is applied to the YO FM

Coil by the FM Coil Driver on the A49 YO Loop Phase Detector board. The low frequency portion (<100 Hz) is summed with PRETUNE on the A55 YO Driver and applied to the YO Main Coil. This completes the YO Loop and phase-locks the YO.

Manual Sweep operation is identical to CW in the operation of the Sweep Generator and YO Loop circuitry.

SWEPT MODE

Single Band Sweeps

In swept mode, the instrument phase-locks the YO at the beginning of each sweep, undergoing the same sequence of events as in the CW mode. The Sample and Hold on the A49 YO Loop Phase Detector board is then activated, and it holds the YO TUNE error signal constant at its phase-locked value. In the hold mode the YO phase-lock loop is opened, allowing a ramp signal, VSWP, to be summed into the PRETUNE signal and subsequently applied to the YO Main Coil to sweep the YO. This sequence is called Lock and Roll. The processor writes to the A58 Sweep Generator board the sweep time and sweep width numbers to generate the voltage ramp, VSWP, with the appropriate slope and duration. This board also generates a 0-to-10V voltage ramp (MKR RAMP), which has the same duration as VSWP.

Because of the inherent delay characteristics of the YO during sweeps, a ramping compensation voltage, VCOMP, is summed with PRETUNE in the A55 YO Driver. VCOMP is generated by summing correction data from the processor with the VSWP ramp. This is done in the YO Delay Compensation portion of the A54 YO Pretune Delay Compensation board.

At each YO sweep retrace, the YO Retrace Kick Pulse Generator (on the A54 board) produces a pulse with a programmable width pulse (via the processor) which is summed with PRETUNE. When activated, this momentarily tunes the YO lower in frequency (by about 2.5 GHz) to remove the effects of YO magnetic hysteresis.

Multiband Sweeps

The operation of the Sweep Generator/YO Loop circuitry in multiband sweeps is essentially the same as in single band sweeps. The difference is that at each band crossing, the YO is retraced and the lock and roll sequence is initiated again. This produces a pause in the instrument sweep at each bandcrossing while each loop is being reset. VSWP is reset to zero volts between bands, however the MKR RAMP signal remains fixed at its end-of-band value until the lock and roll sequence for the next

band begins. The sum of the durations of the ramping portions of MKR RAMP will still equal the selected instrument sweep time.

Narrow Band Sweep

Sweep widths ≤5 MHz are achieved by sweeping the 20-30 Loop. The A58 Sweep Generator board produces the 20-30 SWP (from inputs from the processor) which causes the 20-30 Output to sweep in frequency. The A49 YO Loop Phase Detector keeps the YO phase-locked to this signal for the duration of the sweep. For narrow band YO sweep widths between 500 kHz and 5 MHz, PRETUNE is also swept (VSWP summed in) a proportional amount so that the pretuned YO frequency will remain within the capture range of the YO Phase Lock Loop. This is in addition to the phase-locked error correction by YO TUNE. For YO sweep widths < 500 kHz, VSWP is dissabled, and YO TUNE alone supplies the correction to keep the YO phase-locked for the entire sweep ramp voltage.

SWEEP GENERATOR DESCRIPTION

Introduction

The assemblies documented in this functional group that cause the frequency of the 8340A to sweep are A58 Sweep Generator, A54 YO Pretune/Delay Compensation board, and A55 YO Driver.

When the YO loop phase-locks at the start frequency of an instrument sweep or at the start of a new band, the A54 YO Pretune/Delay Compensation board provides PRETUNE voltage to the A55 YO Driver. PRETUNE is a dc voltage proportional to the frequency at which the YO is locking. The sensitivity of this voltage is -2.5 volts/GHz. The A55 YO Driver converts this voltage to a current which is also proportional to the lock frequency. This current is fed to the YO Main Coil where it tunes the frequency of the YO to be within the phase-lock range of the YO loop.

For sweep widths >5 MHz, the A49 YO Loop Phase Detector opens the YO phase-locked loop by activating the sample and hold, thus holding YO TUNE constant at its phase-locked value. The A58 Sweep Generator then provides a voltage ramp which is summed with the PRETUNE voltage on the A54 YO Pretune/Delay Compensation board. The resulting voltage ramp produces a current ramp from the A55 YO Driver board which in turn sweeps the frequency of the YO.

VSWP is also used on the A54 YO Pretune/Delay Compensation board to produce another negative going ramp called VCOMP. This is added to PRETUNE on the A55 YO Driver board to compensate for the eddy-current induced swept frequency error inherent in the YO magnetic structure.

When a bandcrossing or end of sweep is reached, LBX (Low Bandcross) and HSP (High SweeP) are pulled LOW by the A57 Marker/Bandcross board. This causes VSWP to pause (stop ramping). Then the instrument processor pulls LRSP (Low Reset SweeP) LOW which resets VSWP to zero volts.

To erase the magnetic memory of the YO magnetic structure, the instrument processor initiates a retrace kick via the YO RETRACE KICK PULSE Generator (Block **G**) in the A54 YO Pretune/Delay Compensation board. This pulse is summed with the PRETUNE voltage. The effect is to temporarily offset the YO frequency by approximately -2.5 GHz. This intializes the domains in the YO magnets.

Finally, the instrument processor sets PRETUNE to a value proportional to the next lock frequency. When the loop is locked, the sweep sequence is repeated.

In sweeps where the YO is to move less than 5 MHz, the 20-30 loop is swept and the YO loop remains phase-locked. Since the YO loop is phase-locked to the 20-30 loop output, the YO frequency will follow that of the 20-30 Loop.

The 20-30 Loop is swept by a voltage ramp, 20-30 SWP, generated by the A58 Sweep Generator board. For YO sweeps <500 kHz, the Sweep Width Range Attenuator on the A58 Sweep Generator board is open-circuited so that VSWP remains at zero volts.

START/STOP Sweep Operation

Starting and stopping of the sweep ramp is controlled primarily by HSP (High SweeP), which is generated on A57 Marker/Bandcross board. When HSP is HIGH, the A58 Sweep Generator is free to sweep. When HSP is LOW, the A58 Sweep Generator stops, but does not reset sweep voltage, VSWP.

The A57 Marker/Bandcross board pulls HSP LOW, stopping the sweep whenever any one of the following three events takes place.

(1) LBX (Low Bandcross) goes LOW. The A57 Marker/Bandcross board pulls LBX and HSP LOW at bandcrossings and at the end of the sweep. The A58 Sweep Generator pulls LBX LOW if there is an instrument malfunction which allows VSWP to go beyond its normal limits.

(2) LSSP (Low Stop SweeP) on the rear panel is pulled LOW. Note: this line is meant for special, dedicated applications and is not designed to be a general purpose stop sweep input.

(3) The instrument processor issues a STOP SWEEP.

The A57 Marker/Bandcross board drives HSP HIGH, starting a sweep whenever any one of the following three events takes place.

(1) A line trigger input is received after line trigger mode has been selected.

(2) An external trigger input is received after external trigger mode has been selected.

(3) The instrument processor issues GO SWEEP IMMEDIATE.

(4) LSSP on the rear panel goes HIGH after the instrument processor has completed its tasks and is waiting for the input.

The A57 Marker/Bandcross board keeps track of when to initiate

the various sweep events (marker on/off, bandcross, and end of sweep) by monitoring MARKER RAMP. This is a zero to ten volt ramp generated by the A58 Sweep Generator board. A buffered version of this, SWEEP OUTPUT, is available on the front and rear panels. MARKER RAMP is a monotonic ramp with pauses for bandcrossings. It starts at zero at the beginning of each sweep. It reaches five volts at the center frequency of the sweep and goes to ten volts at the end of the sweep.

YO LOOP DESCRIPTION

Introduction

The assemblies (documented in this functional group) that comprise the YO Loop are A44 YO, A45 Pre-Leveler, A46 7 GHz Low Pass Filter, A48 YO Loop Sampler, A49 YO Loop Phase Detector, A50 YO Loop Interconnect, A54 YO Pretune/Delay Compensation, and A55 YO Driver.

In the CW and Manual Sweep instrument modes, the YO Loop phase-locks the YO at the appropriate frequency. The information to tune the YO comes from two sources, PRETUNE and YO TUNE, which combine to form the YO FM COIL DRIVE and the YO MAIN COIL DRIVE.

Pretune

The PRETUNE voltage is generated on the A54 YO Pretune/Delay Compensation board. It is the scaled sum (A54, Block **C**) of VDAC, a tune voltage generated from inputs from the instrument processor, and VREF, a constant dc offset voltage. PRETUNE has a sensitivity of -2.5V/GHz YO.

LKICK and VCOMP have no contribution to PRETUNE in the CW/Manual Sweep instrument modes. LVSX (Low Voltage Sweep disable) is LOW to shunt out any unwanted noise contribution from the VSWP line.

YO Tune

The YO TUNE voltage is generated by the A49 YO Loop Phase Detector from the 20-30 MHz input (from the 20-30 Loop) and the Sampler IF, which is the down-converted product of the YO RF OUTput and the Nth harmonic of the M/N OUTput. The A45 Preleveler couples a portion of the YO Output back through the A46 7 GHz Low Pass Filter to the A48 YO Loop Sampler. There it is mixed with the Nth harmonic of the M/N Output to produce the Sampler IF, which is in the frequency range of 20-30 MHz. This signal and the one from the 20-30 Loop are compared in the Phase/Frequency Detector (A49, Block **D**) of the A49 YO Loop Phase Detector. The resulting error signal is amplified and integrated to produce YO TUNE, with a sensitivity of -3 MHz/Volt. When HLEY (High Lock Enable Yig Oscillator) is HIGH, the YO Loop is closed. When HLEY is LOW, the Sample And Hold (A49, Block **H**) holds constant the phase-locked value of YO TUNE, thus breaking the loop to allow a voltage ramp (VSWP) to be summed into PRETUNE to sweep the YO.

YO FM Coil Drive

The FM Coil Driver (A49, Block **I**) has a 100 Hz high pass filter, so that only the high frequency (>100 Hz) portion of YO TUNE is applied to the YO FM Coil. The resulting output is the YO FM COIL DRIVE current. The low frequency portion (<100 Hz) of YO TUNE is summed with PRETUNE and applied to the YO Main Coil.

YO Main Coil Drive

The YO MAIN COIL DRIVE current is derived at the A55 YO Driver from the PRETUNE and YO TUNE voltages. YO TUNE is summed (A55, Block **E**) with the OFFSET voltage, and PRETUNE is scaled (A55, Block **A**) by the GAIN adjustment. The YO MAIN COIL DRIVE current is constructed as a linear function of the desired YO frequency. The OFFSET adjustment varies the offset of the curve; the GAIN adjustment varies the slope. These two adjustments are used to ensure the tuning accuracy of the YO versus PRETUNE voltage over its full range of operating frequency. OFFSET has greater effect on the low end of the range (2.30 GHz), and GAIN has greater effect on the high end (6.99 GHz).

The Voltage-to-Current Converter (A55, Block **B**) on the A55 YO Driver and the A47 Sense Resistor Assembly are part of the same circuit. (A47R6 and A47Q1 are located externally to be properly heat sunk.) This circuit converts the (scaled) sum of the PRETUNE and YO TUNE voltages to the YO MAIN COIL DRIVE current that drives the YO Main Coil. This completes the YO loop which tunes and phase-locks the YO.

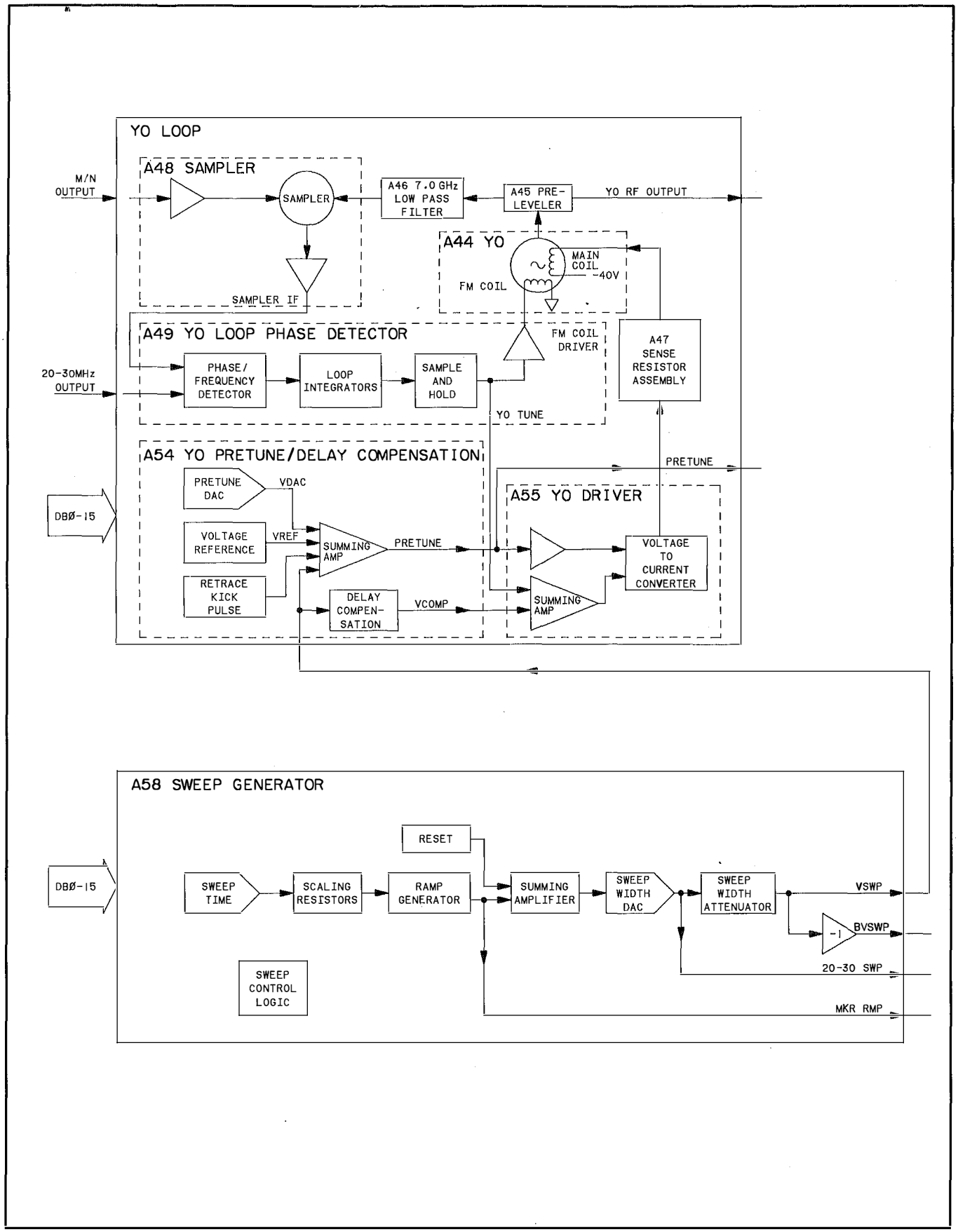


Figure 8D-1. Sweep Generator and YO Loop, Block Diagram

SWEEP GENERATOR - YO LOOP
TROUBLESHOOTING TO ASSEMBLY LEVEL

YO LOOP TROUBLESHOOTING

Introduction

The YO UNLOCKED error condition can be caused by a number of different failure mechanisms. The YO Loop Troubleshooting Flow Chart, Figure 8D-2a, provides a systematic way to identify the board or boards at fault for the majority of the cases. Refer also to the Sweep Generator and YO Loop Block Diagram, Figure 8D-1. Each of the following headings refer to the Troubleshooting Flow Chart and assumes that the Front Panel UNLK indicator is lit.

YO UNLK - CW/MANUAL Mode

The instrument UNLK diagnostics can be selected by pressing **[SHIFT] [EXT]** on the front panel. This will display the following:

OSC: REF M/N HET YO N2 N1

A YO unlock condition exists when the "YO" indicator is flashing.

In the majority of cases, the error condition will occur in the CW/MANUAL mode, and the troubleshooting should be done in this mode first. If the YO Loop will not acquire phase-lock in CW/MANUAL at all frequencies, then it will also not function properly in the SWEPT mode.

To troubleshoot in the CW/MANUAL mode, answer the following questions:

(1) ARE OTHER LOOPS LOCKED?

Check to see that the UNLK indicators for the REF, M/N, N2, and N1 loops are not also flashing. If these other loops are unlocked, then the YO Loop will not function correctly; troubleshoot the other loops first. If they are all locked, then proceed to question 2.

(2) IS FRONT PANEL RF POWER OK?

Check that RF is present at the front panel at a level close to the selected power. If not, there is a problem in the RF path; go to question 14. If the front panel RF is present at the correct

power, then proceed to question 3.

(3) IS YO FREQUENCY WITHIN ±25 MHZ?

The correct YO frequency can be found by pressing **[SHIFT] [M2]** on the front panel that will display the following:

BAND # YO FREQUENCY (MHz)

Typically PRETUNE will tune the YO within ±5 MHz. YO tune can change the YO frequency by ±20 MHz (capture range of YO Phase Lock Loop).

If the YO frequency offset is more than ±25 MHz, then the offset is more than the YO TUNE can normally cause; go to question 17. If the YO offset is less that 25 MHz, then the problem is most likely with YO TUNE; proceed to question 4.

(4) IS YO TUNE AT MAXIMUM POSITIVE OR NEGATIVE? (APPROXIMATELY ± 6.9 V)

This test must be made at a CW frequency that exhibits the UNLK error condition. The YO TUNE and FM COIL cables must remain connected so that the YO Loop is closed. Check the YO TUNE voltage at TP3 (TUNE) on the A55 YO Driver. When the loop is operating properly, the YO TUNE voltage should be close to zero volts. If YO TUNE is within the range of nominally +6.0 V dc, then the YO Loop is locked and the UNLK indication is false; proceed to question 5. If YO TUNE is at maximum positive or negative (approximately ±6.9 V), then the YO Loop is unlocked; go to question 6.

NOTE:

In the CW/MANUAL mode, whenever the YO is locked, YO TUNE should be within the range of ±2 V dc. If the actual magnitude is between 2V and 6V dc, then proceed to question 5 and 6, and then return to question 4. If the actual magnitude of YO TUNE is greater than approximately 6.9 V, then troubleshoot the A49 YO Loop Phase Detector board.

(5) IS HULY HIGH?

If the YO Loop is actually locked but HULY (High UnLock Yig oscillator) is HIGH indicating unlock, then the Unlocked Detector on the A49 YO Loop Phase Detector is at fault. If HULY is LOW, then the problem is on the A59 Digital Interface board.

(6) IS HLEY HIGH?

HLEY (High Lock Enable Yig oscillator) must be HIGH for the YO Loop to lock. If HLEY is LOW or intermittent, then troubleshoot the A59 Digital Interface board. If not, then proceed to question 7.

(7) IS M/N OUTPUT FREQUENCY AND POWER OK?

Check for the proper M/N signal frequency and power at the output of A33J2. The correct frequency can be found by pressing **[SHIFT] [M1]** on the front panel that will display the following.

M #	N #	M/N FREQUENCY (MHz)	20-30 FREQUENCY (MHz)

The correct M/N signal power is 0 dBm ±3 dB. If no signal is present or if the power and/or frequency is incorrect, then troubleshoot the M/N Loop. If the M/N signal is correct, then proceed to question 8.

(8) IS 20-30 OUTPUT FREQUENCY AND POWER OK?

Check for the proper 20-30 signal frequency and power at the output of A36J2. The correct frequency can be found by pressing SHIFT M1 on the front panel (see question 7 above). The correct power is 0 dBm ±3 dB. If no power is present or if the power and/or frequency is incorrect, then troubleshoot the 20-30 Loop. If the signal is correct, then proceed to question 9.

(9) IS THE YO FREQUENCY CHANGE PROPORTIONAL TO YO TUNE?

Record the actual YO frequency. Then disconnect YO TUNE and FM COIL DRIVE, cables A49J1 and A49J2. Place a 50 Ohm load on the YO TUNE cable, A49J2. (These cables will remain disconnected for the remainder of the troubleshooting.)

Note the YO frequency now and compare it with the value recorded before the cables were removed. It should have changed approximately 20 MHz. The YO frequency sensitivity to YO TUNE is approximately -3.0 MHz/Volt. If the frequency does not change or else changes an amount much greater than 20 MHz, this indicates a problem on the A55 YO Driver (Block **E**).

If the frequency change is proportional to the YO TUNE voltage, then proceed to question 10.

(10) IS THE OPEN-LOOP YO FREQUENCY ACCURACY ±5 MHz AT 2.300 AND 6.999 GHz?

With the YO TUNE and FM COIL cables disconnected (and a 50 Ohm load on the YO TUNE cable, A49J2), the YO frequency accuracy should be within a ±5 MHz window over the entire YO operating range. The YO accuracy should be checked at 2.300 and 6.999 GHz. If the actual YO frequency is outside of these limits, then go to question 17; if not, then proceed to question 11.

(11) IS SAMPLER IF FREQUENCY AND POWER OK?

Check for the correct frequency and power for the SAMPLER IF. The frequency accuracy (open loop) should be ±5 MHz, the same as the YO. If the SAMPLER IF frequency and power are correct, then troubleshoot the A49 YO Loop Phase Detector; if not correct, then proceed to question 12.

(12) IS RF POWER INTO THE A48 YO LOOP SAMPLER OK?

Check the RF signal power into the A48 YO Loop Sampler. If the RF power is correct, then troubleshoot the A48 YO Loop Sampler. If no signal is present or if the power is incorrect, then proceed to question 13.

(13) IS PRE-LEVELER POWER OUT OF A45J2 OK?

Check the coupled-back RF power out of the A45 Preleveler at A45J2. If no signal is present or the power level is incorrect, then troubleshoot the A45 Preleveler. If the RF power is correct, then troubleshoot the A46 7 GHz Low Pass Filter and connecting cables.

(14) IS PRE-LEVELER POWER OUT OF A45J3 OK?

This portion of the troubleshooting guide is a branch from question 2.

Check the RF power out of the A45 Preleveler at A45J3. If the signal is present at the correct power, then a problem also exists in the Main RF path. To continue to troubleshoot the YO UNLK, however, go to question 3. If no signal is present or if the power output is low, then proceed to question 15.

(15) IS YO POWER OUT OK?

Check the RF power out of the YO. If the power is correct, then troubleshoot the A45 Preleveler. If no signal is present or if the power is low, proceed to question 16.

(16) IS THE YO MAIN COIL DRIVE OK?

Check the YO MAIN COIL DRIVE. This can be done by testing the

SENSE voltage, TP4 on the A55 YO Driver board. (The SENSE voltage is related to the YO frequency by -2.4 V/GHz.) If the YO Main Coil is greatly mistuned, then no YO signal will be present. If the SENSE voltage (hence the YO MAIN COIL DRIVE current) is correct to within ±1 V, then troubleshoot the YO; if not, then proceed to question 17.

(17) IS THE PRETUNE VOLTAGE OK?

This portion of the troubleshooting guide is a branch from question 3, question 10, and question 16.

Check the PRETUNE voltage. PRETUNE has a sensitivity of -2.5 V/GHz of YO frequency. If the PRETUNE voltage is correct, then troubleshoot the A55 YO DRIVER (OFFSET and GAIN) and the A47 Sense Resistor Assembly. If PRETUNE is not correct, then proceed to question 18.

(18) IS THE VSWP VOLTAGE OK?

Check the VSWP voltage; it should be zero volts. If it is correct, then troubleshoot the A54 YO Pretune/Delay Compensation board. If VSWP is much different than zero volts, then proceed to question 19.

(19) IS LVSX LOW?

If the VSWP voltage is much different than zero volts, it will affect the PRETUNE voltage only if the Sweep Disable Switch (A54, Block **E**) is also not operating correctly. If LVSX (Low Voltage Sweep Disable) is HIGH or intermittent, then troubleshoot the A59 Digital Interface board. If LVSX is LOW (that should be the case for CW/MANUAL), then troubleshoot Block **E** on the A54 YO Pretune/Delay Compensation board. In either case, also troubleshoot VSWP on the A58 Sweep Generator board.

YO UNLK - Swept Mode

To troubleshoot in the swept mode with the YO unlocked, answer the following questions:

(1) IS CW/MANUAL MODE OK?

If the YO UNLK error condition can be made to occur in the CW/MANUAL mode, then go to the YO UNLK - CW/MANUAL troubleshooting section. It will also be helpful if the YO UNLK condition can be made to occur in the SINGLE SWEEP mode, for this will hold the YO Loop (error) condition constant while troubleshooting.

If the error condition can only be made to occur in the SWEPT mode and CONTINUOUS SWEEP mode, then the error will be more difficult to resolve. Proceed to question 2 in this section. There are several mechanisms that could cause a YO Loop unlock in only the SWEPT mode; these relate to the function and operation of VSWP, LKICK, HLEY (High Lock Enable Yig Oscillator), and possibly VCOMP, LVSX, and LYSP. Most of the potential causes of the error are related to timing, mainly at the start of sweep.

(2) IS VSWP OK?

Check to see that VSWP is at zero volts at the start of each sweep. LVSX (Low Voltage Sweep Disable) is HIGH in SWEPT mode for sweep widths > 500 kHz, but LOW in CW/MANUAL. Thus, any offset in VSWP would only affect the YO tuning in the SWEPT mode. Because of the high sensitivity of the YO frequency to VSWP (500 MHz/V), an offset of as little as 50 mV added from VSWP to PRETUNE will result in the YO being tuned outside of the capture range of the YO Phase Locked Loop. If VSWP is zero, then proceed to question 3. If VSWP is not zero, then troubleshoot the A58 Sweep Generator board.

(3) IS THE YO KICK PULSE OK?

Check to see that the YO Kick Pulse is being generated correctly. The LKICK line should be < 2V for a time at the start of the sweep and then return to zero volts before the sweep occurs. PRETUNE should also change a proportional amount. (It is normal for PRETUNE to have an intermediate voltage step if the PRETUNE DAC, A54 Block **B**, is set before the end of the kick pulse.) If the YO kick pulse, LKICK, is not generated, or if it does not return to zero volts, then troubleshoot the A54 YO Pretune/Delay Compensation board. If LKICK is good, then proceed to question 4.

(4) IS HLEY HIGH AT START OF SWEEP?

Check the HLEY (High Lock Enable Yig oscillator) voltage at the start of sweep. If it is LOW or intermittent, then the YO Loop will not lock; troubleshoot the A59 Digital Interface Board.

SWEEP GENERATOR TROUBLESHOOTING

Introduction

There are two basic failure modes that have to do with the sweep function of the instrument. One, the instrument is simply not sweeping. Two, it is sweeping, but the sweep is incorrect; the frequency limits of the sweep are wrong and/or bandcrossings are not occurring. The first task is to get the instrument to do repetitive sweeps of any kind.

If the MARKER RAMP is sweeping zero to ten volts and the Front Panel LED is blinking then the instrument is considered to be sweeping even though the output frequency may not be moving. If, on the other hand, MARKER RAMP is stuck and the front panel sweep LED is continuously on or off, then the instrument is not considered to be sweeping. When looking at the LED, care must be taken because in fast sweeps it may appear to be on all the time, even though it is actually blinking.

No Sweep

Assuming that the instrument processor is functioning correctly, the only external lines that can prevent the A58 Sweep Generator from sweeping are HSP (High SweeP), LBX (Low Bandcross) and LRSP (Low Reset SweeP). HSP and LRSP are standard TTL lines with HSP being driven by the A57 Marker/Bandcross board and LRSP being driven by the A59 DIGITAL INTERFACE board. LBX is an open collector line that can be driven by both the A58 Sweep Generator and A57 Marker/Bandcross boards. HSP is coupled to LBX on the A57 Marker/Bandcross board so that if LBX is pulled down, the A57 Marker/Bandcross board pulls down on HSP also.

If the instrument is in the continuous sweep mode and is not sweeping, then remove the A57 Marker/Bandcross board. If the instrument now sweeps, the problem is most likely on the A57 Marker/Bandcross board. Note that in this mode, the frequency limits that the instrument is sweeping over will not be correct. This is because it is the OVER SWEEP DETECTOR (Block **U**) on the Sweep Generator that is pulling down on LBX to stop the sweep when the MARKER RAMP reaches 12 volts.

If the instrument still will not sweep with the A57 Marker/Bandcross board removed, next check the state of the HSP line. Since only the A57 Marker/Bandcross board can pull down on this line, it should be HIGH in this mode. If it is LOW, then troubleshoot this problem. If HSP is HIGH, then check the state of LBX. If it is LOW, then determine what is pulling it down by looking at HBX on the A58 Sweep Generator. If HBX is HIGH, then the OVER SWEEP DETECTOR is pulling down on LBX. If HBX is LOW,

then something off the board is at fault.

Finally, look at LRSP, TP11, on the A58 Sweep Generator board. If it is stuck LOW, troubleshoot this problem.

If the three lines just discussed, LBX, HSP and LRSP are all HIGH, then the problem is indeed on the Sweep Generator board. Reinstall the Marker/Bandcross board and consult the troubleshooting section for the A58 Sweep Generator board.

Incorrect Sweep

If the instrument sweeps, as defined above, but the YO does not sweep or the frequency limits are incorrect, check the two sweep ramps from the A58 Sweep Generator board, 20-30 SWP (TP8) and VSWP (TP10). The sensitivities of these lines are discussed below.

YO sweeps widths >5 MHz are derived from VSWP. Note that the instrument sweep width, delta F, is related to the YO sweep width by the harmonic number of the band being used. For example, if the instrument is sweeping from 8 to 10 GHz, the instrument sweep width is 2 GHz. However, this is the second harmonic of the YO so that the YO is sweeping from 4 to 5 GHz; a sweep width of 1 GHz. The sensitivity of VSWP is +2 volts/GHz of YO sweep width. In the example above, VSWP should be a ramp starting at zero and going to +2 volts.

If VSWP is correct, then look at PRETUNE (TP3) on the A54 Pretune/Delay Compensation board. It has a sensitivity of -2.5 volts/GHz of YO frequency. In the foregoing example where the YO swept from 4 to 5 GHz, PRETUNE should go from -10 to -12.5 volts.

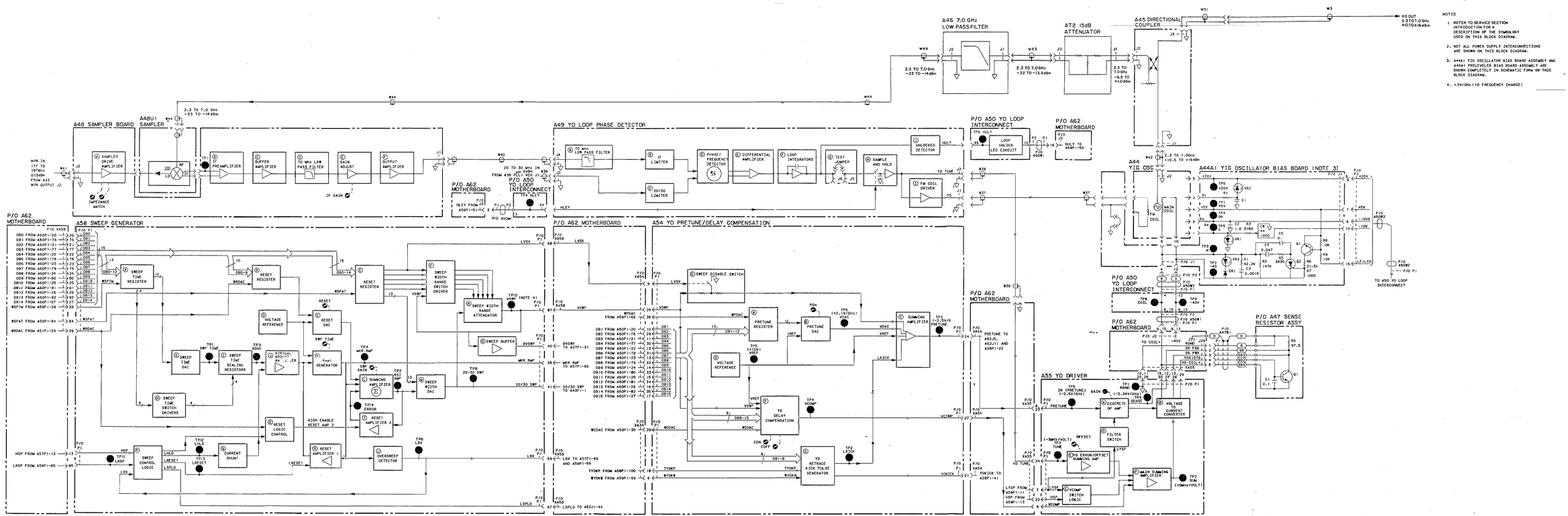
If PRETUNE is correct, look at SENSE (TP4) on the A55 YO Driver board. This point has a sensitivity of about -2.34 volts/GHz of YO frequency. If this is correct, the problem is most likely in the A44 YIG Oscillator assembly.

YO sweep widths $\leq$ 5 MHz are derived from 20-30 SWP. The sensitivity of 20-30 SWP is related to YO sweep width but changes depending upon the particular sweep width selected, as shown in Table 8D-1.

Table 8D-1. Sensitivity of 20-30 SWP Line

SWEEP WIDTH	SENSITIVITY
5 MHz ≥ YO sweep width > 500 KHz	500 KHz/volt
500 KHz ≥ YO sweep width > 100 KHz	50 KHz/volt
100 KHz ≥ YO sweep width > 10 KHz	10 KHz/volt
10 KHz ≥ YO sweep width > 1 KHz	1 KHz/volt
5 KHz ≥ YO sweep width > 500 Hz	500 Hz/volt
500 Hz ≥ YO sweep width > 100 Hz	50 Hz/volt

Verify that VSWP is not sweeping more than 0.0 to 15 mV and that 20-30 SWP is correct. If both of these are correct, the problem is most likely in the 20-30 Loop.



Scans by HB9HCA and HB9FSX

Figure 8D-2a. Sweep Generator and YO Loop Troubleshooting Block Diagram

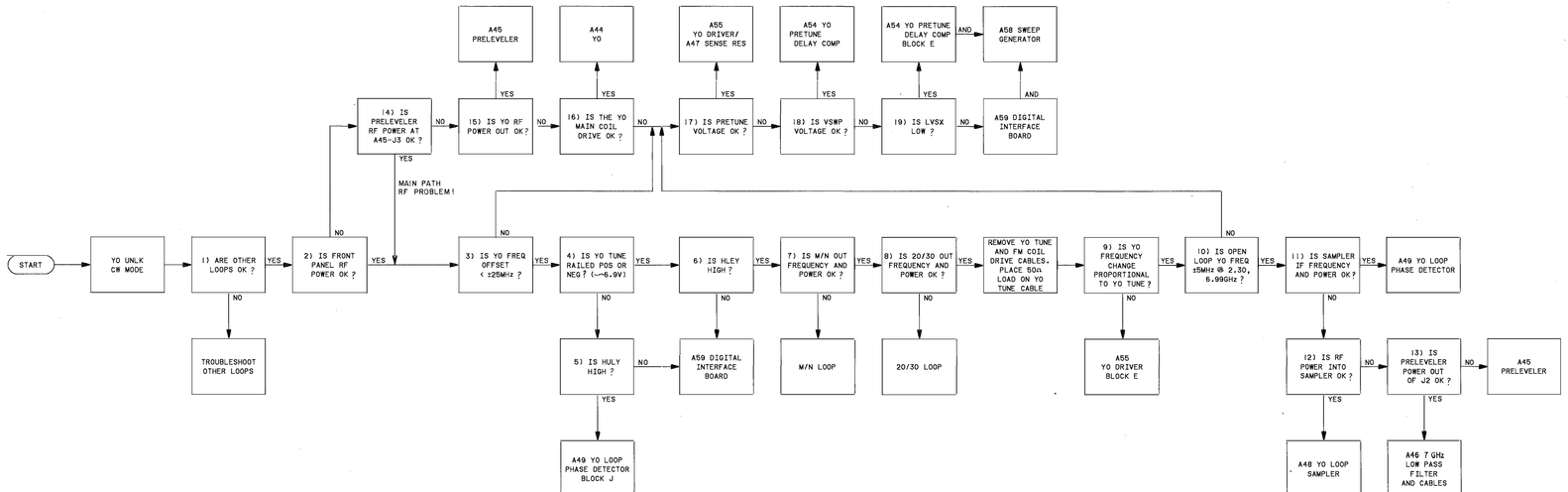


Figure 8D-2b. Sweep Generator and YO Loop Troubleshooting Flowchart

REPAIR PROCEDURES

Refer to the **REPAIR PROCEDURES** description in the beginning of Section VIII.

CAUTION

Disengage W3 from where it connects to the YO Loop via a hole in the motherboard (refer to Figure 8I-8, View C, in the RF Section) before lifting out the YO Loop or damage to the instrument will result.

When replacing the YO Loop assembly be careful not to smash the ribbon connector, A50W1.

A44 YIG OSCILLATOR

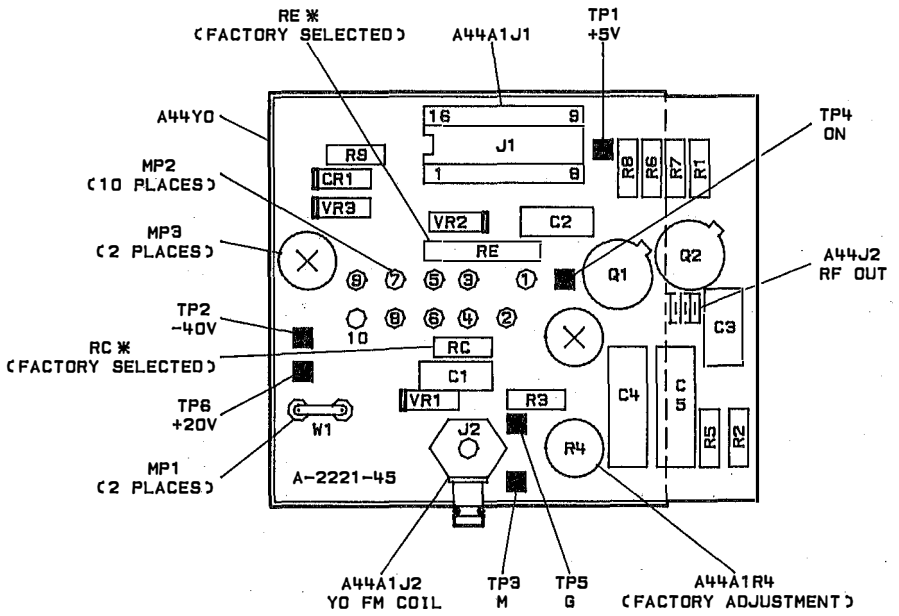
A44A1 YO BIAS BOARD CIRCUIT DESCRIPTION

Selected Resistors

Two resistors (Re and Rc) are selected when the YO is tested. A44A1R4 is adjusted to set up the proper gate bias required by the YO. The FM coil in the 8340A is connected to chassis ground at the Bias Board. During testing, however, the coil must be floating so a jumper has been provided to connect ground after testing.

YO Switchable Filtering

The filtering required at the YO main coil depends upon whether the instrument is in the CW mode or in the Swept mode. A switch circuit is provided to accomplish this filter change. A signal from the processor (HFIL) goes HIGH in CW mode. This signal is buffered on the A50 YO Loop Interconnect board by an open collector darlington inverter. The resulting signal (LFIL) goes to the YO Bias board where it pulls down on the base of Q1 through R9. This turns Q1 ON and pulls R6 UP to +5 volts. R6 and R7 form a voltage divider going to the gate of an SCR. When its gate is pulled positive with respect to its cathode, it turns ON and provides a very low impedance path for the CW filter circuit. The CW filter circuit consisting of C4, C5, and R5 is connected directly across the YO Main Coil when Q2 is ON. C5 is used to reduce the phase noise of the YO and is also effective in reducing the radiated susceptibility of the 8340A. The swept mode filter consisting of R1, R2, and C3 is used to match the delay characteristics of the YO main coil to those of the YO main coil driver circuitry.



NOTE

Refer to Sweep Generator — YO Loop Troubleshooting Block Diagram for schematic of A44.

Figure 8D-3. A44A1 YIG Oscillator, Component Location Diagram

A45 DIRECTIONAL COUPLER

A45 DIRECTIONAL COUPLER DESCRIPTION

The A45 directional coupler divides the RF Output of the A44 YO into two paths. The output of the coupled arm goes to A45J1. This signal is attenuated by AT2 and goes through the A46 7.0 GHz Low Pass Filter to the A48 YO Loop Sampler where it is mixed with the Nth harmonic of the M/N Out signal. The result is the Sampler IF signal to the A49 YO Loop Phase Detector.

The RF Signal from the coupler's main line path is the YO Out signal at A45J3. This signal is sent to the A16 Modulator/Splitter.

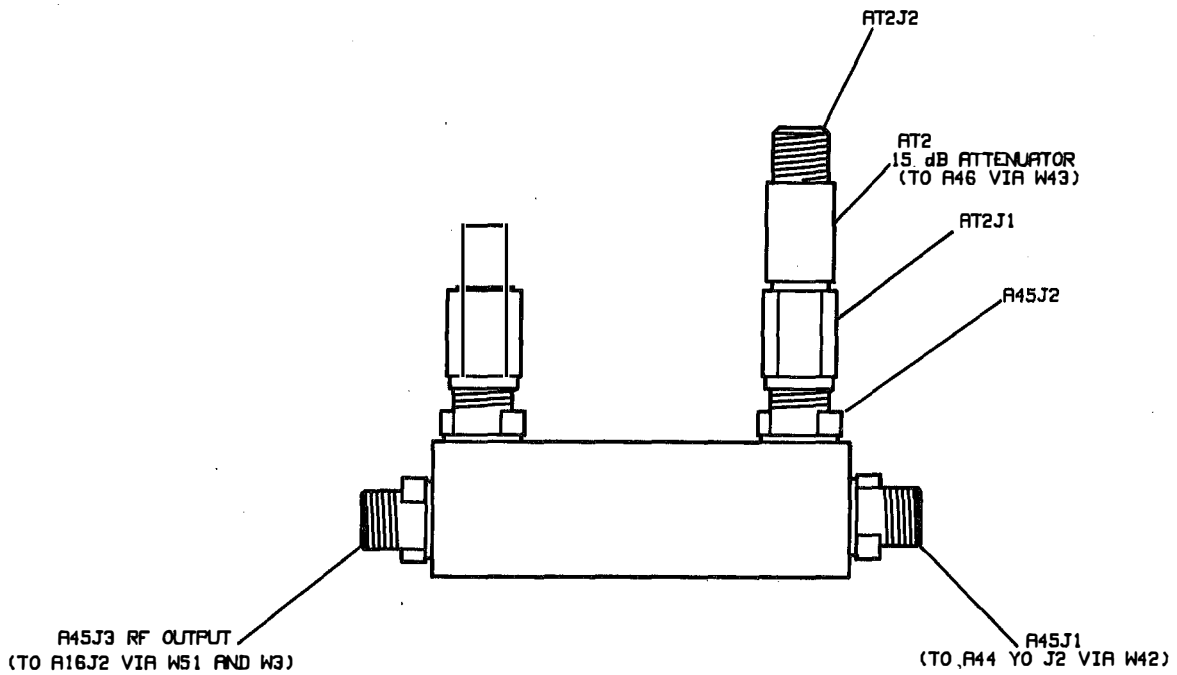
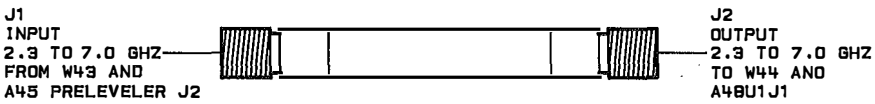


Figure 8D-4. A45 Directional Coupler Component Location Diagram

A46 7 GHz LOW PASS FILTER

A46 7 GHz LOW PASS FILTER CIRCUIT DESCRIPTION

The A46 7 GHz Low Pass Filter is connected by coaxial cables between the A45 Pre-leveler and the A48 YO Loop Sampler. It is used to filter out the harmonics of the coupled-back portion of the YO Output from the Pre-leveler to prevent unwanted mixing products in the Sampler.



NOTE

Refer to Sweep Generator — YO Loop Troubleshooting Block Diagram for schematic of A46.

Figure 8D-5. A46 7.0 GHz Low Pass Filter, Component Location Diagram

A47 SENSE RESISTOR ASSEMBLY

A47 SENSE RESISTOR ASSEMBLY CIRCUIT DESCRIPTION

The A47 Sense Resistor Assembly contains the high-power portions of the A55 YO Driver and the A28 SYTM Driver. (For the schematic of the A47 Sense Resistor Assembly, see schematics for A28 and A55.) A47Q1, A47C1, and A47R6 are part of the compound PNP transistor in the voltage-to-current converter (Block B) of the A55 YO Driver, A47R6 being the sense resistor referred to in the A55 circuit description. A47Q2 and A47R1 through 5 are part of the Current Driver (Block H) of the A28 SYTM Driver. These components are located externally so they will be properly heat sunk.

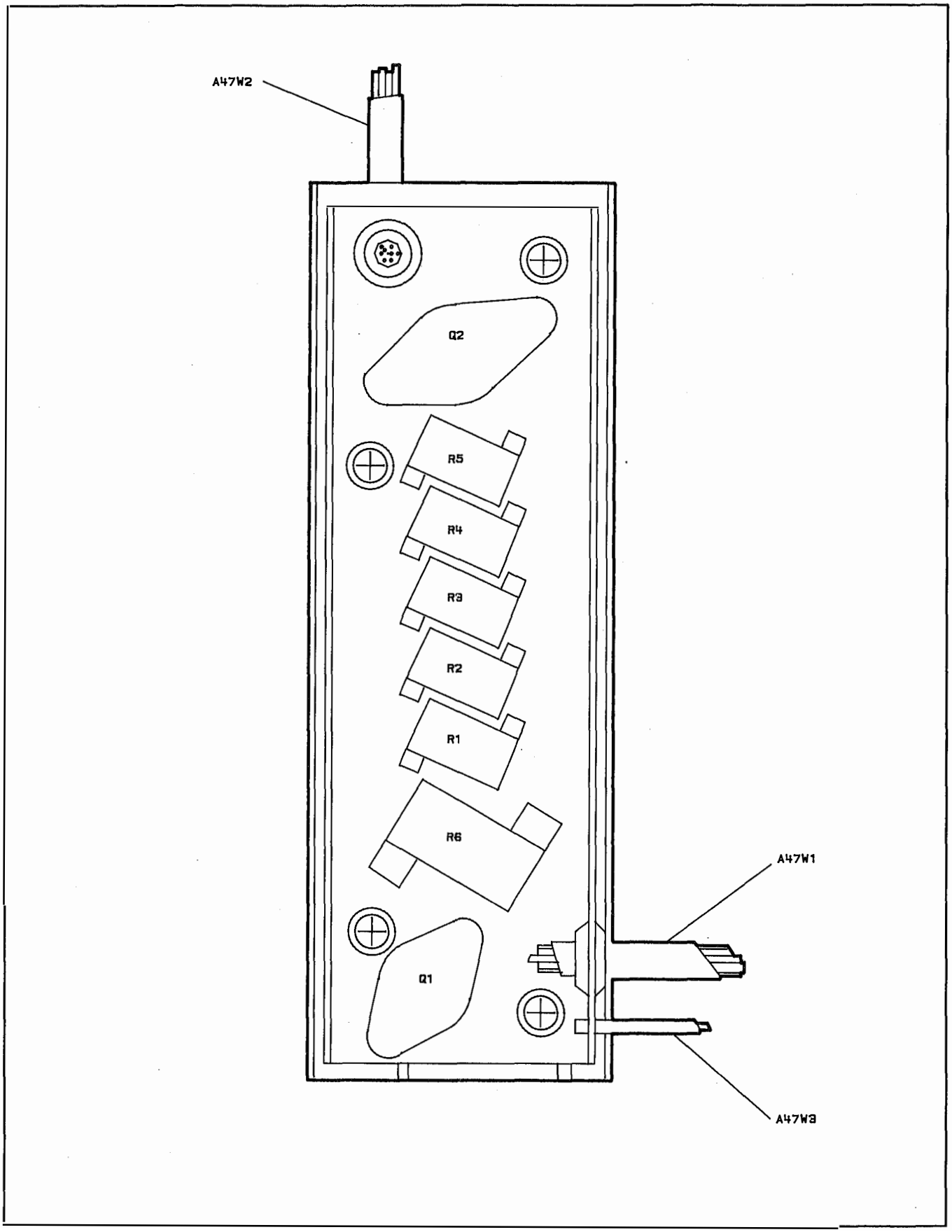


Figure 8D-6. A47 Sense Resistor Assembly, Component Location Diagram

A62J32 TO A47W2P1 PIN I/O

Pin	Mnemonic	A47W2P1	Levels
1	RGND	PIN 1	0V
2	SYTMOB	PIN 2	−22V TO −39V
3	SYTM COIL +	PIN 3	−40V TO −25V
4	SYTMDC	PIN 4	−.6V TO −6V
5	SYTMRES	PIN 5	−.9V LOW BAND CW

Note: Refer to A28 SYTM Driver Schematic Diagram and A62 Motherboard Wiring List for signal source and destination information.

A62J29 TO A47W1P1 PIN I/O

Pin	Mnemonic	A47W1P1	Levels
1	RGND	PIN 1	0V
2	SR FBK	PIN 2	−5V TO −17V
3	SR PWR	PIN 3	−5V TO −17V
4	YOXISTB	PIN 4	−30V TO −39V
5	YO COIL +	PIN 5	−40V TO −20V

Note: Refer to A55 YO Driver Schematic Diagram and A62 Motherboard Wiring List for signal source and destination information.

A48 YO LOOP SAMPLER

INTRODUCTION

The A48 YO Loop Sampler mixes the output of the A44 YO (via the A45 Pre-leveler and A46 7 GHZ Low Pass Filter) with the Nth harmonic of the output of the M/N-Reference Loop (M/N IN). The 20 to 30 MHz difference signal, SAMPLER IF, is output to the A49 YO Loop Phase Detector and is compared with the 20-30 MHz output from the A36 PLL1 VCO assembly for the purpose of phase-locking the YO.

A48 YO LOOP SAMPLER CIRCUIT DESCRIPTION

Sampler Drive Amplifier A

The output of the M/N-Reference Loop (M/N IN) is applied to common-base amplifier Q3. The output of Q3 is AC coupled to common-emitter amplifier Q8. The output of Q8 is passed through an impedance matching network that provides maximum drive power to A48U1 Sampler. Adjustments C1 and C2 optimize this impedance match.

A48U1 Sampler B

A48U1 Sampler contains a step recovery diode (SRD) circuit to create harmonics of the M/N signal which are mixed with the low-level (-15 dBm) signal from the A44 Yig Oscillator via the A46 7 GHz Low Pass Filter (LPF).

When the YO Loop is phase-locked, the mixing product of the Nth harmonic of the M/N signal and the A44 YO signal is precisely equal to the 20-30 signal from the A36 PLL1 VCO assembly. This allows the YO Loop to become phase-locked to that harmonic.

IF Preamplifier C

The IF Preamplifier consists of common-source amplifier Q4, common-emitter amplifier Q2, and feedback divider R20/R16. Overall gain provided is approximately 14 dB.

Buffer Amplifier D and 70 MHz LPF E

The A48U1 Sampler output, after being amplified, is buffered by emitter-follower Q7 and applied to the 70 MHz Low-Pass Filter (Block **E**). This filtering is done to remove any unwanted signals produced by the mixing action of the sampler.

Gain Adjust F

After being filtered, the IF signal is applied to a common-emitter amplifier Q6 which has adjustable gain. IF Gain adjustment R1 can be adjusted to provide from 5 dB to 20 dB of gain. This is used to adjust the IF signal to the proper level for comparison to the 20-30 signal in the A49 YO Phase Detector.

Output Amplifier G

The IF signal is further amplified by output amplifier Q5 and Q1. Gain is approximately 21 dB. This provides the proper signal level to drive the A49 YO Phase Detector.

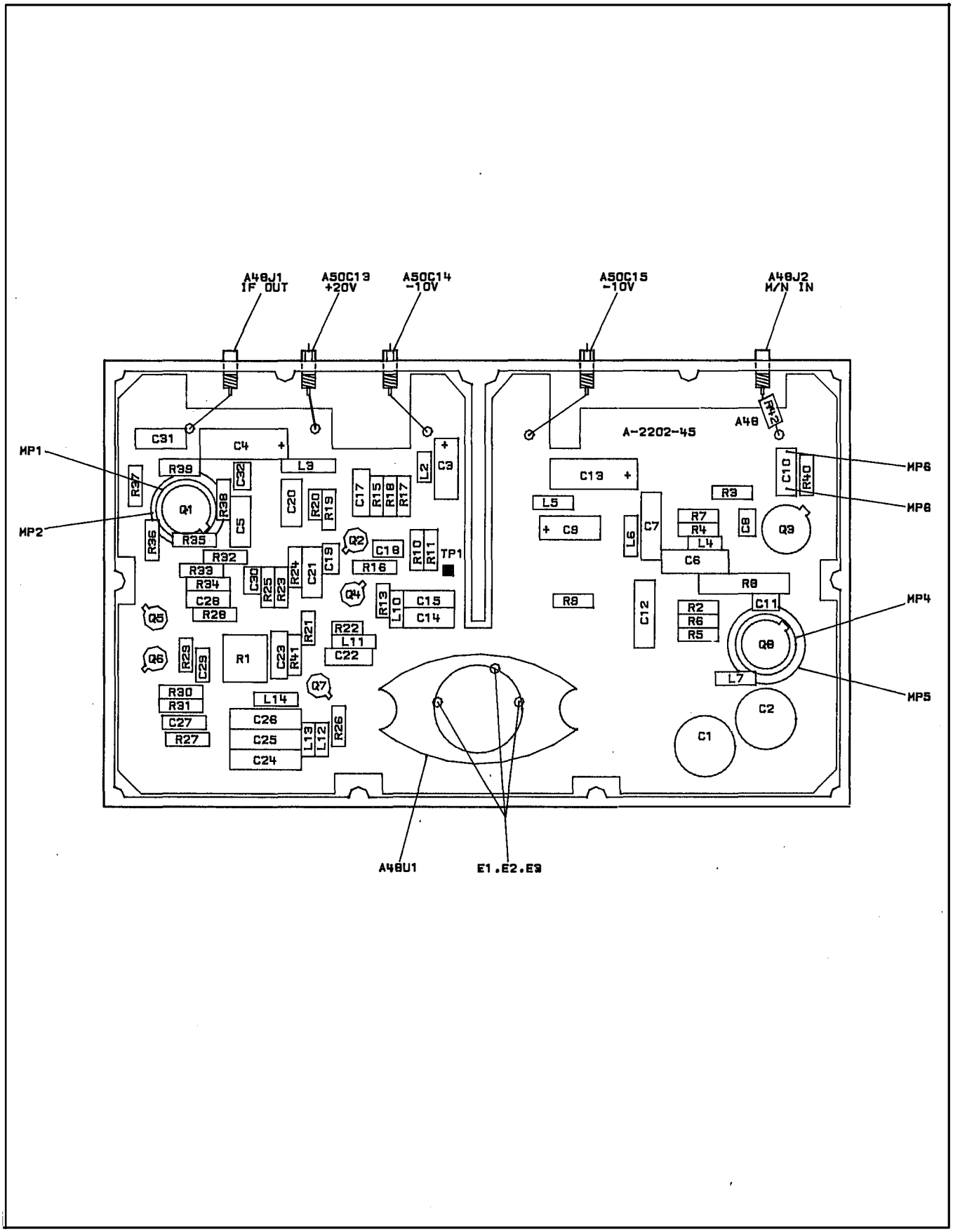


Figure 8D-7. A48 YO Loop Sampler, Component Location Diagram

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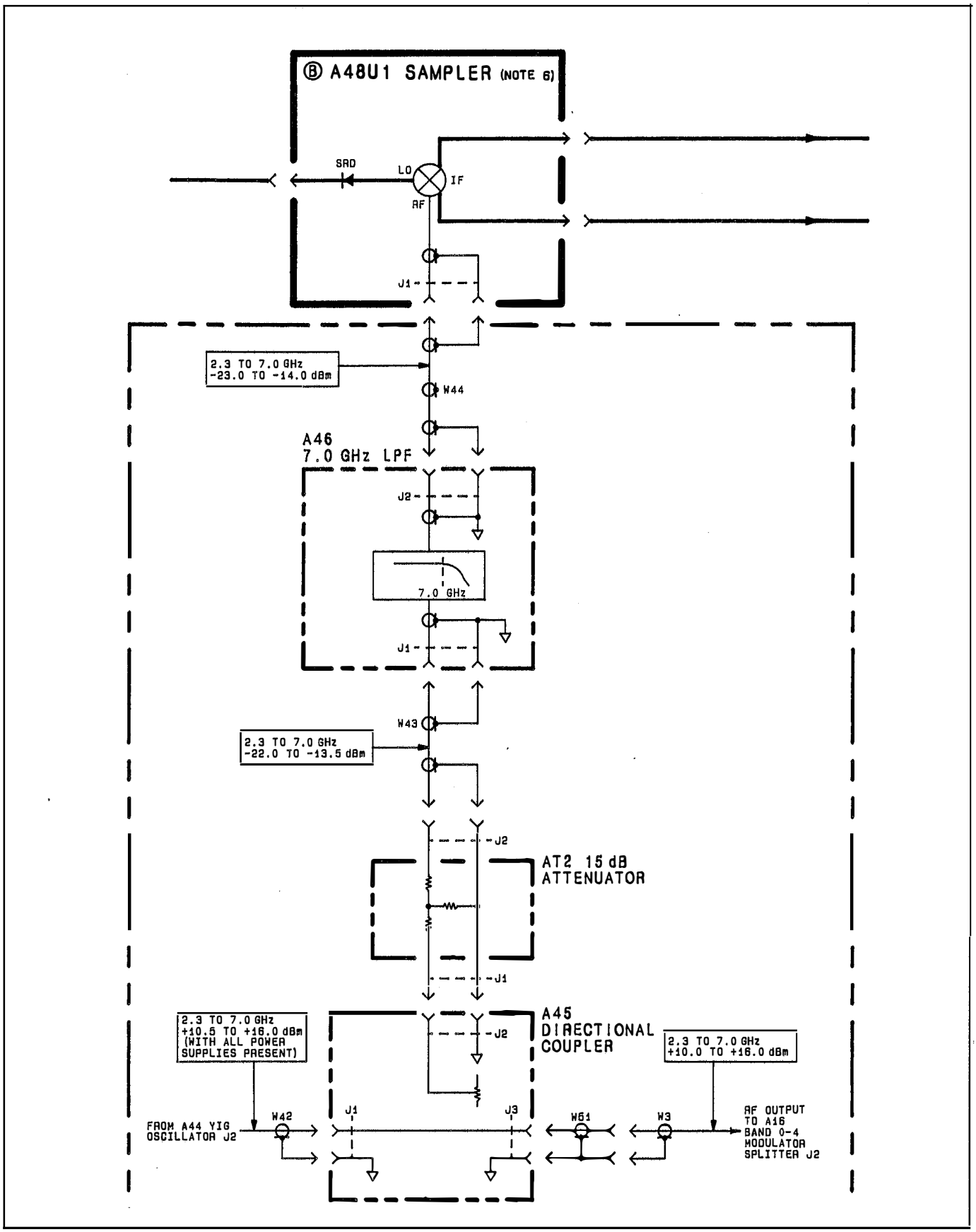


P/O Figure 8D-8. A48 YO Loop Sampler, Schematic Diagram

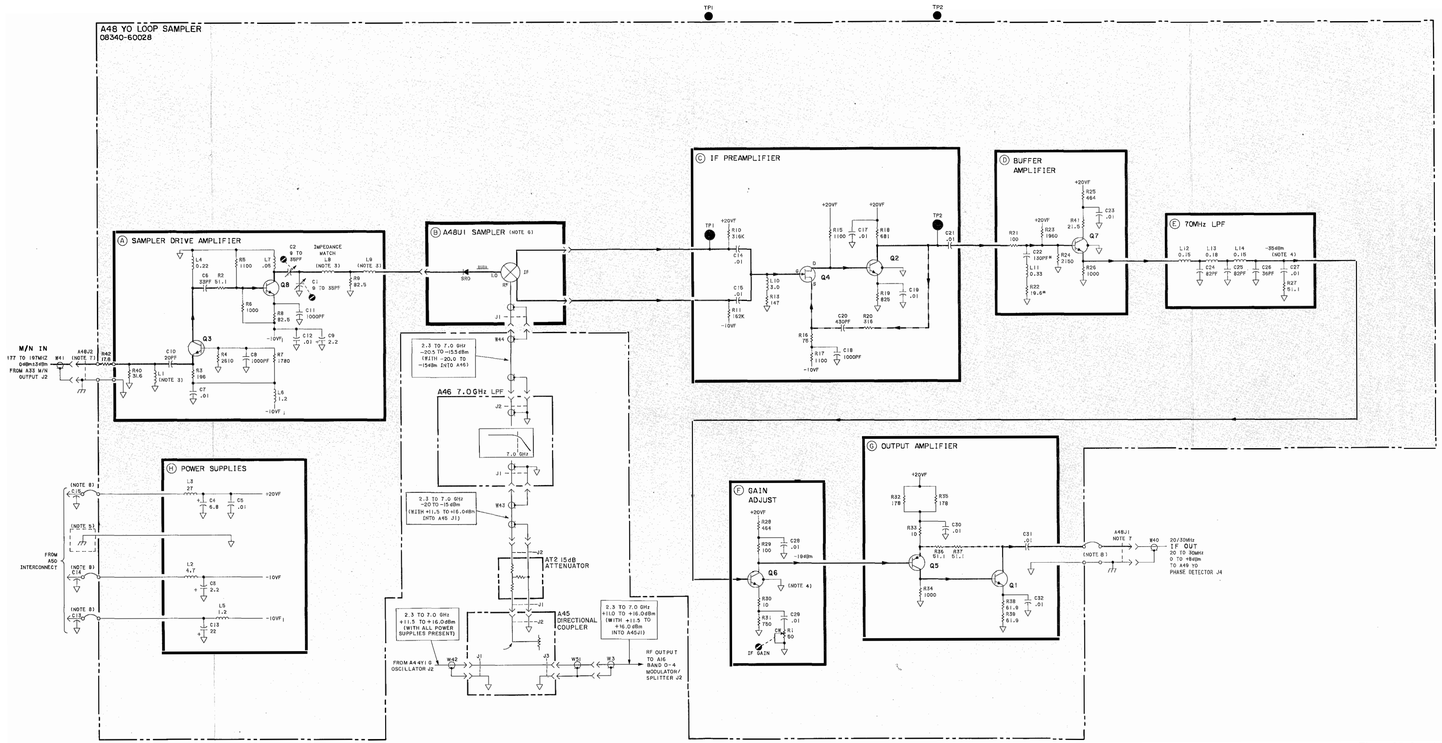


Figure 8D-8. A48 YO Loop Sampler, Schematic Diagram

A49 YO LOOP PHASE DETECTOR

INTRODUCTION

The A49 YO Loop Phase Detector Board receives as inputs the Sampler IF signal and the 20-30 signal from the A36 PLL1 VCO. These signals are phase-compared and the result is integrated to produce the YO TUNE signal as well as the FM Coil Drive signal, which are its main outputs. It also generates the High Unlock YO (HULY) signal.

The A54 YO Pretune/Delay Compensation board generates the PRETUNE voltage required to tune the A44 YO main coil to approximately the desired frequency. A portion of the YO output is coupled back to the sampler (A48U1) where the YO signal is mixed with the Nth harmonic of the output of the A33 M/N Output assembly. This generates a difference signal of 20 to 30 MHZ (Sampler IF) which is input to the A49 YO Loop Phase Detector where it is phase compared to the 20-30 MHz reference signal from the A36 PLL1 VCO. The resulting error signal tunes the YO to achieve phase-lock.

The YO frequency is related to the M/N Output frequency and the 20-30 MHz reference loop frequency in the following manner:

$$F_{YO} = (N)(Fm/n) - F20\text{-}30$$

Where:

F_{YO} = YO output frequency (MHz)
N = N number input to the M/N Loop
(harmonic near the frequency to which the YO Loop is tuned)
Fm/n = M/N Loop output frequency (MHz)
F20-30 = 20-30 Loop output frequency (MHz)
(the 20-30 frequency can be changed in 1 Hz steps)

The YO TUNE output from the A49 YO Loop Phase Detector board is routed to the A55 YO Driver board where it is summed with the Pretune voltage from the A54 Pretune/Delay Compensation board. This sum is then applied to the YO main coil. The YO FM Coil Drive from the A49 YO Loop Phase Detector board is routed to the A44A1 YO Bias board and applied to the YO FM coil.

A49 YO LOOP PHASE DETECTOR CIRCUIT DESCRIPTION

70 MHz Low Pass Filter A

The 20-30 MHz Sampler IF into the A49 YO Loop Phase Detector board is passed through the 70 MHz Low Pass Filter to remove any

unwanted frequencies which may have been introduced during the sampling process.

IF Limiter B and
20-30 Limiter C

Each of the two input signals, Sampler IF IN and 20-30 REF IN, are passed through a limiter to establish ECL signal levels and to sharpen the edges of the two signals. The limited SAMPLER IF can be measured at TP5; the limited 20-30 signal can be measured at TP4.

Phase/Frequency Detector D

The two signals, Sampler IF IN and 20-30 REF IN, are applied to the phase/frequency detector (U6). The function of U6 is to output a pulse which is related to the phase and frequency difference of the two input signals. The width of this pulse is directly proportional to the amount of phase and frequency difference. When the two signals are at the same frequency, the output is proportional to the difference in phase. If the Sampler IF signal leads the 20-30 REF signal, then a negative pulse appears at U6 pin 3 (TP 2), the width being proportional to the amount of phase difference. If the 20-30 REF signal leads the Sampler IF signal, a negative pulse appears at U6 pin 12 (TP 3). In each case, the other output pin remains at an ECL HIGH level (approximately -0.6V). If the inputs are in phase, one of the detector outputs is an ECL HIGH (approximately -0.6v) with long narrow negative spikes and the other is an ECL HIGH with short spikes. The detector outputs are averaged in a 1.5 MHz low pass filter (L8, L9, C15, C16 in Differential Amplifier Block **E**) before being applied to the differential amplifier.

Differential Amplifer E

The outputs of the 1.5 MHz filters are applied directly to Differential Amplifier Q1. The output of this differential amplifier is directly related to the difference between the Sampler IF and the 20-30 MHz REF signals. The collector supply to this differential amplifier is provided by a 15V three-terminal regulator, U5, in the Power Supplies (Block **K**) which is referenced to the instrument REFerence ground system. This was done to transform the remainder of the YO drive circuitry from the normal chassis ground to the clean, controlled reference ground.

Loop Integrators F

Integrators U4 and U7 and the Phase-Lag Filter help determine the frequency response of the loop.

Integrator U4 has a pole at f=0 and a zero at f=4000 Hz (R17 and C19). Integrator U7 has a pole at f=0 and a zero at f=400 Hz (R19 and C21). The Phase-Lag Filter (FM Coil Driver, Block I) has a pole at 400 Hz (cancelling the zero of integrator U7) and a zero at 4000 Hz (R20, R21, and C23). The YO has an inherent pole at f=0 Hz.

The combined frequency response has a slope of -60 dB/decade until f=4000 Hz where the slope changes to -20 dB/decade. The unity-gain crossover frequency (Loop Bandwidth) is set to nominally 50 kHz by varying the gain of integrator U7. The effect of this frequency response is to provide high gain at frequencies below 4000 Hz and thus reduce (proportional to the loop gain) the YO close-in phase noise and line-related spurs.

R18 is a selected resistor which may be adjusted upward in value to reduce the YO Loop Bandwidth or downward to increase the YO Loop Bandwidth.

If the A55 YO Driver board is misadjusted (Offset and Gain adjustments), there will be a dc offset voltage at the INTG output. There is normally a small offset at any given frequency due to non-linearities in the YO tracking, but the value should vary about zero volts. If the average value is different from zero, it will limit the capture range of the loop.

The resistor-capacitor combinations of R39-C17, R40-C18, R41-C30, and R42-C31 are used to provide additional filtering of the power supply inputs to U4 and U5. R30 and R31 are used to protect the inputs of U4 and U5 from being damaged by a dc voltage accidentally applied to pins 2 or 3 during troubleshooting.

Test Jumper G

The test jumper provides a way to break the YO Loop and insert a test fixture to measure the loop gain, bandwidth, and phase margin.

Sample And Hold H

The purpose of the Sample and Hold (U3 and associated circuitry) is to apply the integrated output of the phase-detector to the YO to tune the YO and achieve phase-lock. It then holds this dc voltage during the sweep to improve the swept frequency accuracy. This is called Lock and Roll.

The Sample and Hold has two modes of operation:

- Sample Mode - This is essentially the no-memory mode where the

input to the Sample and Hold circuit is used directly to tune and phase-lock the YO. This occurs:

(a) When the instrument is in the CW/MANUAL mode or in the Swept mode for YO sweep widths less than 5 MHz. This means that the YO is phase-locked during the entire sweep for sweep widths less than 5 MHz.

(b) Just prior to the sweep in the Swept mode for sweep widths greater than 5 MHz. This tunes and phase-locks the YO at the beginning of each sweep.

- Hold Mode - This is used for sweep widths of greater than 5 MHz. The YO is allowed to achieve phase-lock at the beginning of each sweep. Afterwards the Hold mode is enabled which causes the YO TUNE voltage to be held constant (using C24) while the YO is swept. This sequence is repeated at the beginning of each YO sweep.

The mode of operation of U3 is selected by the control signal LLEY (Low=Lock Enabled, YO) from the Logic Inverter/Translator, Block L. When this signal is a TTL LOW, the sample mode is enabled. When LLEY is a TTL HIGH, the hold mode is enabled.

The sample and hold IC, U3, was chosen for its low droop rate, which translates directly into improved YO sweep accuracy. R52 is used to allow the IC to operate with the large 2.0 uF hold capacitor, C24. CR7 and CR8 are used to bypass R52 during large signal operation (lock acquisition). An on-chip current-booster-charging circuit is also activated at this time. C35 is a compensation capacitor required for stable operation during large signal operation, and it also provides part of the hold circuitry.

FM Coil Driver I

The FM Coil Driver provides the tune signal for the YO FM Coil. It consists of two parts:

- 100 Hz High Pass Filter. This filter allows only the high frequency portion (greater than 100 Hz) of the error voltage signal to be applied to the YO FM Coil. (The YO Tune circuitry on the A55 YO Driver board has a 100 Hz Low Pass Filter applying only the low frequency portion of the error signal to the Main Coil.) There is also a ground transformation (provided by C26, R33, and R34) from Reference ground to FM GND.

- Output Amplifier. This circuit amplifies and filters the high frequency portion of the error signal to provide the drive

current (through R36) to the YO FM Coil. A Phase-Lag Filter is incorporated in the feedback of the amplifier which completes the YO Loop frequency response and improves the overall noise performance of the YO Loop. The output voltage signal is clamped (by VR4 and VR5) to a maximum of +3.8V to prevent the op-amp from becoming saturated during phase-lock.

The resistor-capacitor combination of R44-C28 and R43-C29 are used to provide additional filtering of the power supply inputs to A49U1.

Unlocked Detectors J

The output of integrator U7 in Loop Integrators (Block **F**) is a voltage representing the amount of frequency or phase error between the YO actual output and what it is supposed to be based upon the M/N and 20-30 frequencies. This output voltage is divided by 12 and presented to the comparators of the Unlock Detector.

Comparator U2B compares the output to -0.51V which is equivalent to approximately -6.1V at the output of integrator U7. Comparator U2A compares the output to +0.51V which is equivalent to approximately +6.1V at the output of integrator U7.

The outputs of these two comparators are wire OR'ed together. When the input to the Unlock Detector circuit exceeds approximately +6.1V, one of the comparators will pull up to +20V which will pull HULY up to 4.64V (where it is clamped by zener diode VR3). This High Unlock (HULY) signal is routed (via the A50 Loop Interconnect board) to the A59 Digital Interface board where the processor is able to detect this error condition. HULY is also routed through A50R6, and U1B and U1C (darlington open collector inverters) on the A50 YO Loop Interconnect board, where it causes a green LED (A50 DS1) to light whenever the YO Loop is LOCKED.

When the output of the Loop Integrators (Block **F**) is within approximately 6.1V, both comparator outputs will pull down to -10V and will thus reverse bias the two diodes CR3 and CR4. The HULY signal will then be pulled LOW by R29, being limited to -0.6V by the (forward biased) zener diode VR3.

Power Supplies K

This circuitry filters the supplies used on this board. The -5.2VFA supply routed to the analog circuitry is separately filtered from the -5.2VFB supply for the digital circuitry to prevent crosstalk. The chassis ground is isolated from the Reference ground through R38. FM ground is connected to Reference

ground through R37.

Transistor Q1 and surrounding circuitry form a capacitance multiplier circuit used to provide a filtered +15V supply, TP1, for the Differential Amplifier, Block **E**. The output voltage is determined by the voltage divider of R49 and R50 less the 0.6V base-emitter voltage drop. The circuit also provides a one-pole lowpass filter with Fc = 5.2 Hz (determined by the parallel combination of R49, R50, and C14). This circuit also provides a ground transformation from the chassis ground to the reference ground.

Logic Inverter/Translator L

The Logic Inverter/Translator inverts the HLEY (High=Lock Enable, YO) signal from the A59 Digital Interface assembly through the A50 YO Loop Interconnect assembly. The circuit has two outputs:

* LLEY (Low=Lock Enable, YO) is a TTL signal used to control the Sample and Hold, Block **H**. (LOW = sample; HIGH = hold.)

* YO LOOP DISABLE is an ECL logic signal that is used to disable the YO loop when in the hold mode (during sweeps). It does this by pulling HIGH the second input of IF Limiter U8A, Block **B**, causing U8B's output to remain LOW. This disables the Sampler IF input to the Phase/Frequency Detector, Block **D**, and causes the output of loop integrator U5 to rail to its +6.9V limit. This prevents the YO phase detector from responding to the sweeping YO signal which would produce noise. This noise, present at the input of U3, could feed through to cause low-level disturbances of the YO TUNE signal.

C32 is present to delay the YO Loop Disable signal to assure that the sample and hold circuit is activated before the loop is disabled. The circuit is designed so that the discharge rate of C32 (through Q2) is several times faster than the charge rate (through R46). The result is that, although the disable signal is delayed, the loop is quickly enabled so that the YO lock time is not affected.

A49 YO LOOP PHASE DETECTOR TROUBLESHOOTING

YO Unlock

A YO UNLOCK error condition can be caused by a number of different failure mechanisms in any of a number of assemblies. When the YO UNLOCK indicator is on, the YO Loop Troubleshooting Procedure should first be used to determine which assembly is at fault. It will also help locate which block of the assembly is malfunctioning. The following procedure should be used only when reasonably certain that the problem is with the A49 YO Loop Phase Detector.

NOTE

When troubleshooting the A49 YO Loop Phase Detector, the YO Loop should be placed in its service position and the cover removed. The YO TUNE and FM COIL cables must be connected and all assemblies involved with the YO Loop kept in place so that the loop remains closed.

The YO UNLOCK is signaled by the HULY (High = UnLocked Yo) line going HIGH. This is accompanied by the green LED on the A50 YO Loop Interconnect board turning off. This condition is indicated by the Unlocked Detector whenever the YO TUNE voltage at A49J2 goes outside the ±6.0 V range. Using a 3-way connector at A49J2 to keep the YO Loop closed, measure YO TUNE. If it is not outside the ±6.0 V range, then troubleshoot the Unlocked Detector, Block J.

Limiters

To verify the operation of the Limiters, Blocks B and C, use a 100 MHz oscilloscope with a 10:1 probe to measure the input at A49J3 and A49J4 and the outputs of the limiters at TP4 and TP5. The signals at TP4 and TP5 should be square waves at ECL voltage levels (-5.0 to -0.7 V).

For a signal to exist at TP5, HLEY must be HIGH and the Logic Inverter/Translator circuitry must be functioning properly. This provides an ECL LOW (-2V to -5V) to pin 5 of U8A which enables the second IF Limiter.

Phase/Frequency Detector

To verify the operation of the Phase/Frequency Detector, make measurements with an oscilloscope at the two inputs, TP4 and TP5 (see previous section), and the two outputs, TP2 and TP3. The

correct output waveforms are described in the circuit theory section for the Phase Frequency Detector, Block D. Use a 10:1 test probe with a short ground clip. If the grounding is not good, there will be ringing on the signal edges. Also refer to the Open Loop Test, below.

Differential Amplifier and Loop Integrators

The bias voltages for Q3 will change with loop conditions. The three conditions of interest are (1) Loop Locked, (2) Sampler IF frequency less than the 20-30 frequency ("lag", YO TUNE $\leq$ -6.0 V), and (3) Sampler IF frequency greater than the 20-30 frequency ("lead", YO TUNE $\geq$ +6.0 V). The approximate bias voltages for these three conditions are given in Table 8D-2. Also refer to the Open Loop Test, below.

Table 8D-2. Bias Voltages on A49Q3 Under Different Loop Conditions

Loop Condition	Q3A			Q3B		
	Emitter (pin 4)	Collector (pin 1)	Base (pin 2)	Emitter (pin 3)	Collector (pin 6)	Base (pin 5)
(1) LOCKED	−1.5 V	+15.0 V	−0.9 V	−1.5 V	+6.7 V	−0.9 V
(2) LAG	−1.5 V	+15.0 V	−1.8 V	−2.1 V	+3.7 V	−0.8 V
(3) LEAD	−2.1 V	+15.0 V	−0.8 V	−1.5 V	+9.9 V	−1.8 V

Open Loop Test

The following is an open-loop test that can be used to troubleshoot the A49 YO Loop Phase Detector. Set the instrument to CW mode. Disconnect the cables at A49J1 and A49J2, and measure the YO TUNE voltage at A49J2. The voltage will be either -6.9 V, corresponding to case Number 2 above (lag), or else +6.9 V corresponding to case Number 3 (lead). The bias voltages of Q3 should be close to those listed in Table 8D-2. Switch the Sampler IF and the 20-30 MHz input cables (A49J3 and A49J4). This should reverse the polarity of YO TUNE. The corresponding bias voltages for Q3 can now be verified. If the bias voltages of Q3 are correct for both cases but the polarity of YO TUNE does not reverse, then troubleshoot the Loop Integrators, Block F, and the Sample and Hold, Block H.

Sample and Hold

With HLEY (High Lock Enable Yig Oscillator) HIGH, and LLEY LOW (CW or MANUAL mode), the output of the Sample-and-Hold, Block H, should track the input. Verify that HLEY is HIGH and LLEY is LOW, then measure the input and output of U3; they should be identical.

FM Coil Driver

If the FM Coil Driver, Block I, is malfunctioning, the YO Loop will acquire phase-lock, but the residual FM on the YO Output will be far greater than the typical specification of 60 Hz. The dc output of the op-amp should be 0 V.

Logic Inverter/Translator

To test the Logic Inverter/Translator, TP3 (HLEY) on the A50 YO Loop Interconnect assembly can be used to force a logic condition to occur. Connect HLEY to +5V and then to ground, verify that the outputs are within the given limits. LLEY can be measured at U3 pin 14; YO Loop Disable can be measured at U8 pin 5.

HLEY	LLEY	YO LOOP DISABLE
+5V	2.4 to 5.0V	-0.5 to -1.0V
0V	0.0 to 0.5V	-2.0 to -5.0V

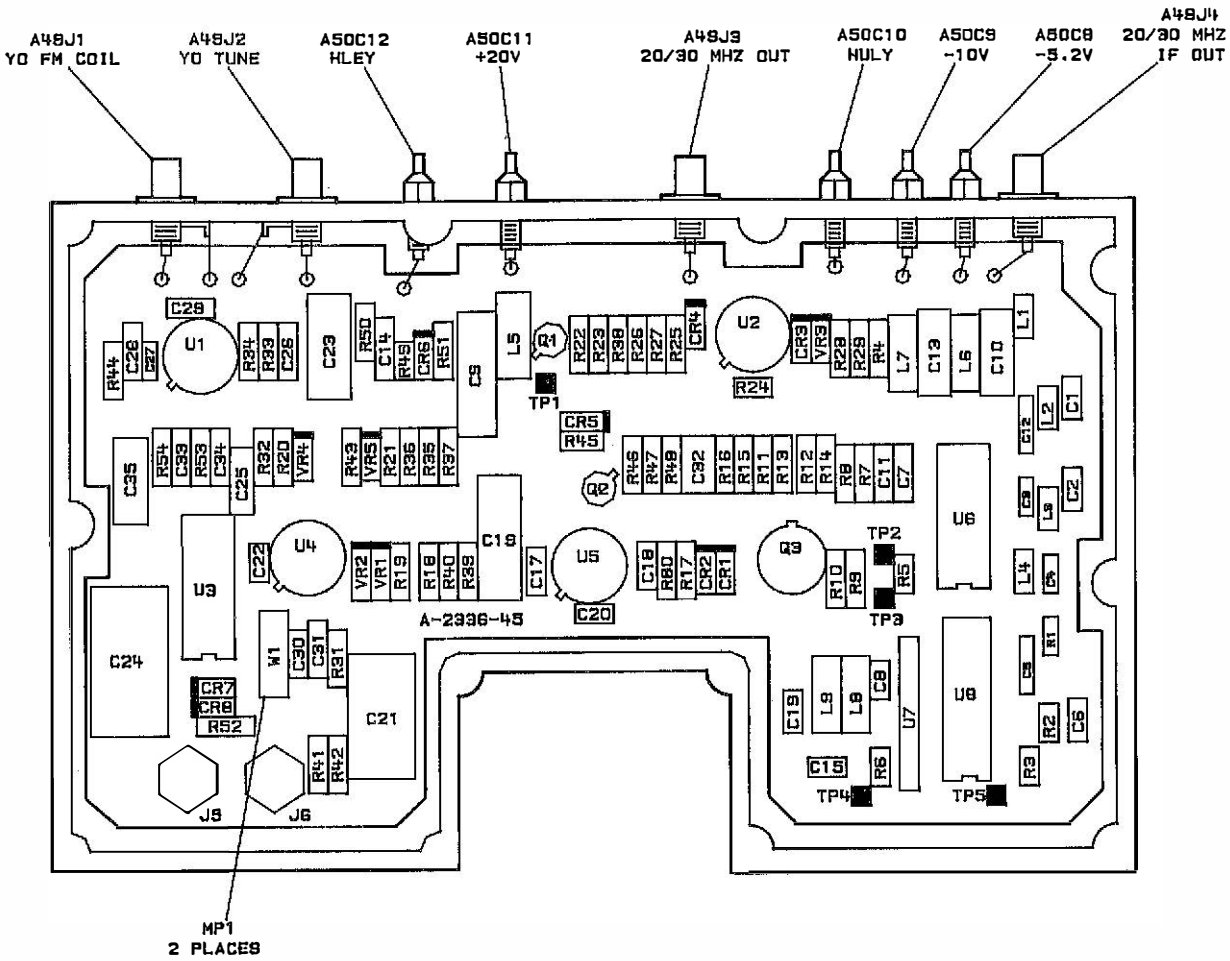


Figure 8D-9. A49 YO Loop Phase Detector, Component Location Diagram

A50 YO LOOP INTERCONNECT BOARD

A50 YO LOOP INTERCONNECT BOARD CIRCUIT DESCRIPTION

The A50 YO Loop Interconnect board is used to distribute power and signals to the A48 YO Sampler Assembly, the A49 YO Phase Detector, the A45 Directional Coupler, and the A44A1 YO Bias board. It also contains the following signals, and each is provided with a testpoint.

TP3 HFIL HIGH = YO CW Filter is switched IN
TP4 HLEY HIGH = Lock is Enabled, YO
TP6 HULY HIGH = UnLocked YO

The test points serve two purposes. Each test point can be used to monitor the state of the digital signal. (The level will be somewhat less than the actual signal level due to the resistors on each side of the test points.) The test point can also be used to force a logic condition to occur by tying it to +5V or ground. These features are useful for troubleshooting and to verify circuit operation.

Also provided on the YO Loop Interconnect board are test points for each supply voltage and for the YO Coil voltage.

The A50 YO Loop Interconnect board also isolates and separately filters supplies going to different portions of the YO Loop Assembly.

8-331

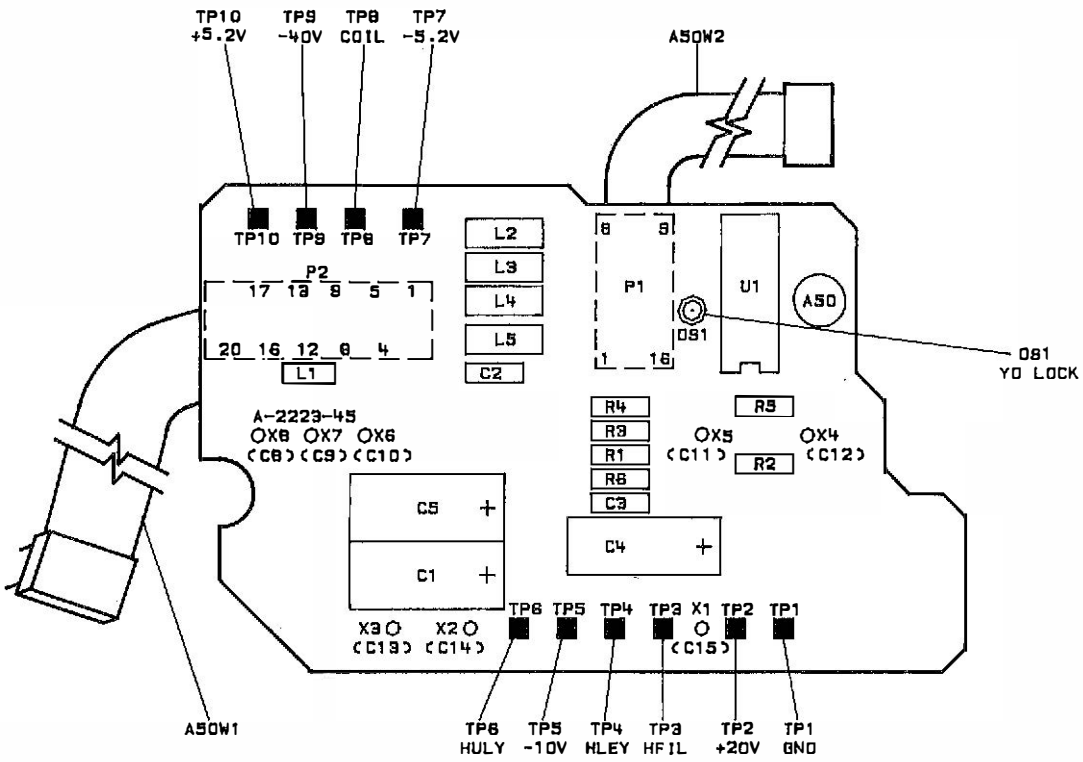
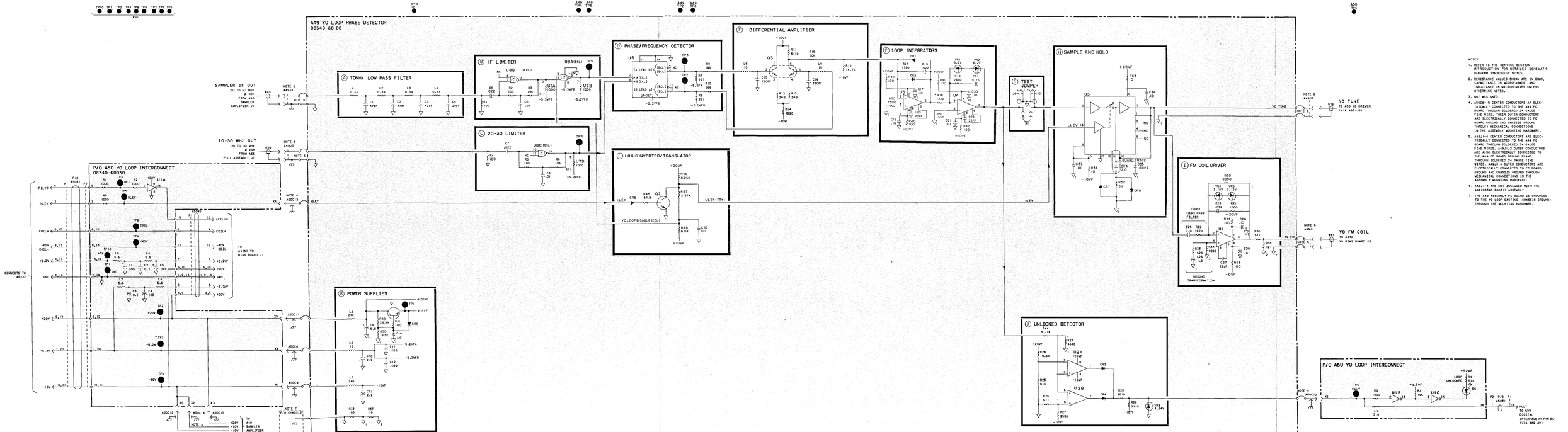


Figure 8D-10. A50 YO Loop Interconnect, Component Location Diagram

A62J2 TO A50W1P2 PIN I/O

Pin	Mnemonic	A50W1P2	Levels
1 2	−5.2V GND	PIN 1 PIN 2	−5.2V 0V
3 4	HLEY +5.2V	PIN 3 PIN 4	TTL (HIGH TRUE) +5.2V
5 6	HFILYO YO COIL +	PIN 5 PIN 6	TTL (HIGH TRUE) −40V TO −20V
7 8	YO COIL −/−40V	PIN 8	−40V
9 10	+20V −10V	PIN 9 PIN 10	+20V −10V
11 12	−10V +20V	PIN 11 PIN 12	−10V +20V
13 14	YO COIL −/−40V	PIN 13	−40V
15 16	YO COIL + HULY	PIN 15 PIN 16	−40V TO −20V TTL (HIGH TRUE)
17 18	+5.2V	PIN 17	+5.2V
19 20	GND −5.2V	PIN 19 PIN 20	0V −5.2V

Note: Refer to A50 YO Loop Interconnect Schematic Diagram and A62 Motherboard Wiring List for signal source and destination information.



NOTES:

1. REFER TO THE SERVICE SECTION INTRODUCTION FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES SHOWN ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENERIES UNLESS OTHERWISE NOTED.
3. NOT ASSIGNED.
4. A50C6-15 CENTER CONDUCTORS ARE ELECTRICALLY CONNECTED TO THE A49 PC BOARD THROUGH SOLDERED 24 GAUGE FINE WIRE; THEIR OUTER CONDUCTORS ARE ELECTRICALLY CONNECTED TO PC BOARD GROUND AND CHASSIS GROUND THROUGH MECHANICAL CONNECTIONS IN THE ASSEMBLY MOUNTING HARDWARE.
5. A49J1-4 CENTER CONDUCTORS ARE ELECTRICALLY CONNECTED TO THE A49 PC BOARD THROUGH SOLDERED 24 GAUGE FINE WIRES. A49J1-3 OUTER CONDUCTORS ARE ALSO ELECTRICALLY CONNECTED TO THE A49 PC BOARD GROUND PLANE THROUGH SOLDERED 24 GAUGE FINE WIRES. A49J1-3 OUTER CONDUCTORS ARE ELECTRICALLY CONNECTED TO PC BOARD GROUND AND CHASSIS GROUND THROUGH MECHANICAL CONNECTIONS IN THE ASSEMBLY MOUNTING HARDWARE.
6. A49J1-4 ARE NOT INCLUDED WITH THE A49 (08340-60011) ASSEMBLY.
7. THE A49 ASSEMBLY PC BOARD IS GROUNDED TO THE YO LOOP CASTING (CHASSIS GROUND) THROUGH THE MOUNTING HARDWARE.

Figure 8D-11. A49 YO Loop Phase Detector and A50 YO Loop Interconnect, Schematic Diagram

A54 YO PRETUNE/DELAY COMPENSATION

INTRODUCTION

The A54 YO Pretune/Delay Compensation board performs three major functions:

- It provides a dc voltage, Pretune, to the A55 YO DRIVER which is proportional to the frequency to which the YO is being phase-locked. The YO sensitivity of this line is -2.5 V/GHz. Pretune is also used by the A28 SYTM Driver to tune the SYTM.

- It generates the kick pulses which are necessary at a YO retrace to preset the magnetic domains of the YO to eliminate the affects of magnetic hysteresis. These pulses are of constant amplitude, corresponding to about 2.5 GHz, and are of varying width. The width is a function of the YO start frequency and sweep width of the previous sweep as well as the YO start frequency of the next sweep. These pulses are subtracted from the phase-lock Pretune voltage and have the affect of temporarily tuning the YO 2.5 GHz below the next lock frequency.

- It provides a voltage, VCOMP, to the A55 YO Driver which is used to compensate for the YO frequency delay.

A54 YO PRETUNE/DELAY COMPENSATION CIRCUIT DESCRIPTION

Pretune Register A

U11 and U13 latch data bits 1-12 from the 16 bit instrument data bus to set the Pretune voltage. The strobe that activates the latch is WPDAC (Write Pretune DAC). This strobe is channel 3, sub-channel 2 from the processor (3,R2:). U10 AND U12 contain pull-up resistors to back bias the output stages of the latches when the outputs are HIGH so that bus noise cannot come through to the DAC.

Pretune DAC B

U6 is a 12 bit bipolar DAC. It takes the 10 volt reference voltage and the latched data bits to give a dc voltage at TP6, VDAC, given by the formula:

$$VDAC = 2.10V/(f_{YO} - 2.3)GHz$$

The voltage corresponding to 2.3 GHz is derived from the reference voltage and added at the Summing Amplifier (Block C). The sensitivity of this block is +2.100 Volts/GHz.

The formula for calculating the digitized number that is present at the input of U6 at any given frequency is:

[Lock frequency (GHz) - 2.3 (GHz)] ⊠ 870.

Note that the latches pick off data bits 1-12, NOT 0-11. This means that the number sent by the processor and the number that shows up at the input of the DAC differ by a factor of 2. The formula for the number sent by the processor is:

[Lock frequency (GHz) - 2.3 (GHz)] ⊠ 1740.

R14 takes out the tolerance of the summing resistors R19 and R20 as well as the gain tolerance of U6 itself. CR4 is a protection diode to insure that pin 9 of U6 does not go much below pin 12. U2 is a high performance OP-AMP chosen for its low offset voltage, good temperature characteristics, and low noise. C15 provides stability compensation for the DAC.

Summing Amplifier C

The Summing Amplifier combines four signals to give the final Pretune voltage. These signals are:

- A voltage corresponding to 2.3 GHz (R22-24)
- The DAC voltage which is proportional to lock frequency minus 2.3 GHz (R19, R20)
- The sweep ramp (R25, R26)
- The retrace kick pulse (R46)

The combined signal is called PRETUNE, TP3, and has a YO sensitivity of -2.5 V/GHz. R22 adjusts for the tolerance of R21, R22, R23, the +10 volt reference, and the offset voltage of U4.

A further note about PRETUNE: The 2.3 GHz offset is used so that the greatest resolution can be achieved from the DAC. 2.3 GHz is the lowest frequency that the YO can be tuned to and corresponds to a DAC number of zero. The highest frequency that the YO can be tuned to is 7.0 GHz and this corresponds to a DAC number of 4089. Note that this is not all digital ones at the DAC input but a slightly smaller number. This was done to simplify the calculations that the processor has to do. Pretune is also routed to the A28 SYTM Driver where it is scaled and used to tune the SYTM.

Voltage Reference D

The voltage reference for the whole Pretune system is derived from VR1, a low noise, 1%, 5 ppm reference zener diode. The circuit provides a constant bias current of 7.5 mA through the diode. R10 and C11 give extra filtering of diode noise.

Note that C11 is a polycarbonate capacitor which has low leakage, noise, and current, and has good temperature stability. The current from the op-amp is not sufficient to cover the worst case needs of the board, so R49 provides the remainder of the current.

Sweep Disable Switch E

FET Q3 is a switch that grounds the junction of R25 and R26 (Block **C**) when LVSX (Low Voltage Sweep disable) is LOW. This prevents noise from the sweep generator from being added to the PRETUNE voltage when the instrument is in the CW, MANUAL, or narrow sweep modes. Narrow sweeps are sweep widths $\leq$ 500 kHz.

LVSX is HIGH any time that the 8340A is in the sweep mode and the sweep width is >500 kHz. Therefore, any slight dc offset that might be at the output of the sweep generator when it is reset (and supposed to be at zero) is added to the PRETUNE voltage while the instrument is acquiring phase-lock. This offset will not effect the sweep accuracy, however, as long as it is not great enough to keep the YO from acquiring phase-lock.

YO Delay Compensation F

The frequency lag or delay in the YO during a sweep due to eddy currents in the magnetic poles is described by the equation:

Delay(Freq) = [A+(B*F)]*dF/dt

where:

Delay(freq) = Frequency lag or delay

F = (measurement frequency) - (start frequency)

dF/dt = sweep rate

The YO DELAY COMPENSATION circuit generates a voltage, VCOMP (TP4), proportional to the delay shown above. This voltage is sent to the A55 YO DRIVER board where it is used to speed up the sweep to make the frequency more closely follow the PRETUNE voltage and thus compensate for the YO frequency delay.

To generate this voltage, the circuit sums a dc voltage (COFF adjustment) and the VSWP voltage ramp (CGN adjustment) to

generate the (A + B*F) term. (This is done through resistors R30 through R34.) The resulting voltage is used as the analog input to an 8 bit DAC whose digital input, provided by the processor, is related to the sweep rate, dF/dt. The DAC then performs the multiplication, and thus the voltage, called VCOMP, is of the desired form. The strobe for this DAC is 5,R3: (Write Compensation DAC). C31 is used for stability compensation of the DAC.

In the configuration used, U16 gives a high impedance voltage output at pin 21. U14A buffers this voltage and provides the necessary low output impedance. R35 was chosen to match the 5K Ohm internal DAC impedance to ensure unity gain for U14A. CR6 clamps the maximum DAC output at ground.

YO Retrace Kick Pulse Generator G

Through the use of an 8 bit DAC, U15, this circuit generates a programmable width pulse. This LOW-going pulse is applied to the gate of Q1 (Block **C**) which switches in an additional current to offset the PRETUNE voltage. This offset is 6.2 volts in the positive direction, which has the effect of tuning the YO lower in frequency (about 2.5 GHz).

The instrument processor initiates a kick pulse by first writing to the pulse width DAC address, 5,R1: (WYOKW, Write YO Kick Width), a number that corresponds to the desired pulse width. This write loads U15 and resets the pulse circuit through U9. At the appropriate time, the processor sends a trigger 3,R0: (TYOKP, Trigger YO Kick Pulse), which starts the pulse. The circuit then terminates the pulse after the programmed length of time has elapsed.

The write to the pulse width DAC (WYOKW, Write YO Kick Width) initializes the pulse width circuitry as follows. U9 is set. (Note: U9 is an LS74, and the set and reset inputs function as a standard flip-flop.) The positive edge triggered clock input clocks the D input to the Q output or in this case effectively sets the flip-flop. The Q output of U9 (pin 9) through U7B turns off switch Q1 (Block **C**) which turns off the kick pulse. The Q_O output of U9, pin 8, turns on switch Q4, which zeros the integrator formed by U14B and C29. The write (WYOKW) also programs the DAC, U15, to a voltage between 0 and +10 volts which corresponds to the desired pulse width.

Since the inverting input of U14B is a virtual ground and the reference voltage from U15, pins 13 & 14, is a constant +5 volts, there is a constant current of about 64 microamps into the integrator. Because the capacitor is shorted by Q4 at this point, the output of U14B is zero volts.

When the trigger pulse (TYOKP, Trigger YO Kick Pulse) is received from the processor, U9 is reset and Q1 is turned on through U7B. When U9 is reset, pin 8 goes HIGH turning Q4 off through U7D. The constant current of 64 microamps into the integrator now gives rise to a negative going ramp at the output of U14B with a constant slope of about -291 volts/second. When this ramp reaches a value equal in magnitude, but opposite in polarity, to the voltage at the output of the DAC (U15), then comparator U8 fires and clocks U9. This effectively sets U9, turning off the kick pulse and zeroing the integrator.

The only adjustment in this circuit is R36, that varies the current to the integrator to take out tolerances in the integrating capacitor, C29, and current setting resistor, R37.

The number written to the pulse width DAC address is related to the desired pulse width by the formula:

Pulse width (msec) = [(Number) / 512] * 34 msec

Since the DAC input itself is bits 1-8 rather than 0-7, the number that appears at the input of U15 is the number calculated above, divided by two.

Power Supplies H

L1-L5 and C1-C5 form standard low-pass power supply filters. The inductor type was chosen to have a relatively high series resistance, while the capacitor was chosen to have a low series resistance. This results in a Q of about 2 for the filter formed by the LC circuit.

U1 and U3 are 3-terminal 5 volt and 15 volt regulators. CR1 and CR2 are protection diodes. If the input to either regulator is somehow shorted to ground the discharge currents of C9, C35 and any onboard capacitance is shunted through these diodes rather than through the regulators. Reverse current through these regulators results in catastophic failures.

Q2 is a simple voltage follower. C7, R3 and R4 provide noise filtering to the base of the transistor.

R2 provides a back-up connection between reference and chassis grounds so that if the motherboard connection between the grounds is broken for some reason, this board will continue to operate, although not necessarily within specifications.

A54 YO PRETUNE/DELAY COMPENSATION TROUBLESHOOTING

In all modes, the sensitivity of the PRETUNE output, TP3, is -2.5 volts/GHz. This is the place to start in troubleshooting the board. In CW mode, run the frequency from 2.3 GHz to 6.99 GHz and see if the correct voltage is present on the PRETUNE test point. Note, if you set the CW frequency to 7.0 GHz, the PRETUNE will be -8.75 volts, corresponding to 3.5 GHz. This is because the instrument switches to the second harmonic band at this point.

If the PRETUNE voltage (TP3) is not correct, then check all inputs to the summing amplifier. VDAC (TP6) should have a sensitivity of 2.10 volts/[(f_{YO}-2.3)GHz] and VREF should be +10 volts, ± 10%. Also BLVSX (TP1) should be <+0.5 volts and LKICK should be +5 volts. If these last two lines are not correct, they will add unwanted voltages to PRETUNE. In particular, if LKICK is LOW, <+0.5 volts, it will add +2.5 Volts error to the PRETUNE signal. If VDAC (TP5) is not at the correct voltage, check the digital inputs and the input from VREF. The formula for calculating what the VDAC and digital input should be is given in the theory section for Pretune DAC, Block **B**.

In the sweep mode, if the PRETUNE voltage does not ramp, check to see that VSWP, P1-26, is present. Then see that BLVSX, TP1, is HIGH, +15 volts, so that the sweep voltage is summed with the start frequency PRETUNE voltage.

If there is no retrace kick pulse, check LKICK to see that it goes LOW, <+0.5 volts, during the period of the kick. If LKICK is not working correctly, then the YO Retrace Kick Pulse Generator, Block **G**, must be checked. The operation of U15 can be verified by writing to its address, WYOKW 5,R1: (Refer to A60 Processor documentation). Writing zero to this address should result in zero volts at U15, pin 18. Writing 511 should result in +10 volts at U15 pin 18.

To test U16 (YO Delay Compensation, Block **F**), set the instrument to sweep from 2.3 GHz to 7.0 GHz with a 10 msec sweep time. VCOMP should then be a negative-going ramp with a step at the start as shown on the schematic. The voltage should go from approximately -0.5 to -2 volts. These voltages are very loose limits and depend upon how the COFF and CGN pots have been adjusted. Variations of +50% are to be expected. However, as the sweep time is increased to half a second, the step at the start of sweep should decrease smoothly to zero as should also the slope of the ramp.

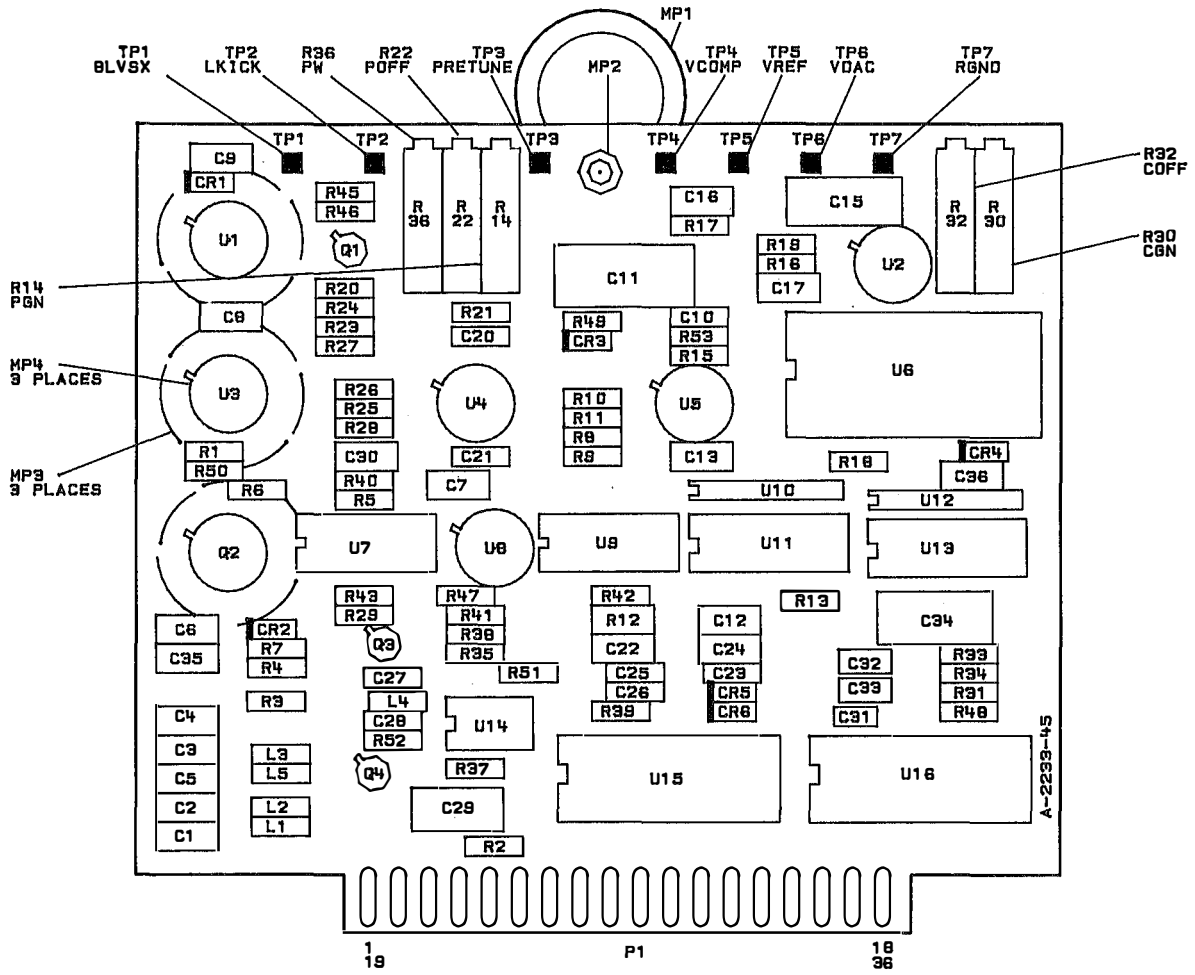


Figure 8D-12. A54 YO Pretune/Delay Compensation, Component Location Diagram

A54 YO Pretune DAC/Delay Compensation P1 Pin I/O

A54

Pin	Mnemonic	Levels	Source	Destination
1 19	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*H *H
2 20	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*H *H
3 21	−40V/−40V SENSE (−) YOKICK	−40V TTL (HIGH TRUE)	XA53P1-11, 30/XA53P1-23 G	*H/H *
4 22	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*H *H
5 23	GND GND	0V 0V	A62 STAR GNO A62 STAR GND	*H *H
6 24	WYOKW PRETUNE	TTL (LOW TRUE) −2.5V/GHZ, 0V = 2.3 GHZ	XA59P1-99 C	G *
7 25	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*H *H
8 26	−15V VSWP	−15V 0 TO 10V SWEEP	XA56P1-15, 30 XA58P1-97	*H *C F
9 27	LVSX VCOMP	TTL (LOW TRUE) −26 MHZ/VOLT	XA58P1-68 F	E XA55P1-9
10 28	DB1 WCDAC	TTL TTL (LOW TRUE)	XA60P1-76 XA59P1-30	*A G F
11 29	DB3 DB2	TTL TTL	XA60P1-77 XA60P1-21	*A G *A G
12 30	DB5 DB4	TTL TTL	XA60P1-78 XA60P1-22	*A G *A G
13 31	DB7 DB6	TTL TTL	XA60P1-79 XA60P1-23	*A G *A G
14 32	DB9 DB8	TTL TTL	* *	*A F *A F G
15 33	DB11 DB10	TTL TTL	* *	*A F *A F
16 34	DB13 DB12	TTL TTL	XA60P1-82 *	*F *A F
17 35	DB15 DB14	TTL TTL	XA60P1-83 XA60P1-27	*F *F
18 36	TYOKP WPDAC	TTL (LOW TRUE) TTL (LOW TRUE)	XA59P1-100 XA59P1-68	*G A

A circled letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete listing of signal destinations.

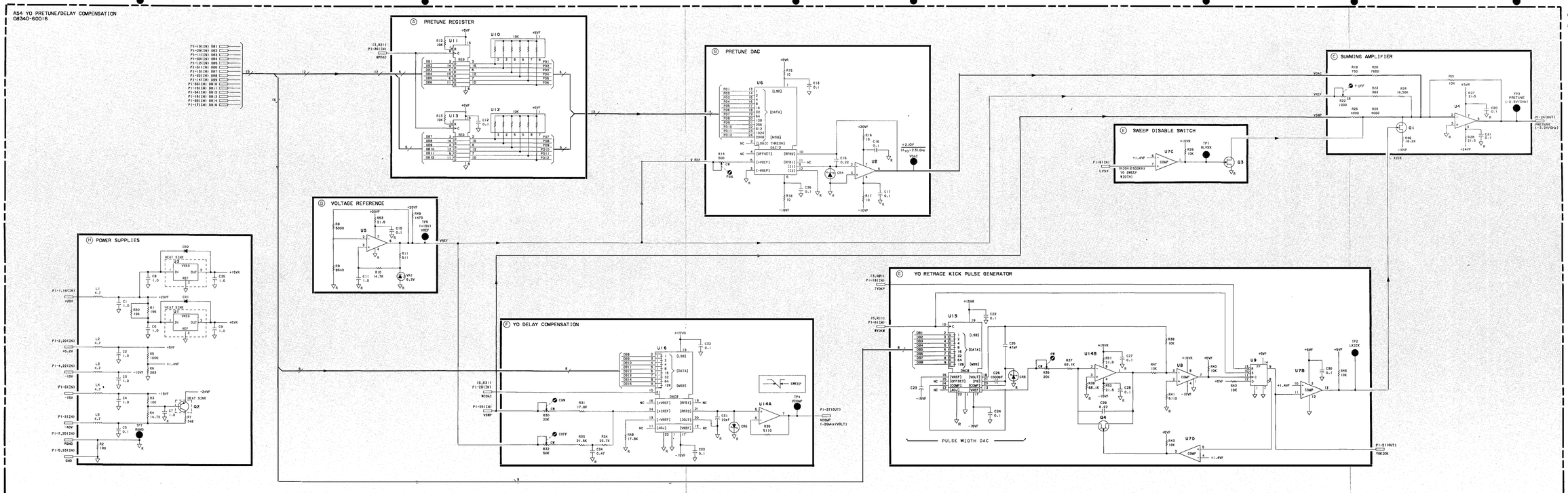


Figure 8D-13. A54 YO Pretune/Delay Compensation, Schematic Diagram

A55 YO DRIVER ASSEMBLY

INTRODUCTION

The YO Driver board performs several functions in the 8340A.

- It acts as a voltage to current converter to transform the Pretune voltage (sensitivity = -2.5 Volts/GHz) to YO MAIN COIL current (sensitivity is approximately 24 ma/GHz).
- It provides the summing point for the low frequency portion (less than 100 Hz) of the YO phase-locked loop error voltage (YO TUNE).
- It provides the summing point for the YO Delay Compensation voltage (VCOMP).
- It provides the summing point for the YO coil offset current.

Figure 8D-14 shows a simplified block diagram of the YO Driver circuit. Notice that the sense resistor and part of the Compound PNP Transistor circuit (A47Q1) are physically located on the A47 Sense Resistor Assembly.

The Discrete Op-Amp (Block **A**) is connected with the Compound PNP Transistor (Voltage-to-Current Converter, Block **B**) to form a current source which sets the YO coil current and hence the YO frequency. The negative feedback for the Discrete OP-Amp is taken from the sense resistor (A47R6); therefore the voltage present at the inverting input of the Discrete OP-Amp will also be present at the sense resistor. Since the other end of the sense resistor is connected to ground, this voltage defines the current through the sense resistor and thus through the YO coil. The voltage at the non-inverting input of the Discrete OP-Amp (TP5) is slightly lower than the PRETUNE voltage due to the GAIN adjustment potentiometer, which acts as a voltage divider. The coil current is related to the voltage at TP5, the IN test point, by the following equation:

$$I(coil) = V(IN)/R(sense), \text{ with } R(sense) = 97.5 \text{ Ohms}$$

The feedback point to the Discrete OP-Amp, TP4, also forms a current summing node. Any current that is injected at this point from the Main Summing Amplifier, Block **E**, must flow through the YO coil and not the sense resistor. This is because the feedback loop maintains a given voltage at the feedback point which in turn maintains a given current through the sense resistor. This arrangement provides a way to vary the YO frequency without

upsetting the feedback loop.

Several signals are summed at the feedback point. The delay compensation voltage, VCOMP, is applied through Q4 in Main Summing Amplifier, Block **F**, and a 411 kHz low pass filter formed by C8 and R55. The function of this filter is to round the leading edge of VCOMP in order to properly match the delay characteristics at the start of the sweep. The YO phase-locked loop error voltage (YO TUNE) is summed through the network of R51, R52, R32 and C14. This network is a 100 Hz low pass filter to pass the desired low frequency component of the error voltage. The YO coil OFFSET current (R47 in YO Error/Offset Summing Amp, Block **E**) is summed through the same path as the YO TUNE voltage.

The YO coil OFFSET current is necessary because the YO coil current verses YO frequency characteristic does not go through the origin. That is to say, if you extrapolate the characteristic down to zero current, you do not get zero frequency. This offsetting could have been handled by the processor by varying the number sent to the Pretune DAC except for the fact that the SYTM also uses that voltage and has its own independent offset.

A55 YO DRIVER ASSEMBLY CIRCUIT DESCRIPTION

Discrete Op-Amp A

The Discrete OP-Amp is arranged in a standard configuration. Q3 provides the differential input with TP4 the - input and TP5 the + input. The Q2 circuitry forms a current source for biasing the input stage. C1 is for noise filtering; CR2 and CR3 provide temperature stablization. CR1 limits the differential input voltage to the OP-Amp.

Q1, Q5, R8 and R9 form a current mirror to provide maximum gain from the differential input to the single ended output. Q6 is the output stage of the Discrete OP-Amp. R10 and C2 are for loop compensation.

The gain of the YO Driver is set by the adjustable voltage divider formed by R1 through R4. This adjustment is made at the high end of the YO frequency range (i.e., 6.99 GHz). The GAIN adjustment is interactive with the OFFSET adjustment, R47 in YO Error/Offset Summing Amplifier (Block **E**), which is made at the low end of the frequency range (2.3 GHz). See the adjustment section.

R13, R20, and C3 form a noise filter used in the CW and MANUAL modes. In YO sweeps, however, to avoid unwanted delay in the response of YO Driver, the filter can be switched out by the Filter Switch (Block **D**). This filter also severely limits the

slew rate of the Discrete Op-Amp so Q7 and Q9 serve as speed up transistors by shunting resistor R13 when the Op-Amp is slewing and when the voltage across the resistor is sufficient to turn on one of the other of the transistors. Q8 is a current limiter stage.

Voltage-To-Current Converter B

Transistors Q10 and Q12 are connected as a complementary darlington pair. This circuit, together with A47Q1 on the A47 Sense Resistor Assembly, function as a compound PNP Transistor with its emitter connected to the sense resistor, its base connected to the output of the Discrete Op-Amp, and its collector connected to the YO Main Coil. See Figure 8D-14. The sense resistor, A46R6, and A47Q1 are mounted externally to the board for heat sinking and so the reference grounds of the YO and SYTM can be connected to chassis ground at the same point without any intervening PC edge connections. This configuration results in improved 60 Hz performance as well as better YO/SYTM tracking.

CR6, CR7, CR8 and VR1 protect the darlington transistor against the inductive voltage spikes generated by the YO coil whenever a step change in current is desired. C4, C25 and R23 stablize the Compound PNP Transistor. Oscillation of this stage is aggravated by the inductance of the leads connecting the on-board and off-board components. R24 provides for a slight bias current through Q12 and defines the impedance seen by the base of A47Q1. C26 bypasses the base-emitter junction of Q10 and improves the radiated susceptibility performance of the instrument.

VCOMP Switch Logic C

This circuitry determines when the delay compensation voltage (VCOMP) is applied to the Main Summing Amplifier (Block **F**). When both HSP (High SweeP), and HCEN (High Comp ENable) inputs are HIGH, the output at U5B is LOW, turning on Q4 in the Main Summing Amplifier (Block **F**). This allows the VCOMP signal to be summed with the YO TUNE input. When either HSP or HCEN are LOW, Q4 is turned off, removing the VCOMP signal. HCEN is a latched line that is HIGH whenever the sweep width is greater than 50 MHz. R40 is a pull-up resistor to ensure that the output of U5B goes high enough to turn off Q4.

Filter Switch D

In YO sweeps, switch Q11 is turned on by LYSP (Low Yo SweeP). This grounds R22 in Discrete Op-Amp (Block **A**) which sources current through R13 and R20, thus turning on Q9 and providing a straight through path in shunt with the one resistor, R13. This bypasses the filter and eliminates its associated delay.

YO Error/Offset Summing Amp E

The OFFSET voltage is derived from a 6.2 volt reference zener. R47 provides an adjustment for this voltage and R48 with C15 provide noise filtering. The YO phase-locked loop error voltage, YO TUNE, from the A49 YO Loop Phase Detector (A49J2) is summed with the offset voltage at U2.

Main Summing Amplifier F

The delay compensation voltage (VCOMP) from A54 YO Pretune/Delay Compensation board is added to the output of YO Error/Offset Summing Amp (Block **E**). Q4 switches VCOMP in and out. The resultant voltage (SUM, TP2) is injected through R29 as a current into the summing node of the Voltage-To-Current Converter (Block **B**).

Power Supplies G

The power supply filtering is the standard shunt capacitance, series resistance type. Series resistors were used rather than series inductors to provide a wide-band, low Q impedance for the shunt capacitors to work against.

A55 YO DRIVER ASSEMBLY ADJUSTMENTS

Before the YO Driver adjustments are made, the A54 YO Pretune/Delay Compensation assembly must first be adjusted. Once this is done, carry out the following procedure:

NOTE

GAIN Adjust R4, and OFFSET Adjust R47 are interactive. With the following procedure, however, the number of iterations can be minimized.

Open the YO phase-locked loop by removing Cable A49W1 from between A49J5 and A49J6 on the YO Loop Assembly. Connect a short circuit or a 50 Ohm load to connector A49J6.

Set the instrument to CW, 2.30 GHz. Measure the actual YO frequency and call it F_1. Now set the instrument to CW, 6.99 GHz. Again measure the YO frequency and call it F_2.

Without changing the state of the instrument, adjust the GAIN Adjust R4 in Discreet Op-Amp (Block **A**) so that the YO frequency in GHz is:

$$F_{YO}(GHz) = (4.6 * F_1)/(F_2-F_1) + 4.6$$

where:

F_1 and F_2 are the frequencies in GHz that were measured previously in the procedure.

Finally, set the instrument to CW at 2.3 GHz and adjust the OFFSET Adjust R47 so that the YO frequency is 2.3 GHz. (In setting the YO frequency, an accuracy of 1 MHz is sufficient).

As a final check, reconnect cable A49W1 between A49J5 and A49J6 and measure YO TUNE (A55TP3) in the CW mode over the frequency range of 2.30 to 6.99 GHz. The dc value should vary about 0 volts. The PRETUNE should set the YO within about 5 MHz of the desired frequency. The sensitivity of YO TUNE is about -3 MHz/volt. Therefore, YO TUNE should be < $\pm$2 Volts.

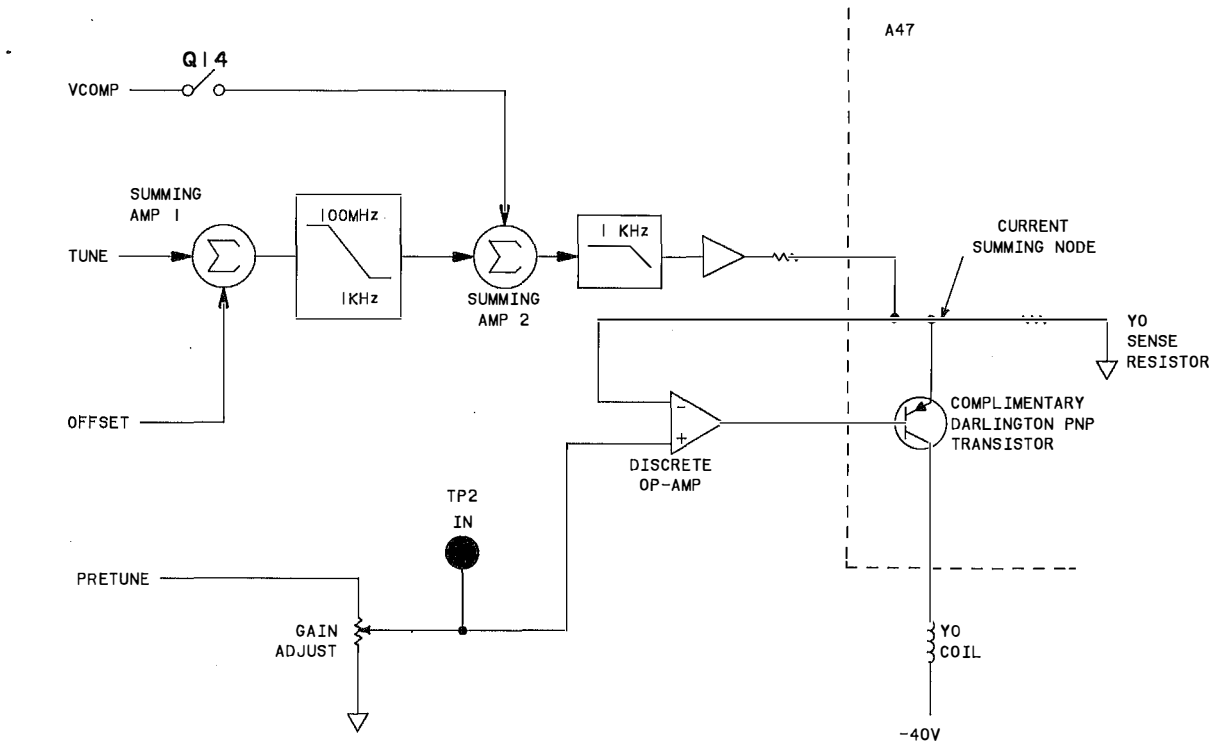


Figure 8D-14. A55 YO Driver Simplified Diagram

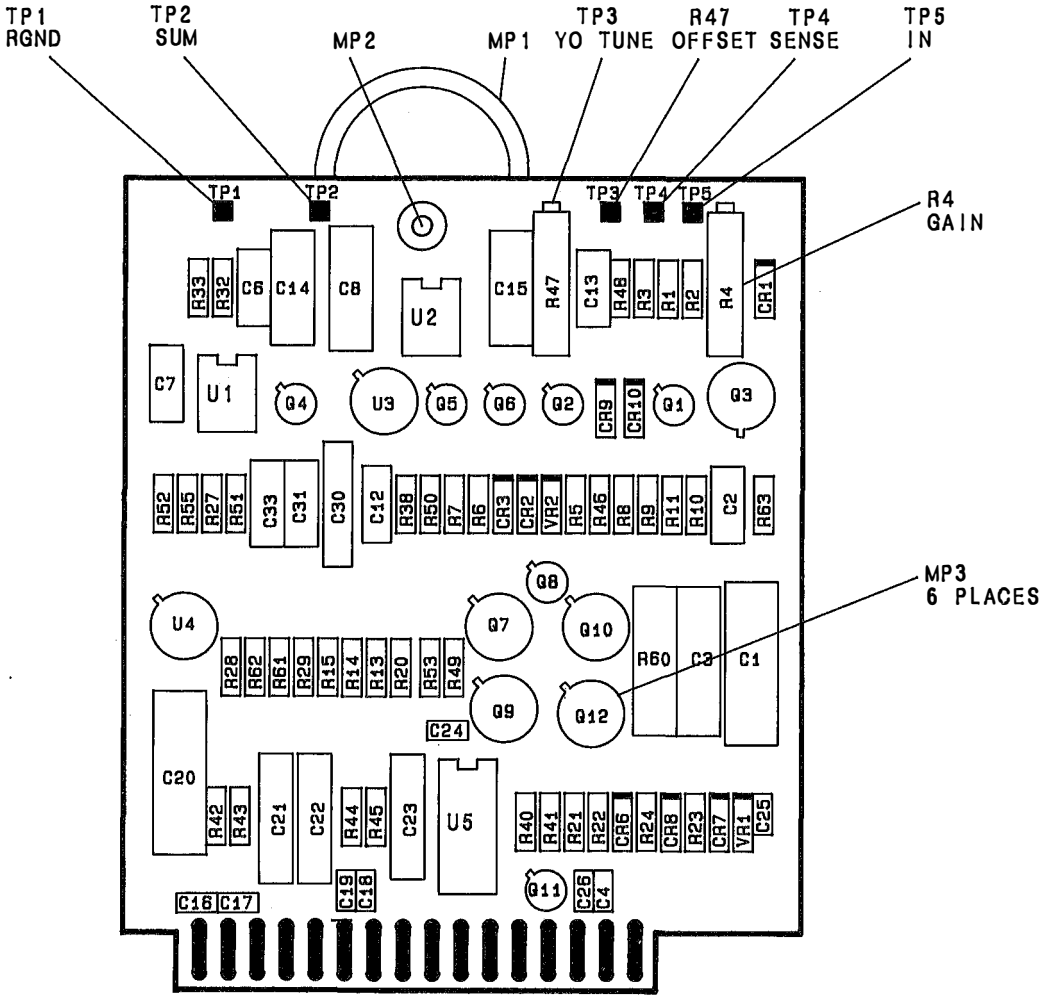


Figure 8D-15. A55 YO Driver, Component Location Diagram

A55 YO Driver P1 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 16	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*G *G
2 17	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*G *G
3 18	−40V/−40V SENSE (−) −40V/−40V SENSE (−)	−40V −40V	XA53P1-11, 30/XA53P1-23 XA53P1-11, 30/XA53P1-23	*G/NOT USED *G/NOT USED
4 19	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*G *G
5 20	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
6 21	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
7 22	LYSP HSP	TTL (LDW TRUE) TTL (HIGH TRUE)	XA59P1-11 XA57P1-13	C D *C
8 23	PRETUNE PRETUNE	−25V/GHZ, 0V = 2.3 GHZ −25V/GHZ, 0V = 2.3 GHZ	XA54P1-24 XA54P1-24	*A *A
9 24	VCOMP YD TUNE	−26 MHZ/VOLT 0V ± 6 V	XA54P1-27 E	F A62J6-SMC CENTER
10 25	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*H *H
11 26	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*H *H
12 27	SR FBK SR FBK	−5V TO −17V −5V TO −17V	A A	A62J29-2 A62J29-2
13 28	SR PWR SR PWR	−5V TO −17V −5V TO −17V	B B	A62J29-3 A62J29-3
14 29	HCEN YOXISTB	TTL (HIGH TRUE) −30V TO −39V	XA59P1-67 B	XA55P1-14 A62J29 PIN 4
15 30	YO COIL + YO COIL +	−40V TO −20V −40V TO −20V	B B	* *

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

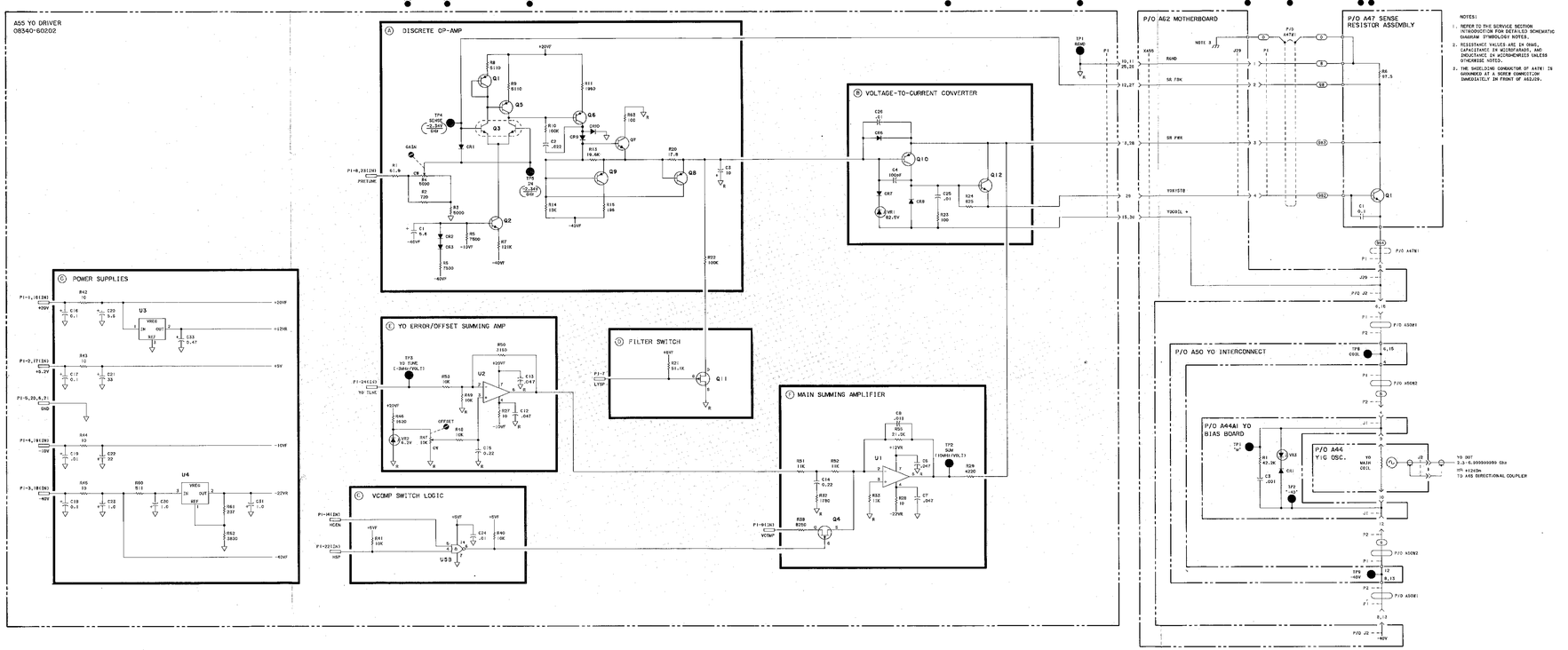


Figure 8D-16. A55 YO Driver, Schematic Diagram

A58 SWEEP GENERATOR

INTRODUCTION

The major function of the A58 Sweep Generator board is to generate three voltage ramps: VSWP (TP10), MKR RMP (TP4), and 20-30 SWP (TP8). VSWP is the ramp voltage that will sweep the YO over the frequency range of interest. When the 8340A is set for a sweep width of greater than or equal to 500 KHz and the entire sweep is contained on one band, the A54 YO Pretune board generates the voltage that tunes the YO to the start frequency of the sweep. VSWP is then summed into the PRETUNE voltage. (VSWP is zero volts at the beginning of the sweep.) Next the 8340A acquires phase-lock at the start frequency. When the sweep is initiated, the YO error voltage (YO TUNE) is sampled and held by the A49 YO Loop Phase Detector, and it remains constant for the duration of the sweep. Finally the loop is opened, and VSWP is allowed to ramp up and sweep the YO from the start frequency to the stop frequency. Thus the PRETUNE voltage always corresponds to the YO frequency. This type of sweep scheme is called lock and roll.

When the sweep is contained in two or more multiply bands, the 8340A re-phase-locks the YO and VSWP resets to zero at each bandcrossing. Thus, in the multi-band case, VSWP provides the voltage to sweep the YO from the last phase-lock frequency (start frequency or last bandcross frequency) to the stop frequency or the next bandcross frequency, whichever the case may be.

VSWP has a sensitivity of +2 Volts/GHz of YO frequency. The distinction between YO frequency and instrument frequency is important because the instrument frequency is not necessarily the same as the YO frequency. In the 10 MHz to 2.5 GHz band (Band 0), the YO output is heterodyned with a 3.7 GHz oscillator. Consequently, the YO frequency in this case is 3.7 GHz higher than the instrument frequency.

In the higher bands (SYTM multiply bands 1 through 4), the instrument frequency is derived from the first, second, third, or fourth multiple of the YO frequency as shown in Table 8D-3 below.

Table 8D-3. Instrument Frequency vs. YO Frequency

Band		Instrument Frequency	YO Frequency
Heterodyne	0	0.01 to 2.5 GHz	3.71 to 6.2 GHz
Multiply	1	2.3 to 7.0 GHz*	2.3 to 7.0 GHz
Multiply	2	7.0 to 13.5 GHz	3.5 to 6.75 GHz
Multiply	3	13.5 to 20.0 GHz	4.5 to 6.67 GHz
Multiply	4	20.0 to 26.5 GHz	5.0 to 6.625 GHz

* Refer to Section I, Figure 1 in Table 1-1, Specifications, for specific bandcross information versus swept mode used.

It is because of this harmonic operation of the 8340A that bandcrossings are necessary. At each crossing, VSWP resets to zero and the YO is phase-locked to the appropriate frequency for the start of the next band. The result is that in a multi-band sweep the Marker Ramp is a monotonic ramp which pauses for bandcrossings, and VSWP is a series of ramps each starting at zero volts. The slope of any particular ramp depends upon the YO harmonic being used in that band. Figure 8D-17 shows the basic characteristics of the Marker Ramp and VSWP for a full-band, 10 MHz to 26.5 GHz sweep.

The MKR RMP is a 0 to +10 Volt ramp that is used as the reference for all sweep events. It is related to the Sweep Out, but since there is other circuitry between the Ramp Generator (Block **K**) and Sweep Out, the Ramp Generator output is called Marker Ramp. On the A58 Sweep Generator board, the Marker Ramp is fed through the Summing Amplifier (Block **L**) and Sweep Width DAC (Block **M**) to give the 20-30 SWP ramp that sweeps the 20-30 Loop for narrow instrument sweeps (YO sweep width less than 5 MHz). This voltage is then run through the Sweep Width Range Attenuator (Block **N**) to give VSWP. In addition, the Marker Ramp goes to the A57 Marker/Bandcross board where it is buffered and sent to the SWEEP OUT (X-axis) ports on the front and rear panels. Finally, the A57 Marker/Bandcross board uses the Marker Ramp to determine when all sweep events (markers, bandcrossings and ends of sweeps) are to occur.

As mentioned before, the Marker Ramp is always a 0 to +10 volt ramp. In a single band sweep, the voltage goes linearly from 0 to +10 volts in the selected sweep time. In a multi-band sweep, the voltage is a segmented ramp where the linear ramp portions correspond to the particular bands being swept and the flat portions correspond to the time necessary to re-phase-lock the instrument for the next band to be swept. In the multi-band case the sum of the times for the various linear ramp portions will

equal the selected instrument sweep time. That is to say, the sweep time of the instrument is the time during which the instrument is actually sweeping and does not include the re-phase-lock time at each bandcrossing. Figure 8D-18 shows a "typical" Marker Ramp in the single and multi-band cases.

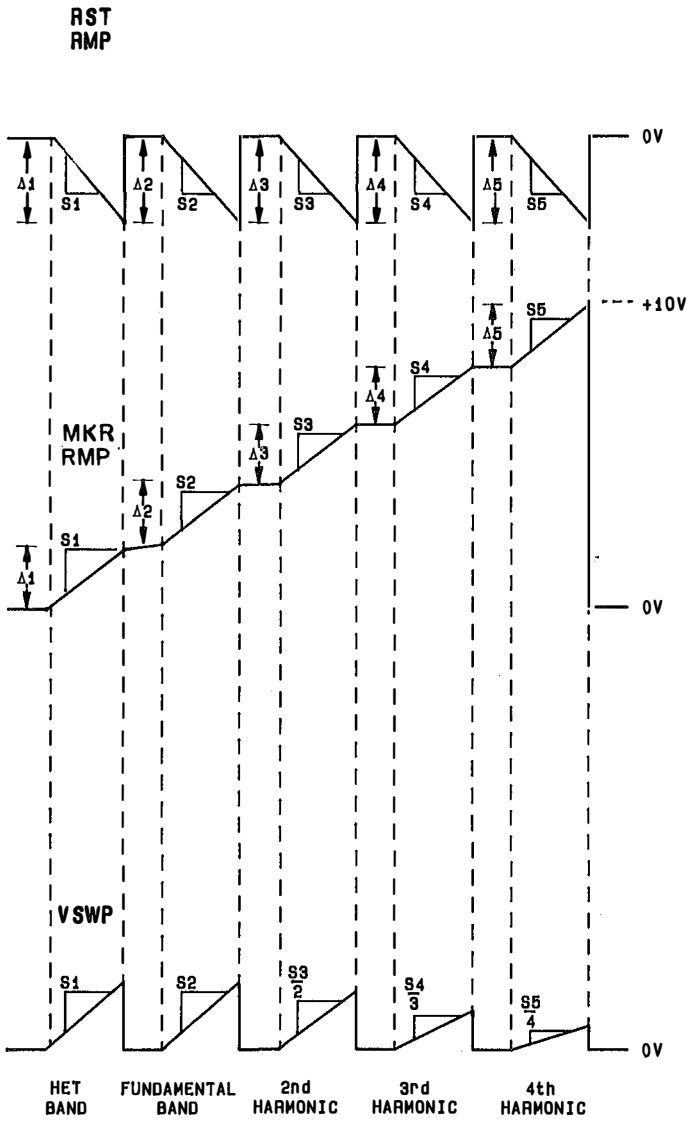


Figure 8D-17. Marker Ramp and VSWP Waveforms

A58 SWEEP GENERATOR CIRCUIT DESCRIPTION

Sweep Time Register A

U20 and U22 latch digital information from the instrument Data Bus which is then sent to the Sweep Time DAC (Block **G**). The strobe for these two latches is 1,R1:, WSPTM (Write Sweep Time). Resistors in U19 and U21 back bias the output stages of the latches when they are HIGH. This helps keep bus noise from feeding through to the DAC. U23 is a latched 3-to-8 decoder that latches the information for the Sweep Time Switch drivers. U23 is latched using the same strobe as U20 and U22.

Reset Register B

U25 and U27 latch information from the instrument Data Bus and direct it to the Reset DAC, U5. The latch strobe is WRDAC (Write Reset DAC 1,R2:). U24 and U26 contain pull-up resistors to back bias the outputs of U25 and U27 when the outputs are HIGH. This keeps noise on the bus from getting to the Reset DAC (Block **C**).

Reset DAC C

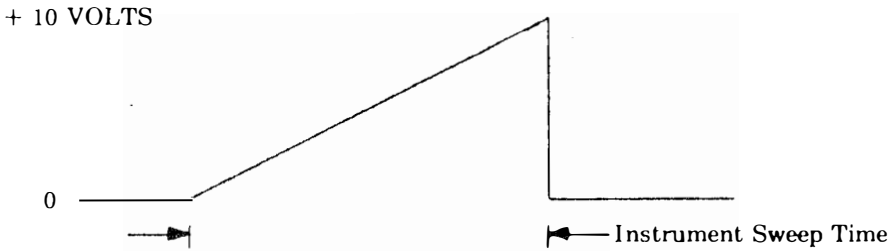
This is a current output DAC. It is referenced to the -7V Voltage Reference (Block **D**), and its output goes to the Summing Amplifier (Block **L**). R1, R19 and R20 set the gain of the DAC. C19 provides DAC compensation.

This block can be checked out by setting the instrument to any single band sweep and stopping it at the end of the sweep by using the "SHIFT XTAL" function. This will stop the Marker Ramp at +10 volts. Now, by writing to the Reset DAC (Block **C**) the voltage at the RST RMP test point (TP2) can be changed. If zero is written to the DAC, the voltage at TP2 should be +10 volts. If 1023 is written to the DAC, the voltage at TP2 should be zero. Refer to Direct I/O Addressing in Section VIII, "Service", for the front panel programming information.

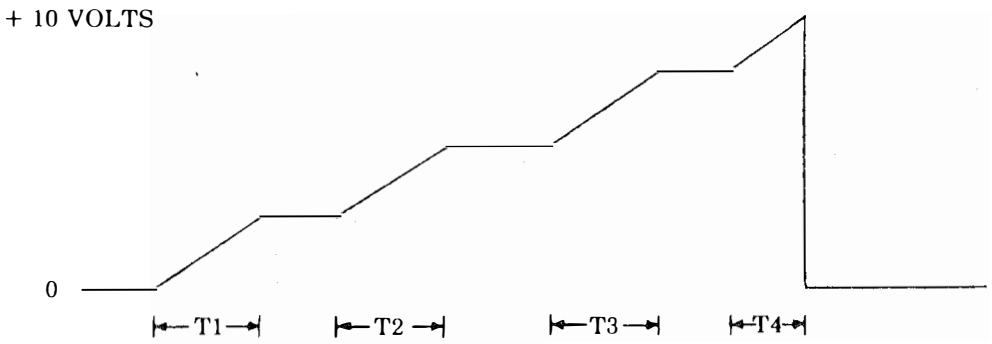
Voltage Reference D

The reference voltage is derived from VR1, a low noise, low TC, reference diode. R3 maintains a constant current through the diode, and R18 together with C1 give noise filtering. Operational amplifier U15 buffers and provides the gain necessary to make the reference voltage nominally -7V. R2 and R17 set the gain of U15.

MARKER RAMP - SINGLE-BAND CASE



MARKER RAMP - MULTI-BAND CASE



T1 + T2 + T3 + T4 = Instrument Sweep Time

Figure 8D-18. Typical Marker Ramp Waveforms

Sweep Width Register E

U34 is a latched 3 to 8 decoder which latches information from the instrument Data Bus and feeds it to the Sweep Width Range Switch Driver (Block **F**). A given line is selected when it is a TTL LOW.

U29 and U31 latch the information for the Sweep Width DAC (Block **M**). The strobe for the entire Sweep Width Register is 1,R0:, WSPAT (Write SweeP ATtenuator). U28 and U30 reverse bias any HIGH output stages in U29 and U31 to keep bus noise from getting into the Sweep Width DAC.

Sweep Width Range Switch Driver F

U35 and U37 are open collector comparators that convert the digital information from the Sweep Width Register (Block **E**) to voltages that will drive the switches in the Sweep Width Range Attenuator (Block **N**). The outputs of these comparators are pulled up by U36 to a voltage equal to VSWP. This ensures that the switch drivers can turn on the switches (in the SWP Width Range Attenuator, Block **N**) for every value of VSWP.

Sweep Time DAC G

U2 and U1 take the digital input from the Sweep Time Register (Block **A**) and convert it to the appropriate voltage. R39 provides a fixed trim for the gain of U2. C22 is for op-amp stablization.

The voltage at TP1 should be +10 volts when all the input bits to U2 are HIGH. This will occur whenever the selected sweep time is at the low end of a particular decade range (i.e., 10 msec, 100 msec, 1 sec, 10 sec or 100 sec). As the sweep time is increased the voltage at TP1 will decrease until it is +1 volt at the top end of the particular decade range of sweep time.

Sweep Time Switch Drivers H

The Sweep Time Switch Drivers take the digital input from the Sweep Time Register (Block **A**) and convert it to a voltage that drives switches Q1 through Q4. U3 serves to pull up the open-collector outputs of U4.

When an output of U4 is at ground, the FET that it is connected to will be turned on. When the output is at -10 volts, the FET will be off.

Sweep Scaling Resistors I

The Sweep Time DAC (Block **G**) and the Sweep Time Scaling Resistors (Block **I**) function together as a current source that produces a current proportional to the selected sweep time. The higher the current, the shorter the sweep time. The Sweep Time DAC (Block **G**) produces a voltage which is applied to the Sweep Time Scaling Resistors (Block **I**). Since the output of the Sweep Time Scaling Resistor block is held at ground, the voltage from the DAC is converted to a current which then goes through the Virtual Ground Amplifier (Block **J**) and then into C30. In deriving the current, which corresponds to the selected sweep time, the Sweep Time Scaling Resistors (Block **I**) select the appropriate decade range, and the Sweep Time DAC (Block **G**) does the interpolation within the range.

Virtual Ground Amplifier J

Figure 8D-19 is a simplified schematic of the Ramp Generator (Block **K**). The input to the Ramp Generator is a current source formed by the Sweep Time DAC (Block **G**), the Sweep Time Scaling Resistors (Block **I**), and the Virtual Ground Amplifier (Block **J**). Since the non-inverting input of U8 is connected to ground, the op-amp will keep its inverting input at ground also. That is, it will create a virtual ground at the Virtual Ground test point (VGND, TP3). It does this by varying the voltage at the gate of Q5. This varies the resistance of that FET and therefore varies the voltage drop across it. The voltage across C30 (Ramp Generator, Block **K**) is always negative, and the conventional current flow is always into the source and out of the drain of Q5.

CR2 and CR3 are low leakage diodes used for current steering.

Ramp Generator K

The Marker ramp signal is generated by feeding a constant current into C30. The voltage across the capacitor is buffered and offset to produce the 0 to +10 volt Marker Ramp. Figure 8D-19 is a simplified schematic showing the ramp generating scheme. These ramp generating circuits operate in one of three distinct states or modes, depending upon the positions of S1 and S2. Since the current source formed by the Sweep Time Scaling Resistors (Block **I**) and the Sweep Time DAC (Block **G**) is always on, the positions of S1 and S2 determine where the current will go.

The first mode is the sweep mode. In this case both S1 and S2 are open, and the current flows into C30. The second mode is the pause or hold mode. Here S1 is open and S2 is closed. This turns on the Current Shunt and diverts the current through through CR3, a current steering diode. The third mode is the reset mode. Here S1 is closed and S2 is open, and the current through CR2 is diverted by switch S1 into the output of U14.

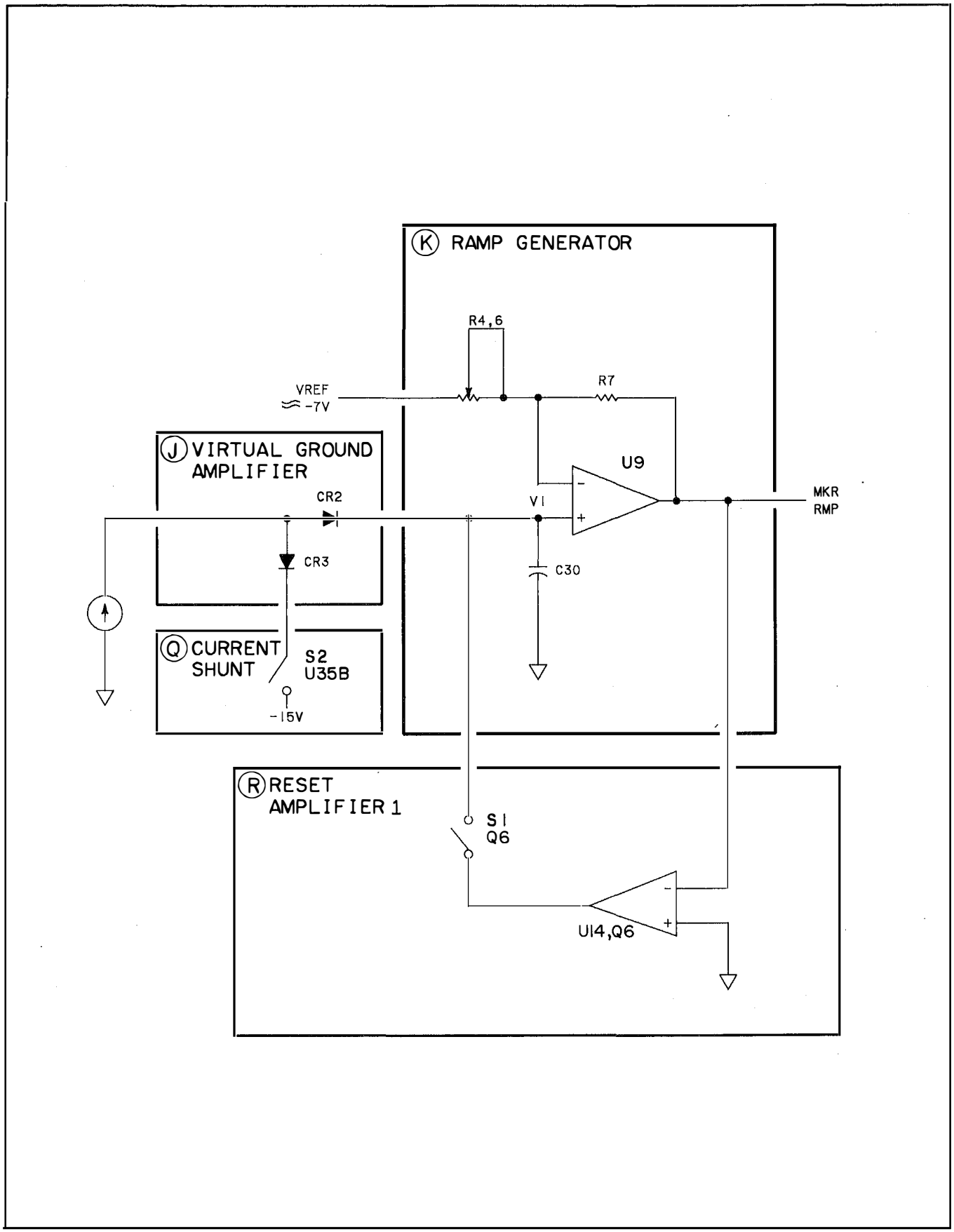


Figure 8D-19. Simplified Ramp Generator

When the sweep is reset, switch S1 (Q6) in Reset Amplifier 1 (Block **R**) is closed. Since the non-inverting input of U14 is grounded, it forces the inverting input to be at ground also. To accomplish this, U14 will discharge C30 to its reset voltage and divert the current from the current source away from C30 (once it is reset) so that the voltage across C30 does not change. The voltage across C30, after the ramp has been reset, is dependent upon the gain from the non-inverting input to the output of U9, and upon the gain from the VREF input to the output of U9.

Since the output of U9 is held at zero by the loop, it is possible to write an equation which describes the voltage at the output of U9 as a function of VREF and the voltage across C30, V1. One can then solve for V1.

$$0 = V1[1+(4640/1620)] - VREF(4640/1620)$$

$$V1 = VREF \times 0.74$$

VREF = approx. -7 volts; therefore, V1 = approx. -5.18 volts.

This assumes that potentiometer R4 is set to zero Ohms. V1 will vary with VREF.

A sweep is initiated by opening switch S1 (Q6) in the Reset Amplifier 1 (Block **R**). The output of the current source is now directed into C30. This constant current into a constant capacitance gives rise to a voltage across C30 that increases linearly. The output of the Ramp Generator (Block **K**), MKR RMP, will increase linearly from 0 to +10 volts where the sweep will be stopped. At this point, the voltage across C30 will have increased, become less negative, to a value that is dependent upon the gain from C30 to the output of U9. This gain is 1+(4640/1620) = 3.864. So when Marker Ramp increases by 10 volts, the voltage across C30 will increase by 10/3.864 = 2.56 volts. Thus at the end of any sweep, the voltage across C30 will be approximately -5.18 + 2.56 = -2.62 volts.

The foregoing discussion of Marker Ramp has been for the single band case. During a multi-band sweep the ramp must pause at each bandcrossing while the instrument phase-locks for the next band. To do this, the Current Shunt (Block **Q**) is turned on and U35B diverts the output of the current source away from C30. CR2 keeps the Current Shunt (Block **Q**) from discharging C30. Since current is no longer going into C30, the voltage across it will simply stay constant at the value that was present when the Current Shunt was turned on. When the bandcrossing is finished, the Current Shunt (Block **Q**) is turned off and the Ramp Generator

(Block **K**) continues to sweep up to +10V. This pause in the ramp will occur once at each bandcrossing. CR3 keeps U35B from sourcing current through CR2 and into C30.

Because any stray current flowing into C30 will cause an error, a guard trace surrounds the entire node comprised of C30, pin 3 of U9, the cathode of CR2, and the source of Q6. To keep the voltage on the guard trace always at the same potential as the node that it protects, the voltage at the inverting input of U9 is buffered by U10B and applied to the guard trace.

R4 is the SWEEP TIME adjustment. It varies the gain from C30 to the output of U9. This varies the slope of Marker Ramp. Since Marker Ramp is always at +10 volts at the end of a sweep, varying the slope of the ramp will vary the time that it takes to complete the sweep (i.e., it will vary the sweep time).

Summing Amplifier L

During single band sweeps the output of the summing amplifier is a 0 to -10V ramp. During multi-band sweeps, however, Marker Ramp will pause at each bandcrossing. At this time VSWP resets to zero for the next phase-lock point. This resetting is accomplished by summing the output of the Reset DAC (Block **C**), the Ramp Generator (Block **k**), and the Reset Amplifier 2 (Block **T**) via the Summing Amplifier (Block **L**). At any particular lock point the instrument processor knows what value the Marker Ramp voltage should be. The processor then programs the Reset DAC (Block **C**) to sink a current that is subtracted from the current generated by Marker Ramp, R8, and R9. This drives the output of U6 toward zero. Since the Reset DAC has finite resolution, it is also necessary to provide analog circuitry to bring the output of U6 to exactly 0 volts. Reset Amplifier 2 (Block **T**) generates an error voltage from the output of the Summing Amplifier (Block **L**) which, when applied to the Summing Amplifier, will force that output to zero. R13, SWP GAIN, varies the gain of U6 slightly to adjust for any gain error in the path from MKR RMP to VSWP.

Refer to Figure 8D-17, MKR RMP, RST RMP, and VSWP Waveforms. The output of the Summing Amplifier (Block **L**) is a series of voltage ramps, each ramp corresponding to one of the bands being swept. During single band sweeps the output of the summing amp will be a single 0 to -10V ramp. During multi-band sweeps the output duplicates the slope and delta-voltage of Marker Ramp, but is inverted and resets to 0V at each bandcrossing. When the first bandcrossing occurs, MKR RMP signal pauses and the output of the summing amplifier increases to 0V. When the MKR RMP signal resumes, the summing amp output matches the slope and delta-amplitude of Marker Ramp from this bandcrossing point to the next. This process repeats until the end of sweep. If the

voltage change of each summing amplifier ramp is added together, the total will equal 10 volts, regardless of the number of ramps during one sweep.

Sweep Width DAC M

The Sweep Width DAC performs two functions. First, it attenuates its input by a factor of 1, 2, 3 or 4 depending upon which harmonic is being swept. Secondly, it attenuates its input to give the appropriate sweep width. The actual sweep width is determined jointly by the Sweep Width DAC and the Sweep Width Range Attenuator (Block **N**). The Sweep Width Range Attenuator (Block **N**) selects the correct decade range, and the Sweep Width DAC then interpolates within that selected range. The two Sweep Width DAC attenuation factors are multiplied together by the instrument processor, and the result is applied to the digital input of the Sweep Width DAC.

CR5 protects U11, which is a CMOS device, in the event that the +5 volt supply comes up before the +15 volt supply. CR7 protects CR5 in the event that the +15 volt supply is shorted to ground. CR6 protects the output of U11 by keeping it from going much below ground. C39 is a compensation capacitor.

To check out this DAC, use the "SHIFT, XTAL" function in a single band sweep to stop the sweep with Marker Ramp at +10 volts. The voltage at TP2 (RST RMP in Summing Amplifier, Block **L**) should also be at +10 volts. Now the Sweep Width DAC can be programmed directly and the output voltage at TP8 (20-30 SWP in Sweep Width DAC Block **M**) observed. A digital input of zero should give zero volts out, and an input of 4096 should give +10 volts out.

Sweep Width Range Attenuator N

R58, R59, R61, and R62 form a decade voltage divider stack. The voltage at each node is a factor of 10 smaller than the voltage at the node above it. This particular arrangement was used so that the impedance at each node is low and approximately equal. This was necessary in order to reduce the susceptibility to radiated noise. Q8, Q10, or Q12 is turned on to select the appropriate node. U17 is a unity gain buffer which drives the VSWP line.

In instrument sweeps of greater than 5 GHz, a gain of six is necessary in this block. To accomplish this, Q7 is turned on and the output of U16 is fed to the buffer.

Only one of the FET switches in this block should be on at any given time. VSWP is fed back to U36 in Sweep Width Range Switch Driver (Block **F**) and becomes the supply voltage for the range

switch pull-up resistors. When a FET is on, the voltage at its gate should be equal to VSWP. When the FET is off, the gate voltage should be approximately -15 volts.

In sweep widths where the YO would be sweeping less than 5 MHz, the 20-30 Loop is swept and the YO loop stays phase-locked. This scheme gives better noise performance for narrow sweeps. However, for the first range of sweep widths where the YO sweep width is between 500 kHz and 5MHz, the PRETUNE voltage is also swept. Since the SYTM also uses the PRETUNE voltage, this improves the YO/SYTM tracking. In this case Q9 is turned on.

For sweeps narrower than 500 kHz, tracking is not a problem (the SYTM bandwidth is about 25 MHz), and only the 20-30 Loop is swept.

It is important to note that the sweep mode used, 20-30 Loop sweep, or PRETUNE sweep, depends not on the actual instrument sweep width but the YO sweep width. For instance, if the instrument is set to sweep from 20 GHz to 24 GHz, the instrument sweep width is 4 GHz but the YO sweep width is 1 GHz. This is because the fourth harmonic of the YO is being used.

For YO sweep widths less than 500 kHz, in MANUAL or CW modes, VSWP is turned off. This is done by turning on Q11 which grounds the input of the buffer U17. This keeps any noise from the Sweep Generator from getting to the Pretune DAC and degrading the phase noise performance.

Sweep Buffer O

U18 simply inverts VSWP. This output (BVSWP) is used on the A27 Level Control board ADC to measure VSWP when trouble-shooting the sweep circuitry.

Sweep Control Logic P

The Sweep Control Logic takes HSP (High Sweep), LRSP (Low Reset Sweep), and LBX (Low Bandcross) and generates control signals to drive the front panel sweep LED (LSPLD Low Sweep LED), Reset Amplifier 1 (Block **R**), the Current Shunt, and the Reset Control Logic.

The Sweep Control Logic timing diagram, Figure 8D-20, shows what happens at the end of sweep and at bandcrossings. The arrows and numbers indicate the sequence of events as well as the cause and effect relationship of various transitions.

When Marker Ramp gets to +10 volts, indicating the end of a sweep, LBX (Low Bandcross, TP6) goes LOW. This interrupts the

instrument processor which pulls down HSP (High SweeP) on the A57 Marker Bandcross board. HSP going LOW causes the LOW ENABLE RESET AMP 2 line to go LOW. This in turn forces LHLD (Low Hold Sweep, TP12) LOW, turning on the Current Shunt (Block **Q**). Finally LSPLD (Low Sweep LED U32A pin 3) goes HIGH, turning off the front panel sweep LED.

At the appropriate time the instrument processor asserts LRSP (Low Reset Sweep, TP11) which causes LRESET (Low Reset, TP13) to go LOW. This allows Reset Amplifier 1 (Block **R**) to pull the output of U9 to ground. LRESET going LOW causes LHLD to go HIGH, turning off the Current Shunt.

During the re-phase-lock sequence, the instrument processor releases LBX and LRSP. These events do not cause any changes on the Sweep Generator board.

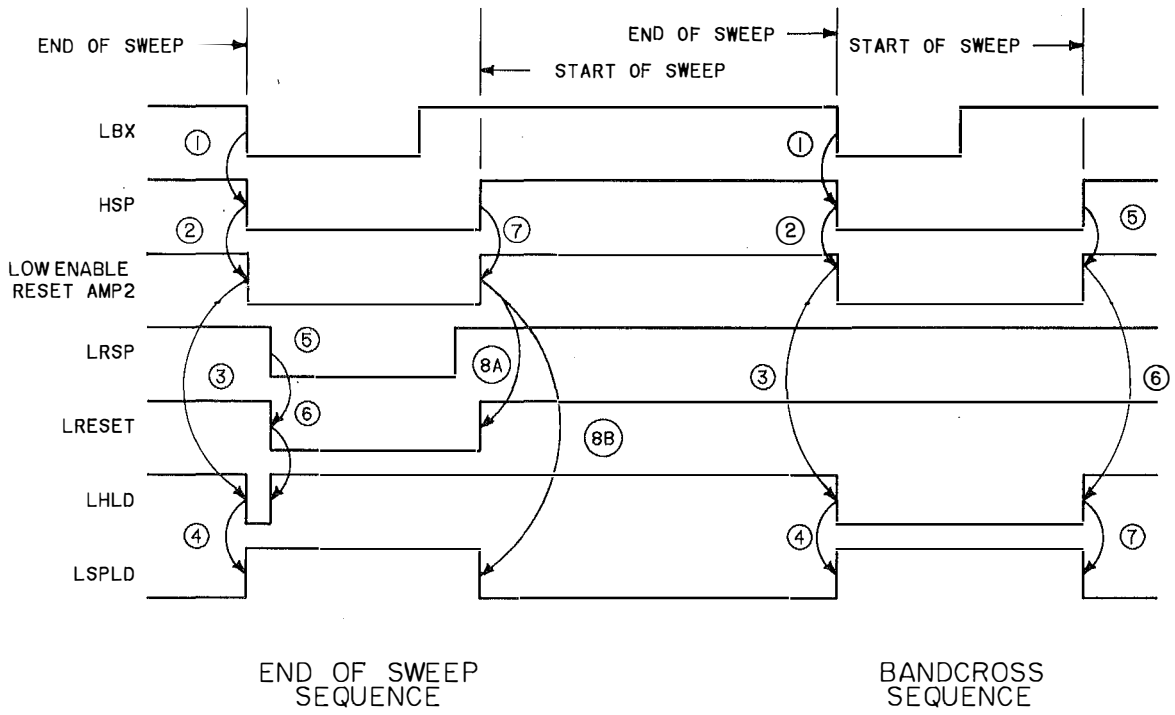


Figure 8D-20. Sweep Control Logic Timing Diagram

When the processor is ready for the next sweep, it lets HSP go HIGH. This causes LOW ENABLE RESET AMP 2 to go LOW. This forces LRESET HIGH and LSPLD LOW, and the sweep proceeds.

At a bandcrossing, the A57 Marker/Bandcross board pulls down LBX, which is coupled to HSP at U33C. This enables LOW ENABLE RESET AMP 2, and LSPLD HIGH and LHLD LOW. This causes the ramp to pause, but since LRSP is not pulled down by the processor, Marker Ramp does not reset. When the new information is written to the Reset Register (Block **B**), its strobe, WRDAC, causes the output of the Reset Control Logic (Block **S**) to go LOW which in turn forces the output of U6 (Block **L**) to ground.

During the re-phase-lock routine, the instrument processor lets LBX go HIGH. Then when it is ready for the next portion of the sweep, it releases HSP. This pulls LOW ENABLE RESET AMP 2 HIGH which ultimately releases the output of U6. It also makes LHLD go HIGH and LSPLD go LOW, and the sweep continues.

U33A and U33D are connected as an R/S flip-flop. As long as only one of its inputs (U33A pin 1, U33D pin 12) is LOW at any given time, its outputs (U33A pin 3, U33D pin 11) will be the opposite TTL level. That is, if one is HIGH, the other will be LOW, and vice versa. It would seem that U32D, which is used as an inverter, could be eliminated by connecting U33A pin 3 to U32D pin 2. However, when the instrument is in the CW or MANAL mode, LBX and HSP are HIGH while LRSP is LOW. This causes both outputs of the flip-flop to be HIGH. Hence the need for U32D.

Current Shunt Q

When the voltage at the non-inverting input of U35B is a TTL logic LOW, <1.4 volts, the output of U35B pulls to -10 volts. This shunts the current coming through Q5, in the Virtual Ground Amplifier (Block **J**), through CR3 and back biases CR2 so that C30 cannot discharge. When the input to U35B is a logic HIGH, its open collector output is pulled to +5 volts by R5. This reverse biases CR3 so that no current is diverted away from C30.

Reset Amplifier 1 R

When the inverting input of U35A, LRESET, is a TTL logic LOW, the output of U35A is pulled to +20 volts by R36. This reverse biases CR1 allowing Q6 to turn on through R34. This closes the reset loop shown in Figure 8D-19. Since the non-inverting input of U14 is connected to ground, the loop forces the inverting input of U14 to also be at ground. This ensures that Marker Ramp is at zero volts at the start of a sweep.

C26, R43 and R44 are loop compensation components.

Reset Control Logic S

At any phase-lock event LOW ENABLE RESET AMP 2 (Block **T**) goes LOW. Then the instrument processor writes to the Reset Register (Block **B**). This LOW-going strobe, WRDAC, comes to the Reset Control Logic (Block **S**) and forces its output to go LOW. This puts U13 in Reset Amplifier 2 (Block **T**) in the sample mode and causes the output of U6 in Summing Amplifier (Block **L**) to be driven to zero. When a sweep is initiated, LOW ENABLE RESET AMP 2 (Block **T**) goes HIGH. This drives the output of U32B HIGH which puts U13 into the hold mode, thereby opening the loop and allowing the output of U6 to start sweeping.

Reset Amplifier 2 T

Since the inverting input of U7 is connected to ground, the reset loop will force the non-inverting input to be at ground also. The error voltage generated by U7 is fed to U13, which is a sample and hold. C31 is the sample and hold capacitor. R83 limits the charging rate of C31 and is required to make U13 stable.

When pin 14 of U13 is LOW, U13 is in the sample mode. This closes the loop and forces the output of U6 (pin 6) in the Summing Amplifier (Block **L**) to be at ground. When pin 14 of U13 goes HIGH, U13 goes into the hold mode and the loop is opened. As the sweep progresses and the output of U6 ramps up, the output of U13 will not change.

There is a guard trace around the node containing the sample and hold capacitor and U13 pin 11. This trace is connected to the output of U13 to keep it at the same potential as the sensitive end of C31.

Oversweep Detector U

When the instrument is operating correctly, the A57 Marker/Bandcross board will stop the sweep when the Marker Ramp gets to +10 volts. However, if that board is not working and the Marker Ramp reaches +12 volts, the OVERSWEEP DETECTOR pulls down the LBX line which stops the sweep and wakes up the processor. This allows the SWEEP GENERATOR to make repetitive sweeps even when the MARKER/BANDCROSS board is not functioning. This makes troubleshooting much easier. It should be noted however, that in the case when the OVERSWEEP DETECTOR is stopping the sweep, no bandcrossings will occur, and the frequency over which the instrument is sweeping will be incorrect.

LBX is an open-collector line that can be pulled down by several boards. Q13 provides the open-collector function on this board and buffers the output of U10A so that by looking at TP5, the HBX test point, one can determine if the SWEEP GENERATOR is the board pulling down on LBX. CR9 is a protection diode for the base-emitter junction of Q13, while R45, R46, and CR4 provide hysteresis for the detector function.

Power Supply Filtering V

The filtering is the standard low pass configuration. The particular L and C components were chosen to have a low-Q self resonance. R48 provides a reference ground for the board in the event that the connection between reference ground and chassis ground on the instrument is broken. Q14 and the associated components create a +15V supply referenced to RGND, This supply is used to provide symetrical ±15V supplies. R49 and R50 divide the +20V supply down to +1.4V to be used as the comparitor threshold for comparitors with TTL inputs. All supplies except +5V and +1.4V are filtered to RGND to prevent digital ground noise from being injected into the analog circuitry via the power supplies.

A58 SWEEP GENERATOR TROUBLESHOOTING

There are two basic failure modes that have to do with the sweep function of the instrument. One, the instrument is simply not sweeping. Two, it is sweeping, but the sweep is incorrect; the frequency limits of the sweep are wrong and/or bandcrossings are not occurring. The first task is to get the instrument to do repetitive sweeps of any kind.

If the Marker Ramp is sweeping and the front panel green LED is blinking, then the instrument is considered to be sweeping even though the output frequency may not be moving. If on the other hand Marker Ramp is stuck and the front panel sweep LED is continuously on or off, then the instrument is considered not to be sweeping. When looking at the LED, care must be taken because in fast sweeps it may appear to be on all the time, even though it is actually blinking.

No Sweep

Set the instrument to sweep continuously from 3 GHz to 7 GHz with a sweep time of 10 msec. Check the voltage at the SWP TIME DAC test point, TP1. It should be +9.77 volts. If you now press **[SINGLE]** SWEEP and then vary the sweep time from 10 to 99 msec, the voltage at this test point should go from +9.77 to +0.977 volts. Varations from these voltages by several tenths of a volt will affect the sweep time accuracy but not the board's ability to sweep.

Return to the continuous sweep mode with a sweep time of 10 msec. Look at the VGND test point, TP3. It should be at ground potential. Anything greater than ±50 millivolts indicates a problem.

If VGND is at zero volts but the instrument still is not sweeping, that is, Marker Ramp is not ramping, then check the output of the CURRENT SHUNT (U35B, pin 1). It should be +5 volts. If it is at -10 volts, then the SWEEP CONTROL LOGIC is erroneously turning on the CURRENT SHUNT.

At this point look at the voltage at the MRK RMP test point, TP4. If it is at ground, then the RESET AMPLIFIER 1 loop is probably closed and holding down the Marker Ramp. Check LRESEST, U35A pin 2, to make sure that it is LOW.

Once the Marker Ramp is behaving correctly, the instrument is considered to be sweeping, and if the output of the SWEEP GENERATOR board is not correct then the trouble-shooting proceedure for an incorrect sweep should be followed.

Incorrect Sweep

If the Marker Ramp waveform is correct, but the output of the SWEEP GENERATOR is still incorrect, then the various gain and attenuation stages must be checked. Set the instrument to sweep from 2.3 GHz to 7 GHz with a sweep time of 10 msec. The voltage at the MKR RMP test point, TP4, should be a ramp from 0 to +10 volts with a forward sweep time of 10 msec. Looking at the RST RMP test point, TP2, should show a ramp going from 0 to -10 volts in 10 msec. If this test point is stuck at ground, then check U13 pin 14 in the RESET AMPLIFIER 2 block. It should be a TTL HIGH during the forward sweep of the ramp and LOW the rest of the time.

Next look at the 20-30 SWP test point, TP8. It should be a ramp going from 0 to +9.4 volts. If it is not, then go to the single sweep mode and press the following key sequence: **[SHIFT] [XTAL]** (leveling). Then press the **[SINGLE]** SWEEP key once. This will cause the Marker Ramp to sweep to +10 volts and stop. Now, using Direct I/O, write a 0 to channel 1 sub-channel 0 by pressing this key sequence:

[SHIFT] [GHz] [1] [Hz]

[SHIFT] [MHz] [0] [Hz]

[SHIFT] [KHz] [0] [Hz].

Check the digital input to U11 (pins 4-15), they should all be LOW. TP8 should be at ground.

Now write a 4095 to the same strobe using the following key sequence: **[4] [0] [9] [5] [Hz].** This should make all the digital inputs to U11 HIGH. The voltage at TP8 should now be the opposite of the voltage at TP2. That is, since TP2 should be at approximately -10 volts, TP8 should be at about +10 volts. By turning the front panel RPG slowly and decreasing the number written to this strobe from 4095 to zero, the voltage at TP8 should go smoothly from +10 volts to ground. Press **[SHIFT] [XTAL]** to return the instrument to the normal operating mode.

Go to the continuous sweep mode and now check to see that the VSWP test point, TP10, is going from 0 to +9.4 volts. If not, then check to see that the gates of Q7-Q12 in the SWEEP WIDTH RANGE ATTENUATOR are at the correct voltage. See the circuit description Block **N** for the appropriate values.

Finally, if the instrument does single band sweeps correctly but does not do multi-band ones, check U5. This can be done by going

to the SINGLE SWEEP mode with the instrument set to sweep from 2.3 GHz to 7 GHz with a 10 msec sweep time. Press **[SHIFT] [XTAL]** (leveling) and **[SINGLE]** SWEEP to get the Marker Ramp to stop at +10 volts. While looking at TP2, write 1023 to Reset DAC (U5) as follows:

[SHIFT] [GHz] [1] [Hz]

[SHIFT] [MHz] [2] [Hz]

[SHIFT] [KHz] [1] [0] [2] [3] [Hz]

This should cause the voltage at TP2 to go to zero. By turning the RPG slowly and decreasing the number from 1023 to 0 the voltage at TP2 should decrease smoothly from zero to -10 volts. With zero written to U5, all the digital inputs to U5 should be LOW. With 1023 written, all inputs should be HIGH.

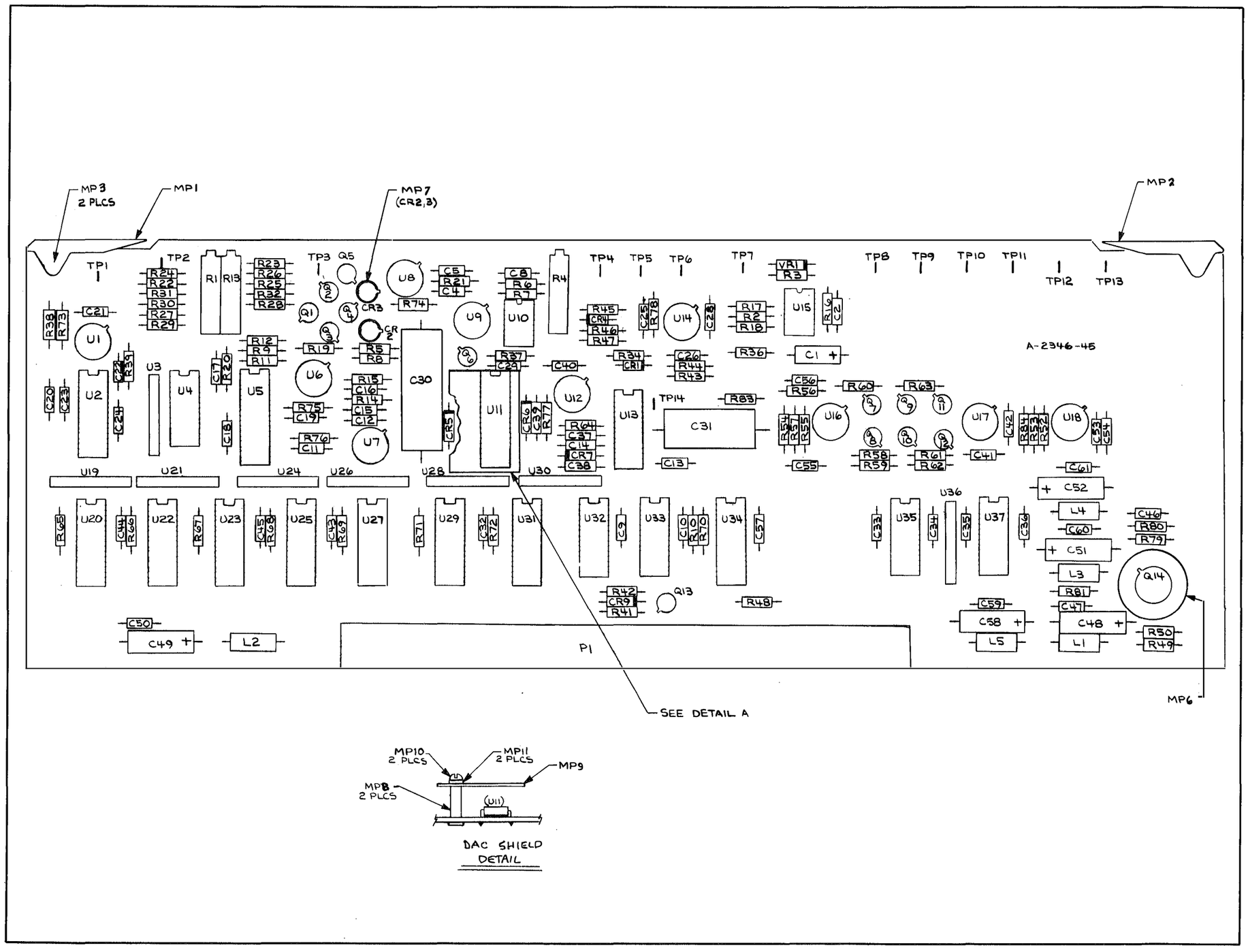


Figure 8D-21. A58 Sweep Generator, Component Location Diagram

A58 Sweep Generator P1 Pin I/O (1 of 3)

Pin	Mnemonic	Levels	Source	Destination
1 56	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*V *V
2 57				
3 58				
4 59				
5 60				
6 61				
7 62				
8 63				
9 64				
10 65				
11 66				
12 67	LSPLD	TTL	P	A62J1-44
13 68	HSP LVSZ	TTL (HIGH TRUE) TTL (LOW TRUE)	XA57P1-13 E	*P XA54P1-9 F
14 69	LIPS LBX	TTL (LOW TRUE) TTL (LOW TRUE)	* *U	*NOT USED XA59P1-69 P
15 70	SIDA GND PLANE	TTL (LOW TRUE) 0V	XA60P1-15 INSTRUMENT GROUND	*NOT USED *V
16 71	SIOB GND PLANE	TTL (LOW TRUE) 0V	XA60P1-16 INSTRUMENT GROUND	*NOT USED *V
17 72	ADR0 HFILYD	TTL TTL (HIGH TRUE)	XA60P1-17 XA59P1-72	*NOT USED *NOT USED
18 73	ADR2 ADR1	TTL TTL	XA60P1-18 XA60P1-73	*NOT USED *NOT USED
19 74	ADR4 ADR3	TTL TTL	XA60P1-19 XA60P1-74	*NOT USED *NOT USED

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A58 Sweep Generator P1 Pin I/O (2 of 3)

Pin	Mnemonic	Levels	Source	Destination
20 75	DB0 GND PLANE	TTL 0V	XA60P1-20 INSTRUMENT GROUND	*A B E *V
21 76	DB2 DB1	TTL TTL	XA60P1-21 XA60P1-76	*A B E *A B E
22 77	DB4 DB3	TTL TTL	XA60P1-22 XA60P1-77	*A B E *A B E
23 78	DB6 DB5	TTL TTL	XA60P1-23 XA60P1-78	*A B E *A B E
24 79	DB8 DB7	TTL TTL	XA60P1-24 XA60P1-79	*A B E *A B E
25 80	DB10 DB9	TTL TTL	XA60P1-25 XA60P1-80	*A E *A B E
26 81	DB12 DB11	TTL TTL	XA60P1-26 XA60P1-81	*A E *A E
27 82	DB14 DB13	TTL TTL	XA60P1-27 XA60P1-82	*A E *A E
28 83	WSPTM DB15	TTL (LOW TRUE) TTL	XA59P1-28 XA60P1-83	A *NOT USED
29 84	WRDAC WSPAT	TTL (LOW TRUE) TTL (LOW TRUE)	XA59P1-29 XA59P1-84	B S E
30 85	TYOKP LRSP	TTL (LOW TRUE) TTL (LOW TRUE)	XA59P1-100 XA59P1-85	*NOT USED P
31 86				
32 87				
33 88				
34 89	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*V *V
35 90	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*V *V
36 91	+5.2V +12V	+5.2V +12V	XA52P1-17, 18, 41, 42 XA52P1-9, 33	*V *NOT USED
37 92	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*V *V

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A58 Sweep Generator P1 Pin I/O (3 of 3)

Pin	Mnemonic	Levels	Source	Destination
38 93	−15V −5.2V	−15V −5.2V	XA56P1-15, 30 XA53P1-18, 36	*V *NOT USED
39 94	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*V *V
40 95	BVSWP	10V SWEEP	O	XA27P1-31
41 96	20/30 SWP MKR RMP	0V TO +10V 0 TO 10V SWEEP	M K	XA43P1-1 N XA57P1-96 R L
42 97	RGND VSWP	0V 0 TO 10V SWEEP	STAR GND POINT N	*V *F O
43 98	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*V *V
44 99	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*V *V
45 100	GND PLANE LCHNG	0V TTL (LOW TRUE)	INSTRUMENT GROUND *	*V *NOT USED
46 101	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*V *V
47 102	HFILYO	TTL (HIGH TRUE)	XA59P1-72	*NOT USED
48 103				
49 104				
50 105				
51 106				
52 107				
53 108	HXREF	TTL (HIGH TRUE)	A62J31-17	*NOT USED
54 109	LSRQ	TTL (LOW TRUE)	*	*NOT USED
55 110	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*V *V

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A58 SWEEP GENERATOR
08340-60154

Figure 8D-22. A58 Sweep Generator, Schematic Diagr
8-383/8-

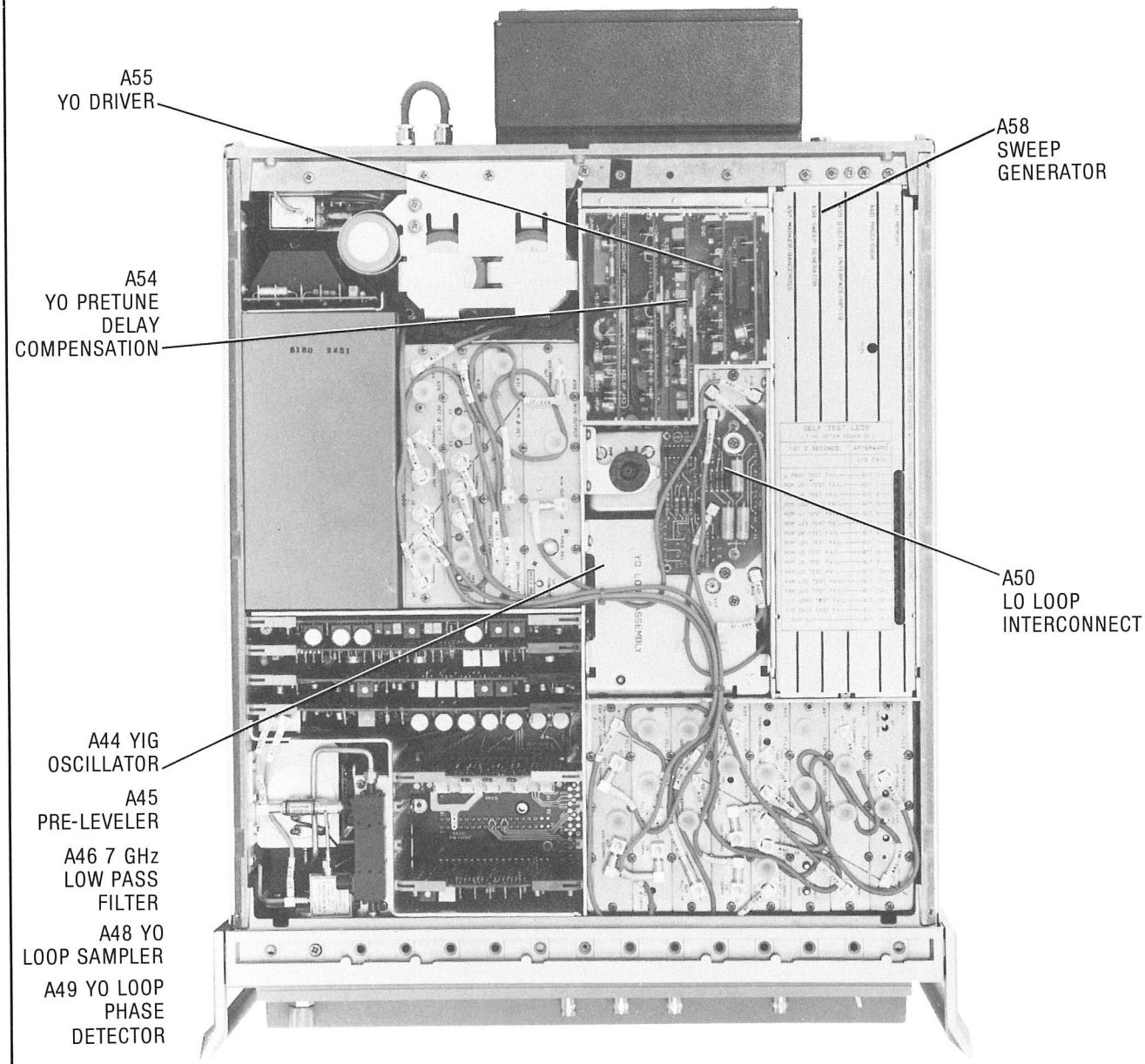
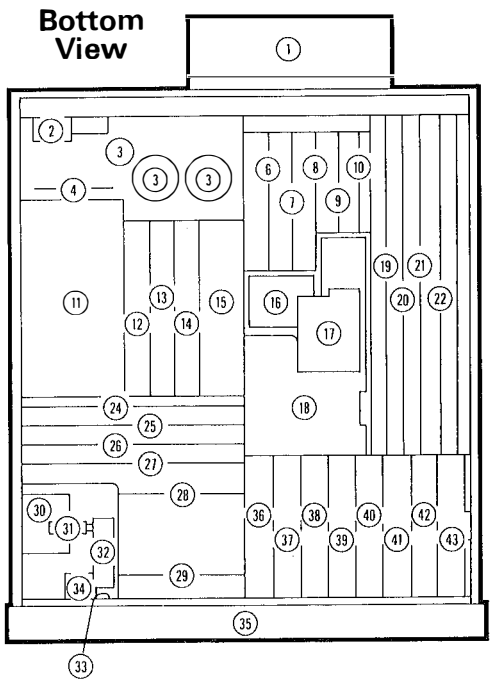
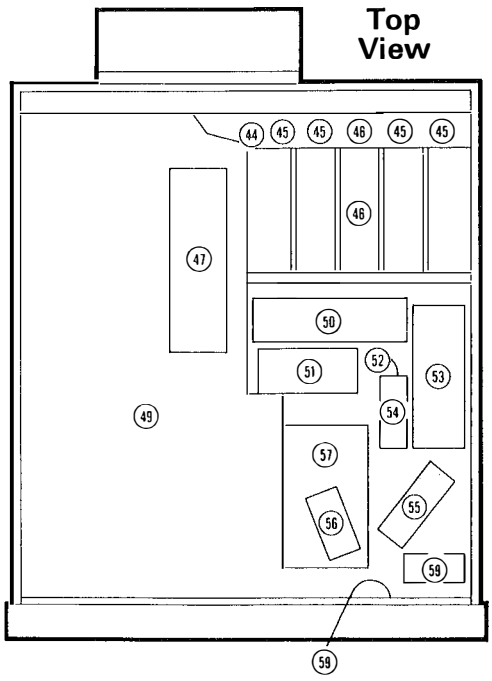


Figure 8D-23. Sweep Generator and YO Loop Major Assemblies Location Diagram

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 3						Volume 4	
			Ref.-M/N Loops	20-30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	33					●			
A2	Display Driver	33					●			
A3	Display Processor	33					●			
A4	Not Assigned	-								
A5	Keyboard	35					●			
A6	Keyboard Interface	35					●			
A7	Lower Keyboard	35					●			
A8	3.7 GHz Oscillator	57						●		
A9	Band 0 Pulse Modulator	56						●		
A10	Directional Coupler	32						●		
A11	Band 1-4 Detector	31						●		
A12	Band 0 Splitter/Detector	34						●		
A13	SYTM (Switched YIG Tuned Multiplier)	30						●		
A14	Band 1-4 Power Amplifier	53						●		
A15	Band 0 Low Pass Filter	52						●		
A16	Band 1-4 Modulator/Splitter	51						●		
A17	Band 0 Mixer	54						●		
A18	Band 0 Power Amplifier	55						●		
		60						●		
A19	Capacitor Assembly	48								●
A20	RF Section Filter	50						●		
A21	Pulse Modulator Driver	29						●		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRO Bias	28						●		
A25	ALC Detector	27						●		
A26	Linear Modulator	26						●		
A27	Level Control	25						●		
A28	SYTM Driver	24						●		
A29	Reference Phase Detector	12	●							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	●							
A31	M/N Phase Detector	14	●							
A32	M/N VCO (Voltage Controlled Osc.)	15	●							
A33	M/N Output	15	●							
A34	Reference-M/N Motherboard	5	●							
A35	Rectifier	4								●
A36	PLL1 VCO (Voltage Controlled Osc.)	36		●						
A37	PLL1 Divider	37		●						
A38	PLL1 IF	38		●						
A39	PLL3 Upconverter	39		●						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		●						
A41	PLL2 Phase Detector	41		●						
A42	PLL2 Divider	42		●						
A43	PLL2 Discriminator	43		●						
A44	YIG Oscillator (YO)	18			●					
A45	Directional Coupler	18			●					
A46	7 GHz Low Pass Filter	18			●					
A47	Sense Resistor Assembly (YO circuit)	47			●					
	(SYTM circuit)	47						●		
A48	YO Loop Sampler	18			●					
A49	YO Loop Phase/Detector	18			●					
A50	YO Loop Interconnect	17			●					
A51	Reference Oscillator	16	●							
A52	Positive Regulator	6								●
A53	Negative Regulator	7								●
A54	YO Pretune/Delay Compensation	8			●					
A55	YO Driver	9			●					
A56	−15V Regulator	10								●
A57	Marker/Bandcross	19				●				
A58	Sweep Generator	20			●					
A59	Digital Interface	21				●				
A60	Processor	22				●				
A61	Not Assigned	23				●				
A62	Motherboard	49								
A63	90 dB RF Attenuator	59						●		
AT1	Peripheral Mode Isolator	58						●		
AT2	15 dB Attenuator	18			●					
B1	Fan Assembly	1								●
A62C1-3	Power Supply Filter Capacitors	3								●
FL1	AC Line Module	2								●
A62Q1-4	Power Supply Regulating Transistors	45								●
A62S1	Power Supply Thermal Switch	44								●
T1	Power Supply Transformer	11								●
A62U1	Power Supply Regulator	46								●

MOTHERBOARD – WIRING LIST E

A62 MOTHERBOARD

Introduction

This section consists of the following items:

- A62 Motherboard description.
- Information concerning Motherboard troubleshooting techniques which includes a component location diagram and Motherboard repair and replacement procedures.
- A Motherboard wiring list that identifies signal mnemonics, typical levels, and sources and destinations of signals used on the Motherboard.

List of Assemblies Covered

Several components appear to be routed to the A62 Motherboard but are not actually discussed in detail in this section. Some of these items include the A47 Sense Resistor Assembly, the A51 Reference Oscillator Assembly, various mechanical parts, and certain casting assemblies. Refer to the following to determine which assemblies are covered and which are not covered in this section:

- Reference Guide to Service Documentation located on the front of each Service Section tab.
- The Illustrated Parts Breakdown List at the end of Section VI, Replaceable Parts.
- The A62 Motherboard Component Location Diagram (Figure 8E-2).
- The A62 Motherboard Wiring List (Table 8E-1).

A62 MOTHERBOARD DESCRIPTION

Introduction

The A62 Motherboard is the common board to which numerous other assemblies are connected and serves to route signals to other printed circuit boards where needed.

CAUTION

The A62 Motherboard is large and complex; it contains six trace layers with several hundred seperate signal paths. Read the entire Motherboard Section before attempting any troubleshooting, component replacement, or repairs on the A62 Motherboard or costly damage may result.

Grounds

Several different grounds are employed on the A62 Motherboard:

- **STAR GND** - STAR GND is the single ground reference point for analog circuitry in all major assemblies. Each assembly block is referenced to STAR GND via individual traces; this minimizes ground noise crosstalk between major assemblies. STAR GND is a screw terminal located between the A62XA57 Marker Bandcross and A62J3 connectors and is visible with the instrument top cover removed.

- **GND** - GND is used to designate individual analog ground traces connecting major assembly blocks to STAR GND. Many of these traces are physically large and are used for high current power supply applications.

- **GND PLANE** - Refer to Figure 8E-1, A62 Motherboard Cross Section for the following explanation.

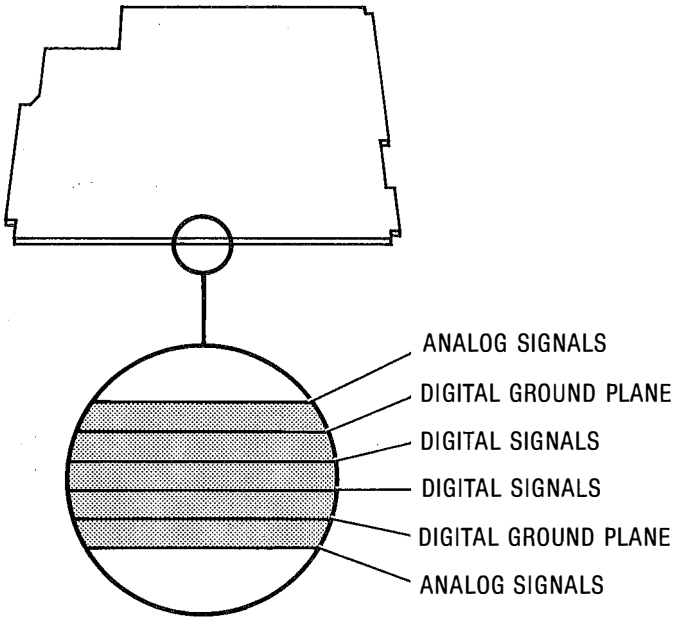


Figure 8E-1. A62 Motherboard Cross Section

As shown in Figure 8E-1, A62 Motherboard Cross Section, the GND PLANE exists between the two innermost and two outermost Motherboard printed circuit layers. These layers were designed to disperse any digital noise into the GND PLANES and act as an electrostatic shield between the digital and analog signal traces. The GND PLANES extend to each edge of the Motherboard and are connected to STAR GND. With this scheme, isolation between analog and digital grounds is maximized and signal crosstalk minimized.

- **REFERENCE GND** - This ground is connected to STAR GND and is used as a low current reference for integrated circuits, cable shields, etc. where a very clean reference is desired.

- **MISCELLANEOUS GROUND PLANES**
  A. The ground plane under the 20/30 Loops' aluminum casting completes a radio frequency interference (RFI) "box" comprised of the casting, assembly covers, and the 20/30 loops' ground plane. This ground plane is connected to STAR GND via a GND trace, and to chassis GND through the aluminum casting.

  B. Under the M/N Loop's aluminum casting is a ground plane which connects to STAR GND and is used as an RFI shield.

- **CHASSIS GND** - All grounds and ground planes are mechanically secured to the 8340A chassis (CHASSIS GND) around the perimeter and at various other places on the A62 Motherboard.

A62 MOTHERBOARD TROUBLESHOOTING

Introduction

Troubleshooting the A62 Motherboard is straightforward since the most common problems encountered are opens and shorts. Table 8E-1, A62 Motherboard Wiring List is included in this manual in lieu of an A62 Motherboard schematic diagram. If a signal is not present or is incorrect, refer to Table 8E-1, A62 Motherboard Wiring List and Figure 8E-2, A62 Motherboard Component Location Diagram to determine the signal source and its location. Ensure that the signal source circuitry is functioning properly and, if so, isolate the source by removing destination assemblies where possible. In most cases, the trouble will occur on other assemblies rather than on the Motherboard itself. Visually inspect the Motherboard for possible loose hardware, stray trim leads, solder splashes, and shorted or open traces. Be aware of feedthrough holes that may be making intermittent contact with inner layer Motherboard traces.

REPAIR PROCEDURES

Introduction

Repair and replacement of A62 Motherboard components and connectors is possible but successful only when the following guidelines are followed.

Component And Connector Replacement

NOTE

Unless otherwise mentioned, do not use a soldering iron with a tip temperature greater than 700 degrees F on Motherboard pads, and, in no case leave the iron on the connection any longer than absolutely necessary. Care must be taken when soldering and desoldering on the A62 Motherboard not to damage wires, cables, or other components located near the work area.

Where soldering iron accessability to Motherboard components is difficult, removal of individual assemblies may be necessary; refer to the replacement procedures of those assemblies for specific removal instructions.

To remove a component, heat one side of the component pad from either side of the board and carefully lift that lead out of the hole. Repeat the procedure with the remaining lead and, after the component has been removed, reheat each pad and use solder wick or an anti-static solder removing tool (vacuum type) to remove the solder from each hole. It is often helpful to have one person pull the component lead while another person heats the pad from the other side of the Motherboard.

Connectors A62XA57-61 are 110-pin male connectors whose pins may be individually replaced without need for replacing the entire connector. The one other connector with the same feature is A62J31.

NOTE

Individual pins are not available and if an individual male pin repair is required, an extra A62J31 connector should be ordered and pins removed from it for replacement purposes.

Have one person gently grab and pull the pin to be replaced from the component side of the Motherboard while another person heats the pin from the other side. Reheat the pad and use solder wick or an anti-static solder removal tool to remove the solder from the hole. Reverse the procedure when installing the new pin by holding the pin straight in the connector while the second person solders it.

On all other Motherboard connectors having the prefix XA, replacement begins with completely masking the connector with tape and then carefully breaking the connector apart (without pulling it) until only contacts remain. The use of paper and masking tape to isolate the area being worked on will help eliminate foreign materials from entering other areas of the 8340A.

WARNING

Whenever soldering or unsoldering and when breaking out bad connectors, always wear safety glasses to protect the eyes.

Using the two-person method previously described, unsolder and remove individual connector contacts; then reheat each pad and remove the old solder. Insert the new connector and hold it straight and flush against the Motherboard while another person solders all connector pins.

Single and dual in-line connectors having the prefix "J" (with the exception of J31) may be successfully removed by heating each connector pin and using a solder removing tool to remove the old solder. If necessary, resolder the connection and try removing the solder again to remove all adhering solder; do not use excessive heat.

To replace type SMC push-on coaxial connectors, heat the body from the component side of the board and remove it when the heat is sufficient. The center conductor will remain on the board. Unsolder the center conductor, then reheat each pad and remove the old solder. Solder the new connector from the non-component side of the board while another person holds it straight and flush against the Motherboard from the other side. Connector A62J1 may be replaced in the same manner as used in replacing other single and dual in-line "J" prefix package connectors (with the exception of J31).

Motherboard Replacement

The 8340A A62 Motherboard is not customer replaceable. Any

questions concerning Motherboard replacement should be directed to your nearest HP Sales and Service Center for more specific instructions. Refer to the HP Sales And Service Offices listing at the end of the Service section in this manual.

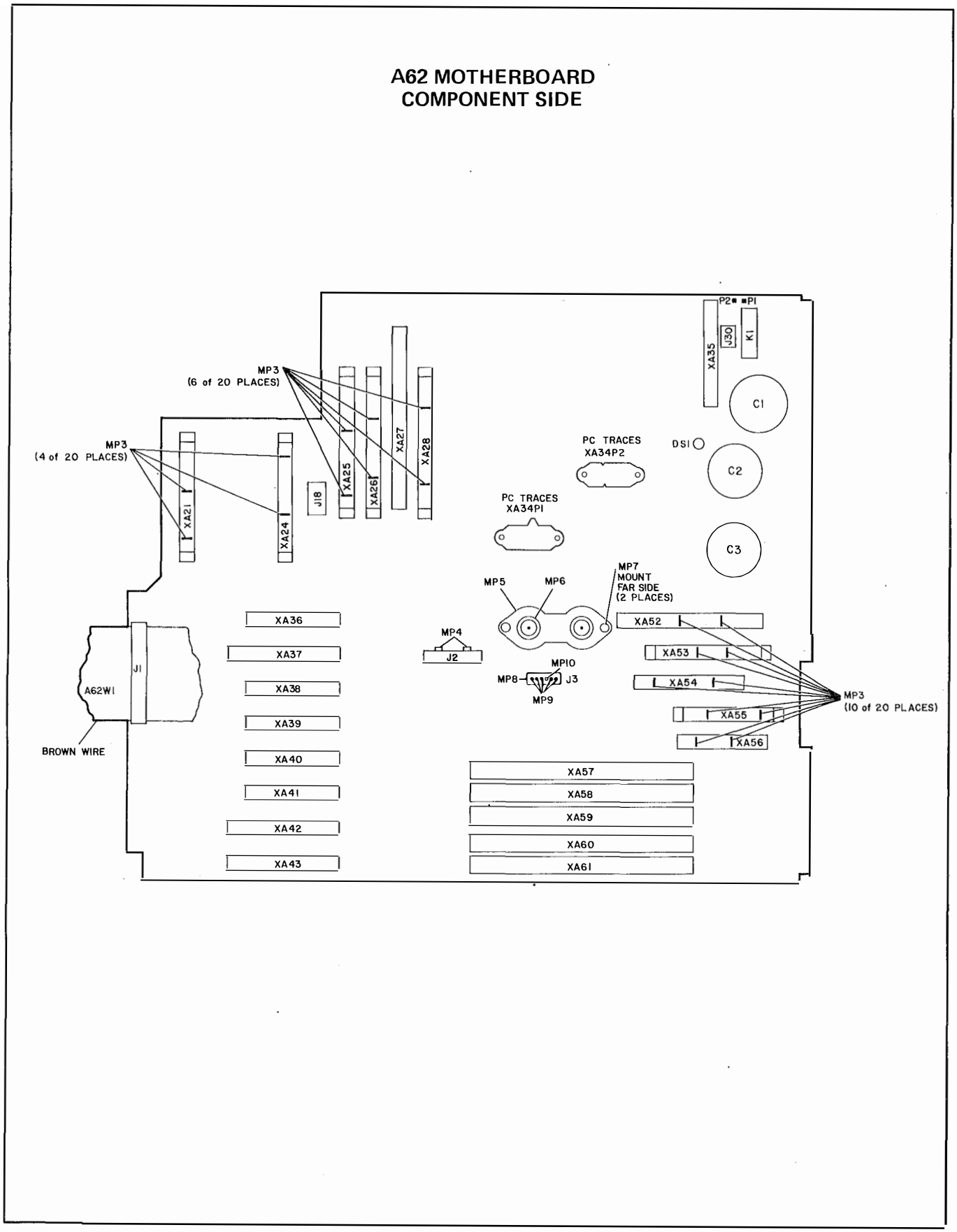


Figure 8E-2. A62 Motherboard Component Location Diagram (1 of 2)

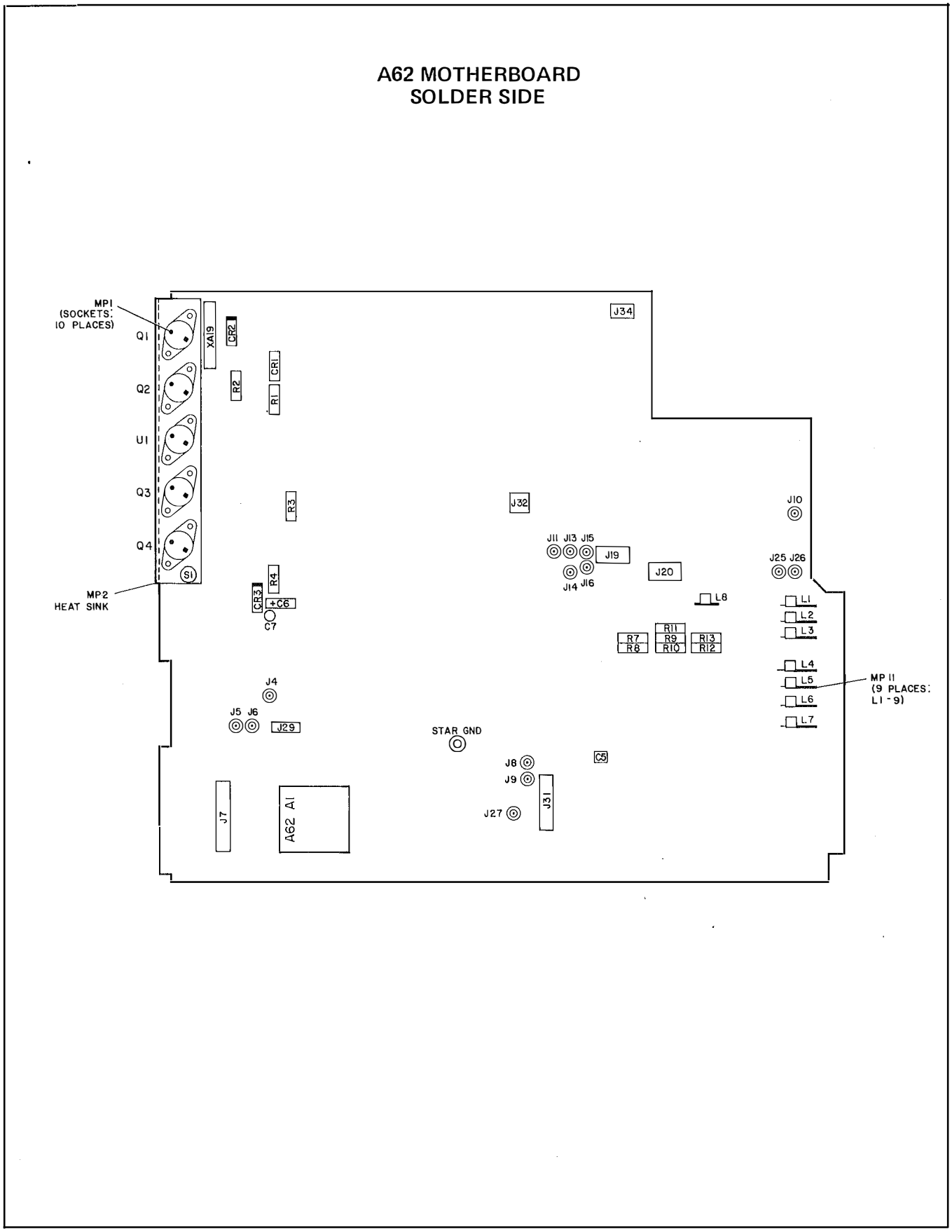


Figure 8E-2. A62 Motherboard Component Location Diagram (2 of 2)

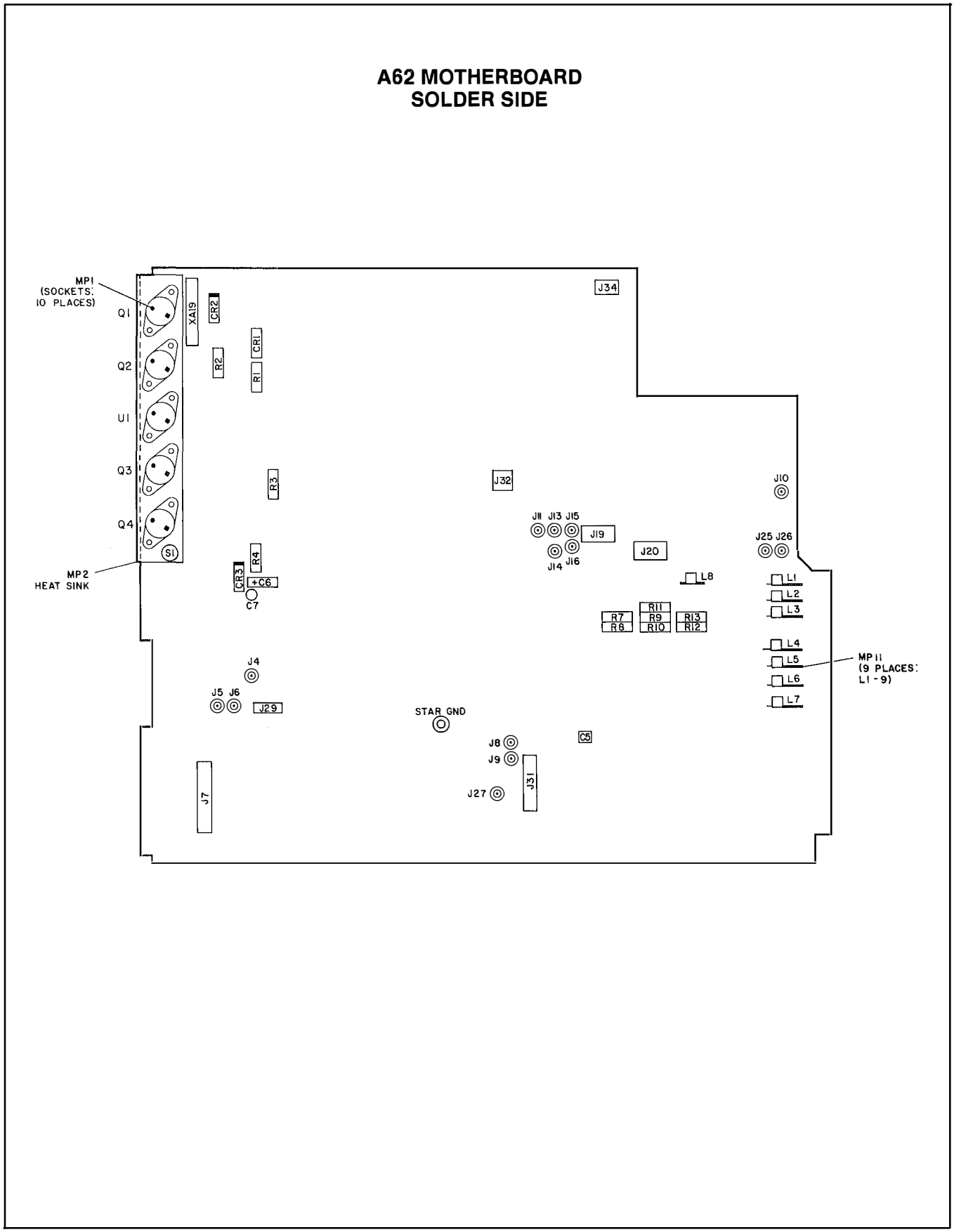


Figure 8E-2. A62 Motherboard Component Location Diagram (2 of 2)

MNEMONIC	DESCRIPTION	TYPE	LEVELS	SOURCE	REF M/N LOOP XR34P1	REF M/N LOOP XR34P2	20/30 LOOP XR35P1	20/30 LOOP XR37P1	20/30 LOOP XR38P1	20/30 LOOP XR39P1	20/30 LOOP XR40P1	20/30 LOOP XR41P1	20/30 LOOP XR42P1	20/30 LOOP XR43P1	SWEEP GENERATOR Y/O LOOP XR54P1	SWEEP GENERATOR Y/O LOOP XR55P1	SWEEP GENERATOR Y/O LOOP XR56P1	CONTROLLER XR57P1	CONTROLLER XR59P1	CONTROLLER XR60P1	CONTROLLER XR61P1	RF SECTION XR21P1	RF SECTION XR22P1 NOTE B	RF SECTION XR23P1 NOTE B	RF SECTION XR24P1	RF SECTION XR25P1	RF SECTION XR26P1	RF SECTION XR27P1	RF SECTION XR28P1	POWER SUPPLIES XR19P1	POWER SUPPLIES XR35P1	POWER SUPPLIES XR52P1	POWER SUPPLIES XR53P1	POWER SUPPLIES XR56P1	MISCELLANEOUS A62 MOTHERBOARD CONNECTORS	TI WIRE COLORS	A62 MOTHERBOARD CORK CONNECTORS J4-J6 J8-J17, J21-J28	A62 MOTHERBOARD COMPONENTS	GROUNDS AND GROUND PLANES	MNEMONICS
ADR0 ADR1 ADR2 ADR3 ADR4	INSTRUMENT I/O ADDRESS BUS BIT 0 INSTRUMENT I/O ADDRESS BUS BIT 1 INSTRUMENT I/O ADDRESS BUS BIT 2 INSTRUMENT I/O ADDRESS BUS BIT 3 INSTRUMENT I/O ADDRESS BUS BIT 4	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL TTL TTL TTL TTL	XA60P1-17 XA60P1-73 XA60P1-18 XA60P1-74 XA60P1-19													17 73 18 74 19	17 73 18 74 19	17 73 18 74 19	17 73 18 74 19							9 40 10 41 11							A62J1 PIN 23 A62J1 PIN 24 A62J1 PIN 25 A62J1 PIN 26 A62J1 PIN 27					ADR0 ADR1 ADR2 ADR3 ADR4
AM IN AM RTN	AMPLITUDE MODULATION INPUT AMPLITUDE MODULATION GROUND RETURN	ANALOG GROUND	±1V MAX. 0V	A62J15 CENTER A62J15 SHIELD: NOTE 10																						19 41								A62J15 - SMC CENTER A62J15 - SMC SHIELD AND GUARD TRACE AROUND AM IN				AM IN AM RTN
ATN ATNAT1 ATNAT2 ATNAT3 ATNAT4	IEEE 488 ATTENTION (ATN) ATTENUATOR ATTENUATION CARD 1 ATTENUATOR ATTENUATION CARD 2 ATTENUATOR ATTENUATION CARD 3 ATTENUATOR ATTENUATION CARD 4	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL OPEN COLLECTOR OPEN COLLECTOR OPEN COLLECTOR OPEN COLLECTOR	**XA60P1-8** **XA24P1-30** **XA24P1-29** **XA24P1-28** **XA24P1-27**														8	8						30 29 28 27							A62J7 PIN 21 A62J20 PIN 2 A62J20 PIN 9 A62J20 PIN 5 A62J20 PIN 10					ATN ATNAT1 ATNAT2 ATNAT3 ATNAT4
ATN COIL+	ATTENUATOR SOLENOID COILS SUPPLY	POWER SUPPLY	+5V	XA24P1-7																					7								A62J20 PIN 6				ATN COIL+
ATNTH1 ATNTH2 ATNTH3 ATNTH4	ATTENUATOR THROUGH CARD 1 ATTENUATOR THROUGH CARD 2 ATTENUATOR THROUGH CARD 3 ATTENUATOR THROUGH CARD 4	DIGITAL DIGITAL DIGITAL DIGITAL	OPEN COLLECTOR OPEN COLLECTOR OPEN COLLECTOR OPEN COLLECTOR	XA24P1-12 XA24P1-11 XA24P1-10 XA24P1-9																					12 11 10 9							A62J20 PIN 13 A62J20 PIN 3 A62J20 PIN 11 A62J20 PIN 4					ATNTH1 ATNTH2 ATNTH3 ATNTH4
BVSWP DAV	BUFFERED 0-10V SWEEP RAMP IEEE 488 DATA VALID (DAV)	ANALOG DIGITAL	10V/SWEEP TTL	**XA58P1-40** **XA60P1-6**													40		6	6									31						A62J7 PIN 11				BVSWP DAV
D80 D81 D82 D83 D84 D85 D86 D87	INSTRUMENT I/O DATA BUS BIT 0 INSTRUMENT I/O DATA BUS BIT 1 INSTRUMENT I/O DATA BUS BIT 2 INSTRUMENT I/O DATA BUS BIT 3 INSTRUMENT I/O DATA BUS BIT 4 INSTRUMENT I/O DATA BUS BIT 5 INSTRUMENT I/O DATA BUS BIT 6 INSTRUMENT I/O DATA BUS BIT 7	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL TTL TTL TTL TTL TTL TTL TTL	XA60P1-20: NOTE 9 XA60P1-76: NOTE 9 XA60P1-21: NOTE 9 XA60P1-77: NOTE 9 XA60P1-22: NOTE 9 XA60P1-78: NOTE 9 XA60P1-23: NOTE 9 XA60P1-79: NOTE 9			1 19 2 20 3 21 4 22						21 3 22 4 23 5 24 6	21 3 22 4 23 5 24 6	10 76 21 77 22 78 23 79		20 76 21 77 22 78 23 79	20 76 21 77 22 78 23 79	20 76 21 77 22 78 23 79	20 76 21 77 22 78 23 79		10 11 12 13 14 15		9 27 10 28 11 29 12 30		15 37 16 38 17 39 40	22 53 23 54 24 55 25 56	11 34 12 35 13 36 14 37						A62J1 PIN 3 A62J1 PIN 4 A62J1 PIN 5 A62J1 PIN 6 A62J1 PIN 7 A62J1 PIN 8 A62J1 PIN 9 A62J1 PIN 10				D80 D81 D82 D83 D84 D85 D86 D87
D88	INSTRUMENT I/O DATA BUS BIT 8	DIGITAL	TTL	XA60P1-24: NOTE 9			THRU R7 TO PIN 2	5					25	25	32		24	24	24	24		31		13			26	15					A62J1 PIN 11				D88
D89	INSTRUMENT I/O DATA BUS BIT 9	DIGITAL	TTL	XA60P1-80: NOTE 9			THRU R8 TO PIN 17	23					7	7	14		80	80	80	80				31	14		57	38					A62J1 PIN 12				D89
D810	INSTRUMENT I/O DATA BUS BIT 10	DIGITAL	TTL	XA60P1-25: NOTE 9			THRU R9 TO PIN 3	7					26	26	33		25	25	25	25				14	15		27	16					A62J1 PIN 13				D810
D811	INSTRUMENT I/O DATA BUS BIT 11	DIGITAL	TTL	XA60P1-81: NOTE 9			THRU R10 TO PIN 18	25					8	8	15		B1	B1	B1	B1		32			32		35	58					A62J1 PIN 14				D811
D812 D813 D814 D815	INSTRUMENT I/O DATA BUS BIT 12 INSTRUMENT I/O DATA BUS BIT 13 INSTRUMENT I/O DATA BUS BIT 14 INSTRUMENT I/O DATA BUS BIT 15	DIGITAL DIGITAL DIGITAL DIGITAL	TTL TTL TTL TTL	XA60P1-26: NOTE 9 XA60P1-82: NOTE 9 XA60P1-27: NOTE 9 XA60P1-83: NOTE 9											34 16 35 17		26 B2 27 B3	26 B2 27 B3	26 B2 27 B3	26 B2 27 B3					16 34							A62J1 PIN 15 A62J1 PIN 16 A62J1 PIN 17 A62J1 PIN 18				D812 D813 D814 D815
DETLVL DETOUT DET S/H+ DET S/H−	DETECTED LEVEL INPUT TO A/D C DETECTED LEVEL INPUT TO LINEAR MOD BOARD DETECTOR SAMPLE/HOLD CONTROL DETECTOR SAMPLE/HOLD CONTROL	ANALOG ANALOG DIGITAL DIGITAL	−0.2V/dB, 0V=0dB −.03V/dB, 0V=0dB +4.5V/+3.5V +3.5V/+4.5V	XA25P1-33 XA25P1-32 XA21P1-3 XA21P1-21																		3 21				33 32 2 24	10	29								DETLVL DETOUT DET S/H+ DET S/H−
DIV N2	500 KHZ DIVIDED OUTPUT FROM PLL2 DIVIDER	DIGITAL	TTL (LOW TRUE)	XA42P1-27								19	27																							DIV N2
DI01 DI02 DI03 DI04 DI05 DI06 DI07 DI08	IEEE 488 I/O DATA BUS BIT 1 IEEE 488 I/O DATA BUS BIT 2 IEEE 488 I/O DATA BUS BIT 3 IEEE 488 I/O DATA BUS BIT 4 IEEE 488 I/O DATA BUS BIT 5 IEEE 488 I/O DATA BUS BIT 6 IEEE 488 I/O DATA BUS BIT 7 IEEE 488 I/O DATA BUS BIT 8	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL TTL TTL TTL TTL TTL TTL TTL	**XA60P1-57** **XA60P1-58** **XA60P1-59** **XA60P1-60** **XA60P1-61** **XA60P1-62** **XA60P1-63** **XA60P1-64**														57 58 59 60 61 62 63 64	57 58 59 60 61 62 63 64													A62J7 PIN 1 A62J7 PIN 3 A62J7 PIN 5 A62J7 PIN 7 A62J7 PIN 2 A62J7 PIN 4 A62J7 PIN 6 A62J7 PIN 8				DI01 DI02 DI03 DI04 DI05 DI06 DI07 DI08
EOI EXDET EXDETR	IEEE 488 END OR IDENTIFY (EOI) EXTERNAL DETECTOR INPUT EXTERNAL DETECTOR INPUT GROUND RETURN	DIGITAL ANALOG GROUND	TTL 0.5MV-2V 0V	**XA60P1-7** **A62J16 CENTER** **A62J16 SHIELD: NOTE 10**															7	7						44 43							A62J9 PIN 9		A62J16 - SMC CENTER A62J16 - SMC SHIELD AND GUARD TRACE AROUND EXDET		EOI EXDET EXDETR

Refer to Table 8E-1. Motherboard Wiring List (7 of 7) for NOTES

MNEMONIC	DESCRIPTION	TYPE	LEVELS	SOURCE	REF M/N LOOP		20/30 LOOP									SWEEP GENERATOR Y/O LOOP			CONTROLLER					RF SECTION									POWER SUPPLIES					MISCELLANEOUS A62 MOTHERBOARD CONNECTORS	T1 WIRE COLORS	A62 MOTHERBOARD CORX CONNECTORS J4-J6 J8-J17, J21-J28	A62 MOTHERBOARD COMPONENTS	GROUNDS AND GROUND PLANES	MNEMONICS
					XR34P1	XR34P2	XR36P1	XR37P1	XR38P1	XR39P1	XR40P1	XR41P1	XR42P1	XR43P1	XR44P1	XR54P1	XR55P1	XR56P1	XR57P1	XR58P1	XR60P1	XR61P1	XR21P1	XR22P1 NOTE 8	XR23P1 NOTE 8	XR24P1	XR25P1	XR26P1	XR27P1	XR28P1	XR19P1	XR33P1	XR52P1	XR53P1	XR56P1						
EXT TRIG	EXTERNAL TRIGGER INPUT	TTL/ANALOG	EXT SOURCE LVL	A62J31-4, 18													106																		A62J31 PINS 4, 18					EXT TRIG
FAN1 FAN2 FAN3 FAN4	SWITCHED FAN POWER SWITCHED FAN POWER PRIMARY FAN POWER PRIMARY FAN POWER	AC LINE AC LINE AC LINE AC LINE	110 VAC 110 VAC 110 VAC 110 VAC	A62K1-7 A62K1-10 A62 SQ PIN P2 A62 SQ PIN P1																															A62J30 PIN 3 A62J30 PIN 1			A62K1 PIN 7 A62K1 PIN 10 A62K1 PIN 5; A62P2 A62K1 PIN 14; A62P1		FAN1 FAN2 FAN3 FAN4
FPNLSWP FPNLSWP RTN	FRONT PANEL SWEEP RAMP FRONT PANEL SWEEP RAMP GROUND RETURN	ANALOG GROUND	10V/SWEEP 0V	XA57P1-43 XA57P1-99															43 99																			A62J9 - SMC CENTER A62J9 - SMC SHIELD AND GUARD TRACE AROUND FPNLSWP				FPNLSWP FPNLSWP RTN
GND	ANALOG GROUND	GROUND	0V	A62 STAR GND		10, 11	1, 5 - 8 10, 11, 14 16 - 19 - 22 26, 29	6, 9, 10 13 - 17 24 - 27 - 35	1 - 11 14 - 26 28, 30	2 - 11 13, 14 17 - 26 28, 29	2 - 6 10, 14, 17 21, 25, 29	1, 3, 6, 10 11, 14, 16 18, 21, 22 25, 26, 29	10, 17, 20 28, 35	11 - 14 17, 27, 29 35	5, 23	5, 6 20, 21							8, 26	5, 6 14, 23 24, 32	8, 26	8	9, 10 31	6, 28	6, 37	6, 28	10, 22	4, 22	19, 39 43	4 - 16 33 - 35	5, 20	A62J2 PINS 2, 19 A62J3 PINS 2, 4	WHT, WHT		A62C1 (−), A62C2 (−) THRU A62C5 TO −40V; A62C6 (−), A62C7 (−); A62D51 CATHODE; THRU A62R3 TO +5V UNREG; THRU A62R4 TO +12V UI ADJ	NOTES 2 THRU 5	GND
GNDHPIB	IEEE 488 GROUND	GROUND	0V	CONNECTED TO REAR PANEL																															A62J7 PINS 12, 14, 16, 18, 20, 22, 23, 24					GNDHPIB
GND PLANE	DIGITAL GROUND	GROUND	0V	INSTRUMENT GROUND													1,34 44 - 46 55,56,70 - 71,75,89 99,101 110	1, 29 - 31 34, 40, 55 56 70 - 72 75 84 - 86 89, 110	1 40 - 44 55, 56, 75 96, 97, 110	1 40 - 44 55, 56 70 - 72 75 96 - 100 110	1, 34 40 - 44 55, 66 70 - 72 75, 88 96 - 100 110				6, 24	26		7, 19 38, 50							A62J1 PINS 1, 21, 29, 38 THRU 41; A62J1 PINS 46, 48, 50; A62J19 PINS 1, 9; A62J20 PIN 1; A62J31 PIN 12, 36				GND NOTE 1	GND PLANE
HADCEN HCEN HENDKICK HFILYO HINT HIPMOD DRV HLWB	A.D.C. CONVERT ENABLE YO DELAY COMPENSATION ENABLE YO AND YTM KICK PULSE COMPLETE FILTER YO ENABLE INTERNAL/EXTERNAL LEVELING CONTROL HIGH BAND PULSE MODULATOR DRIVE ALC LOOP BAND WIDTH CONTROL	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL ANALOG DIGITAL	TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE) PIN DIODE CURRENT TTL (HIGH TRUE)	XA21P1-1 XA59P1-67 XA28P1-18 XA59P1-72 XA26P1-42 XA21P1-36 XA28P1-33												14	47, 72		67 72				1 28 36 6			31	42 11	42 33	8 18						A62J2 PIN 5		A62J25 - SMC CENTER			HADCEN HCEN HENDKICK HFILYO HINT HIPMOD DRV HLBW
HLB0 HLB1 HLB2	ENCODED BAND INFO BIT 0 ENCODED BAND INFO BIT 1 ENCODED BAND INFO BIT 2	DIGITAL DIGITAL DIGITAL	TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE)	XA27P1-46 XA27P1-16 XA27P1-47																						20 21 22		29 30 31	46 16 47	31 32 33									HLB0 HLB1 HLB2
HLEY	LOCK ENABLE FOR YO LOOP	DIGITAL	TTL (HIGH TRUE)	XA59P1-51															51																A62J2 PIN 3					HLEY
HLE2 HMRKR HMTR HNUP HOVC HPLSEN	LOCK ENABLE TO PLL2 MARKER ASSERTED EXTERNAL METER LEVELING CONTROL NEGATIVE POWER SUPPLIES UP SIGNAL INTERNAL 10 MHZ STANDARD TEMP ERROR PULSE MODULATION ENABLED	DIGITAL DIGITAL DIGITAL DIGITAL ANALOG DIGITAL	TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE) +3V — OVEN WARM TTL (HIGH TRUE)	XA59P1-53 XA57P1-2, 12 XA26P1-13 XA53P1-17; XA56P1-1, 16 A62J3-3 XA26P1-2							2	2	2				2, 12 10		53 85				20 9			36 3	43 13 2				44	17	1, 16	A62J3 PIN 3					HLE2 HMRKR HMTR HNUP HOVC HPLSEN
HPME HPUP HRFON HSP HSTD HSTM	PROGRAM ENABLE (USED FOR PROGRAMING) POSITIVE POWER SUPPLIES UP SIGNAL RF OUTPUT POWER ON SWEEP IN PROGRESS INTERNAL 10 MHZ STANDARD ENABLE START MEMORY FETCH CYCLE	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE)	SEE A61 CKT DESCRIPTION XA57P1-46 XA57P1-105 XA57P1-13 XA59P1-66 XA60P1-45												22	13	105 13	95 13 66	95 45	60 95 45				27			24 7		26			46 21		A62J1 PIN 22					HPME HPUP HRFON HSP HSTD HSTM
HULH HULM HULR HULY HUL1 HUL2	3.7 GHZ OSCILLATOR UNLOCKED M/N OSCILLATOR UNLOCKED REFERENCE OSCILLATOR UNLOCKED YO 2-7 GHZ OSCILLATOR UNLOCKED PLL1 OSCILLATOR UNLOCKED PLL2 OSCILLATOR UNLOCKED	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TREU) TTL (HIGH TRUE) TTL (HIGH TRUE)	A62J19-16 XA34P1-8 XA34P2-14 A62J2-16 XA37P1-26; XA39P1-1, 16 XA41P1-4	8	14		26		1, 16		4						49, 104	105 104 49 50 106 107															A63J19 PIN 16 A63J19 PIN 16					HULH HULM HULR HULY HUL1 HUL2
HXREF IFC	EXTERNAL REFERENCE ENABLE IEEE 488 INTERFACE CLEAR (IFC)	DIGITAL DIGITAL	TTL (HIGH TRUE) TTL (LOW TRUE)	A62J31-17 A62J7-17													108		98 3	3															A62J31 PIN 17 A62J7 PIN 17					HXREF IFC
LALTEN LALTSEL LATTN LBX LCHNG	ALTERNATE MODE ENABLED CURRENT INST. STATE (FORE/BACK GROUND) ATENUATOR INSTALLED SENSING BAND CROSS INSTRUMENT STATE CHANGED	DIGITAL DIGITAL DIGITAL DIGITAL DIG. OPEN COLL.	TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE)	XA57P1-60 XA57P1-59 A62J20-14 XA57, 58, 59 P1-69 NOTE 9													69 100	60 59 69	69 45								39 21							A62J31 PINS 9, 23 A62J31 PINS 10, 24 A62J20 PIN 14					LALTEN LALTSEL LATTN LBX LCHNG

Refer to Table 8E-1. Motherboard Wiring List (7 of 7) for NOTES

MNEMONIC	DESCRIPTION	TYPE	LEVELS	SOURCE	REF M/N LOOP		20/30 LOOP								SWEEP GENERATOR Y/O LOOP			CONTROLLER				RF SECTION									POWER SUPPLIES					MISCELLANEOUS A62 MOTHERBOARD CONNECTORS	T1 WIRE COLORS	A62 MOTHERBOARD CORK CONNECTORS J4-J6 J8-J17,J21-J28	A62 MOTHERBOARD COMPONENTS	GROUNDS AND GROUND PLANES	MNEMONICS
					XR34P1	XR34P2	XR36P1	XR37P1	XR38P1	XR39P1	XR40P1	XR41P1	XR42P1	XR43P1	XR54P1	XR55P1	XR56P1	XR57P1	XR58P1	XR60P1	XR61P1	XR21P1	XR22P1 NOTE 8	XR23P1 NOTE 8	XR24P1	XR25P1	XR26P1	XR27P1	XR28P1	XR19P1	XR35P1	XR52P1	XR53P1	XR56P1						
LCK1 LCK2 LCK3 LCK4	DATA STROBE TO PLL2 COUNTERS (0, R2:) DATE STROBE TO PLL2 DIR. DIVIDER (0, R0:) DATA STROBE TO PLL2 PRETUNE DAC (0, R1:) DATE STROBE TO PLL1 VCO GAIN SWITCH (0, R3:)	DIGITAL DIGITAL DIGITAL DIGITAL	TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE)	XA59P1-54 XA59P1-109 XA59P1-108 XA59P1-52			THRU R11 TO PIN 4	8				19 1	19				54 109 108 52																						LCK1 LCK2 LCK3 LCK4
LDETBW LHET LHIBND LHSOT LHSOT RTN	DETECTOR LOW BAND WIDTH CONTROL HETRODYNE BAND ENABLED FUNDAMENTAL OR MULTIPLED BAND ENABLED HEAT SINK OVER TEMPERATURE SENSOR HEAT SINK OVER-TEMP SENSOR BND RETURN	DIGITAL DIGITAL DIGITAL DIGITAL GROUND	TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) 0V	XA26P1-9 XA27P1-20 XA26P1-2 A62J31-26 A62J31-12																	29				39 37	9 14 23	20		12							A62J34 PIN 2 A62J19 PINS 7, 8 A62J19 PIN 15 A62J31 PIN 26 ~~A62J31 PIN 12~~				~~GND PLACE~~	LDETBW LHET LHIBND LHSOT ~~LHSOT RTN~~
LIDA0 LIDA1 LIDA2 LIDA3 LIDA4 LIDA5	PROCESSOR/MEMORY PRIVATE BUS BIT 0 PROCESSOR/MEMORY PRIVATE BUS BIT 1 PROCESSOR/MEMORY PRIVATE BUS BIT 2 PROCESSOR/MEMORY PRIVATE BUS BIT 3 PROCESSOR/MEMORY PRIVATE BUS BIT 4 PROCESSOR/MEMORY PRIVATE BUS BIT 5	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE)	XA60P1-54 XA60P1-109 XA60P1-53 XA60P1-108 XA60P1-52 XA60P1-107															54 109 53 108 52 107	54 109 53 108 52 107																			LIDA0 LIDA1 LIDA2 LIDA3 LIDA4 ~~LIDA5~~
LIDA6 LIDA7 LIDA8 LIDA9 LIDA10	PROCESSOR/MEMORY PRIVATE BUS BIT 6 PROCESSOR/MEMORY PRIVATE BUS BIT 7 PROCESSOR/MEMORY PRIVATE BUS BIT 8 PROCESSOR/MEMORY PRIVATE BUS BIT 9 PROCESSOR/MEMORY PRIVATE BUS BIT 10	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE)	XA60P1-51 XA60P1-106 XA60P1-50 XA60P1-105 XA60P1-49															51 106 50 105 49	51 106 50 105 49																			LIDA6 LIDA7 LIDA8 LIDA9 ~~LIDA10~~
LIDA11 LIDA12 LIDA13 LIDA14 LIDA15	PROCESSOR/MEMORY PRIVATE BUS BIT 11 PROCESSOR/MEMORY PRIVATE BUS BIT 12 PROCESSOR/MEMORY PRIVATE BUS BIT 13 PROCESSOR/MEMORY PRIVATE BUS BIT 14 PROCESSOR/MEMORY PRIVATE BUS BIT 15	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE)	XA60P1-104 XA60P1-48 XA60P1-103 XA60P1-47 XA60P1-102															104 48 103 47 102	104 48 103 47 102																			LIDA11 LIDA12 LIDA13 LIDA14 ~~LIDA15~~
LINE TRIG	LINE TRIGGER SENSING 5V SECONDARY	RECTIFIED AC	LINE FREQ 7-10V	A62-CR1 CATHODE/A62R1													57, 68																		A62CR1 CATHODE ~~THRU A62R1 TO PWR ON LED~~			LINE TRIG
LIPS LMNE LMODHLD LOMD LOPMOD DRV	INSTRUMENT — PRESET M/N OSCILLATOR LOCK ENABLED LINEAR MODULATOR SAMPLE/HOLD OVER-MODULATION DETECTED LOW BAND PULSE MODULATOR DRIVE	DIG. OPEN COLL. DIGITAL DIGITAL DIG. OPEN COLL. ANALOG	TTL (LOW TRUE) TTL (LOW TRUE) TTL TTL (LOW TRUE) CURRENT SOURCE	XA52P1-36/A62J1-19 XA59P1-86 XA21P1-2 XA25P1-8 XA21P1-16	2											14	14	14 86	14	14		2 16				1 8	48		36 45							A62J1 PIN 19 A62J10 SMC CENTER					LIPS LMNE LMODHLD LOMD ~~LOPMOD DRV~~
LRETRACE LRSP LSBY LSOB LSPLD	RETRACE RESET SWEEP CONTROL STANDBY CONTROL STAY OFF BUSS SIGNAL SWEEP L.E.D. CONTROL OFF/ON	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL (LOW TRUE) TTL (LOW TRUE) 0V TO +22V TTL (LOW TRUE) TTL	XA57P1-58 XA59P1-85 A62J1-20 XA60P1-46 XA58P1-67												85 67	58	85 46	46	46																A62J31 PINS 11, 25 A62J1 PIN 20 A62J1 PIN 44					LRETRACE LRSP LSBY LSOB ~~LSPLD~~
LSSP LSRQ LSTEPUP LSTP LUNLVL	STEP SWEEP SERVICE REQUEST STEP UP FOR EXTERNAL FOOT SWITCH PROCESSOR STOPPED INSTRUMENT U NLEVELED	DIG. OPEN COLL. DIG. OPEN COLL. DIGITAL DIGITAL DIG. OPEN COLL.	TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE)	XA57P1-107 NOTE 9 A62J31-14 XA59P1-65 XA26P1-36												54	107 54	89 65	89 65							36	52									A62J31 PINS 5, 19 A62J1 PIN 45 A62J1 PIN 28; A62J31 PIN 14 A62J1 PIN 43					LSSP LSRQ LSTEPUP LSTP ~~LUNLVL~~
LVLCOR LVLREF LVSX LWRT LYOKICK LYSP	LEVELING CORRECTION A.L.C. LEVEL REFERENCE DISABLE YO SWEEPS WRITE TO RAM Y.O. SWEEP	ANALOG ANALOG DIGITAL DIGITAL DIGITAL	1.25dB/v 0V=0dB .2V/dB 0V=0dBM TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE)	XA25P1-14 XA27P1-30 XA58P1-68 XA60P1-101 XA58P1-11											9 21	7	68	11	101	101					14 13	62 30	41										LVLCOR LVLREF LVSX LWRT LYOKICK LYSP
MAR15IN MAR15OUT	MEMORY ADDRESS BIT 15 (IN) MEMORY ADDRESS BIT 15 (OUT)	DIGITAL DIGITAL	TTL TTL	SEE A61 CKT DESCRIPTION SEE A61 CKT DESCRIPTION															9 64																		~~MAR15IN~~ MAR15OUT
MKR RMP	SWEEP RAMP TO MARKER BANDCROSS BOARD	ANALOG	0 TO 10V/SWEEP	XA58P1-66												96	96																					~~MKR RMP~~
MM CLK EN MM ENABLE MM HEAD REF MM REF MM RFON MM SER IN	MILLIMETER CLOCK ENABLE MILLIMETER ENABLE MILLIMETER HEAD DETECT MILLIMETER REFERENCE MILLIMETER RF ON MILLIMETER SERIAL INPUT			XA69P1-71 XA21P1-24 XA27P1-13 XA26P1-14 XA21P1-34 XA59P1-12														71 12				24 34				8	14	13								A62J31 PIN 17 A62J31 PIN 16 A62J31 PIN 34 A62J31 PIN 15 A62J31 PIN 36		A62J28 SMC CENTER			MM CLK EN MM ENABLE MM HEAD REF MM REF MM RFON MM SER IN
MM SER OUT MM UNLVL	MILLIMETER SERIAL OUTPUT MILLIMETER UNLEVELED			XA69P1-70 XA26P1-26														70								25								A62J31 PIN 18 A62J31 PIN 33					MM SER OUT MM UNLVL

Refer to Table 8E-1. Motherboard Wiring List (7 of 7) for NOTES

MNEMONIC	DESCRIPTION	TYPE	LEVELS	SOURCE	REF M/N LOOP		20/30 LOOP								SWEEP GENERATOR Y/O LOOP			CONTROLLER				RF SECTION									POWER SUPPLIES				MISCELLANEOUS A62 MOTHERBOARD CONNECTORS	T1 WIRE COLORS	A62 MOTHERBOARD CORX CONNECTORS J4-J6 J8-J17, J21-J28	A62 MOTHERBOARD COMPONENTS	GROUNDS AND GROUND PLANES	MNEMONICS
					XP34P1	XP34P2	XR36P1	XR37P1	XR38P1	XR39P1	XR40P1	XR41P1	XR42P1	XR43P1	XR54P1	XR55P1	XR56P1	XR57P1	XR59P1	XR60P1	XR61P1	XR21P1	XR22P1 NOTE 8	XR23P1 NOTE 8	XR24P1	XR25P1	XR26P1	XR27P1	XR28P1	XR19P1	XR35P1	XR52P1	XR53P1	XR56P1						
MOD RTN	ALC MODULATORS GROUND RETURN	GROUND	0V	XA26P1-21																						21									A62J13 - SMC SHIELD A62J14 - SMC SHIELD AND GUARD TRACE AROUND MODHI AND MODLO					MOD RTN
MODHI MODLO MODLVL	HIGH BAND MODULATOR DRIVE LOW BAND MODULATOR DRIVE MODULATOR LEVEL	ANALOG ANALOG ANALOG	CURRENT SOURCE CURRENT SOURCE 0 TO −3 LEVELED	XA26P1-20 XA26P1-22 XA26P1-32																						20 22 32	61								A62J13 - SMC CENTER A62J14 - SMC CENTER					MODHI MODLO MODLVL
MUTE	PLOTTER MUTE CONTROL	DIGITAL	TTL (HIGH TRUE)	XA57P1-61													61																		A62J31 PINS 8, 22					MUTE
M1 M2 M3 M4 M5	M NUMBER TO M/N OSCILLATOR BIT 1 M NUMBER TO M/N OSCILLATOR BIT 2 M NUMBER TO M/N OSCILLATOR BIT 3 M NUMBER TO M/N OSCILLATOR BIT 4 M NUMBER TO M/N OSCILLATOR BIT 5	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE) TTL (HIGH TRUE)	XA59P1-33 XA59P1-88 XA59P1-32 XA59P1-87 XA59P1-31	5 6 3 4 1													33 88 32 87 31																					M1 M2 M3 M4 M5
NDAC NEG BLANK NRFD	IEEE 488 NOT DATA ACCEPTED (NDAC) NEGATIVE BLANKING SIGNAL IEEE 488 NOT READY FOR DATA (NRFD)	DIGITAL DIGITAL DIGITAL	TTL 0, −5V TTL	XA60P1-4 XA57P1-41 XA60P1-5												41		4 5	4 5																A62J7 PIN 15 A62J31 PINS 1, 15 A62J7 PIN 13					NDAC NEG BLANK NRFD
N1 N2	N NUMBER TO M/N OSCILLATOR BIT 1 N NUMBER TO M/N OSCILLATOR BIT 2	DIGITAL DIGITAL	TTL TTL	XA59P1-48 XA59P1-103	15 14													48 103																					N1 N2
N2 TUNE N2 TUNE TRN	TUNING SIGNAL TO PLL2 VCO GROUND RETURN	ANALOG GROUND	0V TO +7V 0V	XA41P1-23 XA41P1-8								23 8		28 10																									N2 TUNE N2 TUNE TRN
N3 N4 N5 N6	N NUMBER TO M/N OSCILLATOR BIT 3 N NUMBER TO M/N OSCILLATOR BIT 4 N NUMBER TO M/N OSCILLATOR BIT 5 N NUMBER TO M/N OSCILLATOR BIT 6	DIGITAL DIGITAL DIGITAL DIGITAL	TTL TTL TTL TTL	XA59P1-47 XA59P1-102 XA59P1-46 XA59P1-101	13 12 11 10													47 102 46 101																					N3 N4 N5 N6
PEN LIFT PEN LIFT RTN	PLOTTER PEN LIFT PLOTTER PEN LIFT GROUND RETURN	OPEN COLLECT GROUND	CLAMP AT 56V 0V	XA57P1-108 XA57P1-109													108 109																		A62J31 PINS 6, 20 A62J31 PIN 21					PEN LIFT PEN LIFT RTN
PH1	PLL1 PHASE DETECTOR OUTPUT	ANALOG	0V TO +5V	A62R12			24	THRU R12 TO PIN 11																														PH1
PH2	PLL1 PHASE DETECTOR OUTPUT	ANALOG	0V TO +5V	A62R13			25	THRU R13 TO PIN 12																														PH2
PINBIAS PLS IN PLS IN RTN	SYTM P.I.N. DIODE BIAS EXTERNAL PULSE INPUT EXTERNAL PULSE GROUND RETURN	DIGITAL DIGITAL GROUND	−4V TO +12V TTL 0V	XA24P1-24 A62J26 CENTER NOTE 10																	18 17	24													A62J18 PIN 10		A62J26 - SMC CENTER A62J26 - SMC SHIELD AND GUARD TRACE AROUND PLS IN			PINBIAS PLS IN PLS IN RTN
PMOD RTN	PULSE MODULATOR DRIVE GROUND RETURN	GROUND	0V	XA21P1-35																	35														A62J10/25 - SMC SHIELD AND GUARD TRACE AROUND HIPMOD AND LOPMOD DRV					PMOD RTN
PRETUNE	YO PRETUNE	ANALOG	−2.5V/GC 0 = 2GC	XA54P1-24											24	8, 23												22 NOTE B							A62J5 - SMC CENTER					PRETUNE
PWR ON LED	+5 VAC 2 THROUGH CR1 AND R1 TO DS1	POWER SUPPLY	+.78V ANODE — ON	A62R1																																A62DS1 ANODE: THRU A62R1 TO LINE TRIG			PWR ON LED
Q1B Q1E	TRANSISTOR Q1 BASE TRANSISTOR Q1 EMITTER	ANALOG ANALOG		XA53-4 XA53-7, 8, 25, 26																											4 7, 8 25, 26							Q1B Q1E
Q2B Q2E Q3B Q3C Q3E Q4B	TRANSISTOR Q2 BASE TRANSISTOR Q2 EMITTER TRANSISTOR Q3 BASE TRANSISTOR Q3 COLLECTOR TRANSISTOR Q3 EMMITTER TRANSISTOR Q4 BASE	ANALOG ANALOG ANALOG ANALOG ANALOG ANALOG		XA53P1-21 XA53P1-1, 19 XA52-7 XA52-6, 30 XA52-8, 32 XA52-3, 27																											7 6, 30 8, 32 3, 27	21 1, 19						Q2B Q2E Q3B Q3C Q3E Q4B
Q4C	TRANSISTOR Q4 COLLECTOR	ANALOG		XA52-1, 2, 25, 28																											1, 2 25, 26							Q4C
Q4E	TRANSISTOR Q4 EMITTER	ANALOG		XA52-4, 5, 28, 29																											4, 5 28, 29							Q4E
REN RFSWP	IEEE 488 REMOTE ENABLE (REN) SWEEP RAMP TO R.F. OUTPUT SECTION	DIGITAL ANALOG	TTL (LOW TRUE) 10V/SWEEP	A62J7-10 XA57P1-42													42		2	2							17								A62J7 PIN 10					REN RFSWP

Refer to Table 8E-1. Motherboard Wiring List (7 of 7) for NOTES

MNEMONIC	DESCRIPTION	TYPE	LEVELS	SOURCE	REF M/N LOOP		20/30 LOOP								SWEEP GENERATOR Y/O LOOP			CONTROLLER				RF SECTION								POWER SUPPLIES					MISCELLANEOUS A62 MOTHERBOARD CONNECTORS	T1 WIRE COLORS	A62 MOTHERBOARD CORX CONNECTORS J4-J6 J8-J17, J21-J28	A62 MOTHERBOARD COMPONENTS	GROUNDS AND GROUND PLANES	MNEMONICS
					XR34P1	XR34P2	XR36P1	XR37P1	XR38P1	XR39P1	XR40P1	XR41P1	XR42P1	XR43P1	XR54P1	XR55P1	XR56P1	XR67P1	XR59P1	XR60P1	XR61P1	XR21P1	XR22P1 NOTE 8	XR23P1 NOTE 8	XR24P1	XR25P1	XR26P1	XR27P1	XR28P1	XR19P1	XR35P1	XR52P1	XR53P1	XR58P1						
RGND	REFERENCE GROUND	GROUND	0V	STAR GND POINT										20	7, 25	10, 11 25, 26	42,43,98	45, 46, 101							36	12, 34	11, 34	18, 28 49, 60	21, 43						A62J29 PIN 1; A62J32 PIN 1		A62J11 - SMC SHIELD AND GUARD TRACES AROUND PRETUNE. VSWP, YO TUNE, AND SYTMRES A62J23 - SMC SHIELD AND GROUND TRACES NEAR 20/30 SWP AND VSWP A62J4, J5, J6, J18 - SMC SHIELD AND STANDOFF FOR LUG NEAR A62J29			RGND
RPNLSWP RPNLSWP RTN	REAR PANEL SWEEP OUTPUT REAR PANEL SWEEP GROUND RETURN	ANALOG GROUND	10V/SWEEP 0V	XA57P1-44 XA57P1-100														14 100																		A62J8 - SMC CENTER A62J8 - SMC SHIELD AND GUARD TRACE AROUND RPNLSWP			RPNLSWP RPNLSWP RTN
RSTAT	READ STATUS I/O STROBE (15, R3:)	DIGITAL	TTL (LOW TRUE)	XA27P1-45																			32	23			45	10										RSTAT
SIOA SIOB SR FBK SR PWR	I/O STROBE (FIRST HALF ADDRESSES) I/O STROBE (SECOND HALF ADDRESSES) YO SENSE RESISTOR FEEDBACK YO SENSE RESISTOR POWER	DIGITAL DIGITAL ANALOG ANALOG	TTL (LOW TRUE) TTL (LOW TRUE) −5V TO −17V −5V TO −17V	XA60P1-15 XA60P1-16 XA55P1-12, 27 XA55P1-13, 28												12, 27 13, 28	15 16	15 16	15 16	15 16							42									A62J1 PIN 49 A62J1 PIN 47 A62J29 PIN 2 A62J29 PIN 3			SIOA SIOB SR FBK SR PWR
SRD BIAS SRD BIAS CONT SRQ STAT10	STEP RECOVERY DIODE BIAS STEP RECOVERY DIODE BIAS CONTROL IEEE 488 SERVICE REQUEST (SRQ) STATUS WORD INPUT BIT 10	ANALOG DIGITAL DIGITAL DIGITAL	−10V/2K TO +5V 0 TO −5 LEVELED TTL TTL (LOW TRUE)	XA24P1-25 XA26P1-18 A62J7-19 XA23P1-22															9	9				22	25 13 4		18									A62J18 PIN 2 A62J7 PIN 19			SRD BIAS SRD BIAS CONT SRQ STAT10
SW1 SW2	PLL1 15-30 MHZ ON/OFF CONTROL PLL1 .15 TO .3 MHZ/3-6 MHZ CONTROL	DIGITAL DIGITAL	TTL TTL	XA42P1-32 XA42P1-14			24 22				32 14				23																							SW1 SW2
SYTM COIL + SYTM COIL − SYTM GND SYTMDB SYTMDC SYTMHTR SYTMRES SYTMTHRM	POSITIVE INPUT TO SYTM COIL NEGATIVE INPUT TO SYTM COIL SYTM GROUND SYTM DRIVE TRANSISTOR BASE SYTM DRIVE TRANSISTOR COLLECTOR REGULATOR HEATER DRIVE TO SYTM SYTM CURRENT SENSE FEED BACK TEMP FEED BACK THERMISTOR IN SYTM	ANALOG ANALOG GROUND ANALOG ANALOG ANALOG ANALOG ANALOG	−40V TO −25V −40V 0V −22 TO −39 −6 TO −6V 0 TO +20V −9V LOW BND CW APPROX −5V	XA28P1-42 A62J18-12 A62J18-13, 14, 15 XA28P1-19 XA28P1-20 XA24P1-19 XA28P1-44 A62J18-9																				35 19 2				42 5, 27 19 20 44									A62J18 PIN 4; A62J32 PIN 3 A62J18 PIN 12 A62J18 PINS 13 THRU 15; A62J32 PIN 2 A62J32 PIN 2 A62J32 PIN 4 A62J18 PIN 8 A62J32 PIN 5 A62J18 PIN 9			SYTM COIL+ SYTM COIL− SYTM GND SYTMDB SYTMDC SYTMHTR SYTMRES SYTMTHRM
TCREF THERM1 THERM2 TYOXP	ALC TEMP COMPENSATED REFERENCE LOW BAND DETECTOR THERMISTOR LOW BAND DETECTOR THERMISTOR TRIGGER YO KICK PULSE	ANALOG ANALOG ANALOG DIGITAL	−2V/dB 0V−0dBM −1V TO −8V −10V TTL (LOW TRUE)	XA25P1-35 A62J34-3 A62J34-1 XA59P1-100											18	30			100					35 4 26	12									A62J34 PIN 3 A62J34 PIN 1			TCREF THERM1 THERM2 TYOXP
VCOMP VSWP	YO DELAY COMPENSATION VOLTAGE YO SWEEP RAMP	ANALOG ANALOG	−26 MHZ/VOLT 0V TO 10V/SWEEP	XA58P1-27 XA58P1-97											27 26 NOTE 7	9	97																		A62J27 - SMC CENTER			VCOMP VSWP
WBAND WCDAC WLEVEL WMOD WPDAC WRDAC	BAND INFO I/O STROBE (10, R2:) DELAY COMPENSATION DAC DATA STROBE (5, R3:) ALC REFERENCE DAC DATA STROBE (10, R1:) MODULATION DAC DATA STROBE (10, R0:) PRE-TUNE DAC DATA STROBE (3, R2:) RESET DAC DATA STROBE (1, R2:)	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE)	XA27P1-43 XA59P1-30 XA27P1-12 XA27P1-59 XA59P1-68 XA59P1-29											28 36		30 28					33		33	33		44	43 12 59	29										WBAND WCDAC WLEVEL WMOD WPDAC WRDAC
WSPAT WSPTM WYOKW WYTMCTL WYTMSLP WT1R2	SWEEP ATTENUATOR DATA STROBE (1, R0:) SWEEP TIME DAC DATA STROBE (1, R1:) YO KICK PULSE WIDTH DATA STROBE (5, R1:) YTM CONTROL SIGNALS STROBE (11, R1:) YTM DRIVE SLOPE DAC DATA STROBE (11, R1:) EXTRA I/O STROBE (11, R2:)	DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL DIGITAL	TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE) TTL (LOW TRUE)	XA59P1-84 XA59P1-28 XA59P1-99 XA27P1-14 XA27P1-44 XA27P1-15											6		84 28		84 28 99									14 44 15	8 30										WSPAT WSPTM WYOKW WYTMCTL SYTMSLP WT1R2
YO COIL + YO COIL − YO TUNE YOXISTB	POSITIVE INPUT TO YO COIL NEGATIVE INPUT TO YO COIL LOW FREQ PHASE LOCK TO YO DRIVER YO DRIVE TRANSISTOR BASE	ANALOG POWER SUPPLY ANALOG ANALOG	−40V TO −20V −40V 0V ±8V −30V TO −39V	XA55P1-15, 30 A62J2-8, 13 XA55P1-24 XA55P1-29											15, 30 24 29											15									A62J2 PINS 6, 15; A62J29 PIN 5 A62J2 PINS 8, 13 A62J29 PIN 4		A62J6 - SMC CENTER			YO COIL + YO COIL − YO TUNE YOXISTB
Z-AXIS BLANK	Z-AXIS BLANKING/MARKER	DIGITAL	+5V/−5V	XA57P1-97														97																A62J31 PINS 2, 16					Z-AXIS BLANK
1.4V/GHZ 5 MHZ CLK 20/30 SWP 500 KHZ REF 8410 TRIG	1.4V PER GHZ REFERENCE 5 MHZ CLOCK TO HP/IB CHIP 20/30 MHZ REFERENCE OSCILLATOR SWEEP PLL2 500 KHZ REFERENCE SYNCRONIZING TRIGGER TO 8410B INTERFACE	ANALOG DIGITAL ANALOG DIGITAL DIGITAL	+1.4V/GHZ TTL 0V TO +10V TTL TTL	XA28P1-7 XA60P1-34 XA58P1-41 XA42P1-9 XA57P1-62							20	9	1			41	62	34	34					6			7								A62J31 PIN 7			1.4V/GHZ 5 MHZ CLK 20/30 SWP 500 KHZ REF 8410 TRIG

Refer to Table 8E-1. Motherboard Wiring List (7 of 7) for NOTES

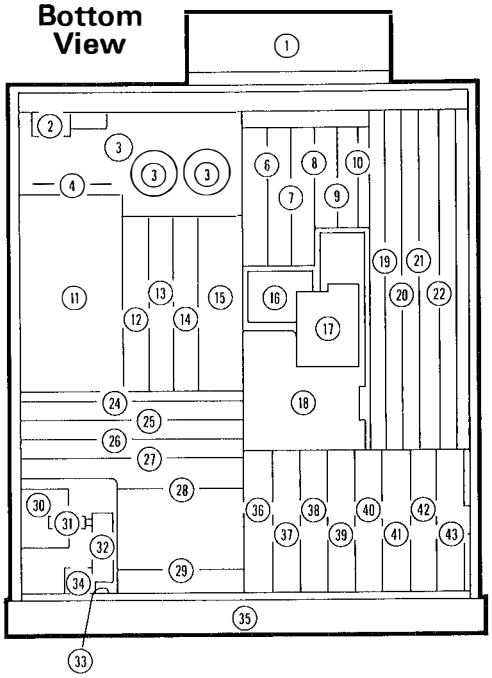
MNEMONIC	DESCRIPTION	TYPE	LEVELS	SOURCE	REF M/N LOOP		20/30 LOOP								SWEEP GENERATOR Y/O LOOP			CONTROLLER				RF SECTION								POWER SUPPLIES					MISCELLANEOUS A62 MOTHERBOARD CONNECTORS	T1 WIRE COLORS	A62 MOTHERBOARD CORX CONNECTORS J4-J6 J8-J17, J21-J28	A62 MOTHERBOARD COMPONENTS	GROUNDS AND GROUND PLANES	MNEMONICS
					XR34P1	XR34P2	XR36P1	XR37P1	XR38P1	XR39P1	XR40P1	XR41P1	XR42P1	XR43P1	XR54P1	XR55P1	XR56P1	XR57P1	XR58P1	XR60P1	XR61P1	XR21P1	XR22P1 NOTE 8	XR23P1 NOTE 8	XR24P1	XR25P1	XR26P1	XR27P1	XR28P1	XA19P1	XR33P1	XR52P1	XR53P1	XR56P1							
+1.0 V/GHZ +1.0 V/GHZ RTN +5V AC1	+1.0V/GHZ FREQUENCY REFERENCE +1.0V/GHZ FREQUENCY REFERENCE GROUND RETURN +5V TRANSFORMER SECONDARY	ANALOG GROUND T1 SEC.	1.0V/GHZ 0V 7 VAC	XA28P1-17 XA28P1-39 A62 LUG (6)																								17 39					A62J31 PIN 27, 32 A62J31 PIN 13					+1.0V/GHZ +1.0V/GHZ RTN +5V AC1
+5V AC2	+5V TRANSFORMER SECONDARY (GREEN)	T1 SEC.	7 VAC	A62 LUG (5)																									8 - 10 26 - 28 12 - 14 30 - 32				GRN GRN					+5V AC2
+5V SENSE (+) +5V SENSE (−) +5V UNREG	+5.2 VOLT SUPPLY POSITIVE SENSE +5.2 VOLT SUPPLY POSITIVE SENSE UNREGULATED SUPPLY TO +5V	POWER SUPPLY POWER SUPPLY POWER SUPPLY	+5.2V 0V +7V TO +9V	XA52P1-15 XA52P1-29 XA35P1-1, 2, 3, 19, 20, 21																									1 - 3 19 - 21	15 39 13, 14 37, 38				A62J1 PINS 31 THRU 37; A62J31 PIN 3		A62C2 (+); A62C3 (+); THRU A62R3 TO GND		NOTE 2	+5 SENSE (+) +5V SENSE (−) +5V UNREG
+5.2V	REGULATED +5.2 VOLT SUPPLY	POWER SUPPLY	+5.2V	XA52P1-17, 18, 41, 42		4, 5	THRU L1 TO 15, 30	THRU L3 TO 18, 36		THRU L7 TO 15, 30	15, 30	15, 30	18, 36	18, 36	2, 20	2, 17	36,37,92	36, 37, 92	36, 37, 92	36, 37, 92	36, 37, 92	5, 23	2, 20	3, 21	3	6, 28	4, 26	3, 34	2, 24						A62J2 PINS 4, 17; A62J19 PINS 3, 11					+5.2V
+12V +12V UNREG +12V U1 ADJ	REGULATED +12 VOLT SUPPLY UNREGULATED SUPPLY TO +12V +12V REGULATOR ADJUSTMENT TERMINAL	POWER SUPPLY POWER SUPPLY POWER SUPPLY	+12V +20V +10.5V	XA52P1-9, 33 XA52P1-11, 35 XA52P1-10			THRU L2 TO 13, 28		THRU L5 TO 13, 28								91	91	91	91	91			2, 20							9, 33 11, 35 10			A62J1 PIN 2			A62CR3 CATHODE; A62U1 CASE A62C7 (+); A62U1 PIN 1 C6 (+); CR3 ANODE: U1 PIN 2; THRU A62R4 TO GND		+12V +12V UNREG +12V U1 ADJ
+20V	REGULATED +20 VOLT SUPPLY	POWER SUPPLY	+20V	XA52P1-16, 40		2, 3				13, 28	13, 28	16, 34	16, 34		1, 19	1, 16	35, 90	35, 90	35, 90	35, 90	35	4, 22	1, 19	1, 19	1	5, 27	3, 26	2, 33	1, 23			16, 40	29		A62J2 PINS 9, 12; A62J18 PIN 6; A62J19 PINS 2, 10					+20V
+20V AC1 +20V AC2 +20V REF OSC +20V UNREG	TRANSFORMER SECONDARY FOR +20V SUPPLY TRANSFORMER SECONDARY FOR +20V SUPPLY SWITCHED +20V SUPPLY TO 10 MHZ REF. UNREGULATED SUPPLY TO +20V	POWER SUPPLY POWER SUPPLY POWER SUPPLY POWER SUPPLY	26.4 VAC 26.4 VAC 0V/+20V +31.2V	A62 LUG (7) A62 LUG (2) XA52P1-20 XA35P1-7, 25																									1, 13 2, 14 9, 21	7, 25	20 23, 24 47, 48		RED RED	A62J3 PIN 1					+20V AC1 +20V AC2 +20V REF OSC +20V UNREG
+21 VPP +22V −25 V/GHZ −5.2V −7V REF −10V	PROGRAMMING SUPPLY REGULATED +22 VOLT SUPPLY −25 VOLTS/GHZ OUTPUT FREQUENCY REGULATED −5.2 VOLT SUPPLY −7V REFERENCE SUPPLY REGULATED −10 VOLT SUPPLY	POWER SUPPLY POWER SUPPLY POWER SUPPLY POWER SUPPLY POWER SUPPLY POWER SUPPLY	+6V/+21V 22V −25V/GHZ −5.2V −7V −10V	SEE A61 CKT DESCRIPTION XA35P1-18, 36 XA28P1-40 XA53P1-18, 36 XA43P1-9 XA53P1-12, 13, 31, 32		12, 13 8, 9	THRU L8 TO 12, 27		THRU L4 TO 12, 27	THRU L6 TO 12, 27	12, 27 7 12, 27	15, 33	9 15, 33		4, 22	4, 19	39, 94	93 39, 94	93 39, 94	93 39, 94	3, 58 90 93 39, 94	7, 25	4, 22	4 5, 23	5	38 7, 29	5, 27	51 1, 32 4, 35	40 3, 25		18, 36	22	18, 36 12, 13 31, 32	4, 19	A62J1 PIN 30; A62J3 PIN 5 A62J19 PIN 14 A62J1 PIN 42; A62J2 PINS 1, 20; A62J19 PINS 4, 12 A62J2 PINS 10, 11; A62J18 PIN 7; A62J19 PINS 5, 13			A62CR2 CATHODE: A62K1 PIN 2		+21 VPP +22V −25V/GHZ −5.2V −7V REF −10V
−10V AC1	TRANSFORMER SECONDARY FOR −10V SUPPLY	POWER SUPPLY	13.9 VAC	A62 LUG (6)																									3, 4 15, 16				8LU					−10V AC1
−10V AC2	TRANSFORMER SECONDARY FOR −10V SUPPLY	POWER SUPPLY	13.9 VAC	A62 LUG (6)																									5, 6 17, 18				8LU					−10V AC2
−10V RETURN	−10V SUPPLY SERIES PASS COLLECTOR	POWER SUPPLY	+6.4V AT 13.3 GHZ	XA53P1-2, 20																									7, 8 19, 20		2, 20							−10V RETURN
−10V UNREG	UNREGULATED SUPPLY TO +10V	POWER SUPPLY	−10V	XA19P1-11, 12, 23, 24																									11, 12 23, 24		8, 10 27, 28							−10V UNREG
−15V −40V −40V AC1 −40V AC2	REGULATED −15V SUPPLY REGULATED −40V SUPPLY TRANSFORMER SECONDARY FOR −40V SUPPLY TRANSFORMER SECONDARY FOR −40V SUPPLY	POWER SUPPLY POWER SUPPLY POWER SUPPLY POWER SUPPLY	−15V −40V 42.8 VAC 42.8 VAC	XA56P1-15, 30 XA53P1-11, 30 A62 LUG (4) A62 LUG (4)		6, 7				11, 26				8 3	3, 18	38	38	38	38	38		3, 21	7, 25				5, 36	4 5, 27		15, 33 18, 34	15, 30 11, 30 3, 18		YEL YEL	A62J2 PINS 8, 13; A62J19 PIN 6			THRU A62C5 TO GND		−15V −40V −40V AC1 −40V AC2
−40V RETURN −40V SENSE (+) −40V SENSE (−) −40V UNREG	−40V SUPPLY SERIES PASS COLLECTOR −40V SUPPLY POSITIVE SENSE −40V SUPPLY NEGATIVE SENSE UNREGULATED SUPPLY TO −40V	POWER SUPPLY POWER SUPPLY POWER SUPPLY POWER SUPPLY	12.7V AT 13.3 GHZ 0V −40V −40V	XA53P1-3, 22 XA53P1-5 XA53P1-23 XA35P1-6, 24		6, 7				11, 26				3	3, 18							3, 21	7, 25					5, 27		5, 23 6, 24	3, 22 5 23 6, 24	3, 18		A62J2 PINS 8, 13; A62J19 PIN 6			C1 (+); THRU R2 TO −40V UNREG THRU A62C5 TO GND C1 (−); THRU R2 TO −40V RETURN	NOTE 2	−40V RETURN −40V SENSE (+) −40V SENSE (−) −40V UNREG
A62J12 CENTER A62J12 SHIELD A62J17 CENTER A62J17 SHIELD A62J21 CENTER A62J21 SHIELD	EXTRA SHIELDED CABLE CONNECTOR TO XA23 EXTRA SHIELDED CABLE CONNECTOR TO XA23 EXTRA SHIELDED CABLE CONNECTOR TO XA23 EXTRA SHIELDED CABLE CONNECTOR TO XA23 EXTRA SHIELDED CABLE CONNECTOR TO XA22 EXTRA SHIELDED CABLE CONNECTOR TO XA22			XA23P1-36 XA23P1-35 XA23P1-18 XA23P1-17 XA22P1-11 XA22P1-29																		11 29	36 35 18 17														A62J12 CENTER A62J12 SHIELD A62J17 CENTER A62J17 SHIELD A62J21 CENTER A62J21 SHIELD			A62J12 CENTER A62J12 SHIELD A62J17 CENTER A62J17 SHIELD A62J21 CENTER A62J21 SHIELD
A62J22 CENTER A62J22 SHIELD A62J23 CENTER A62J23 SHIELD A62J24 CENTER A62J24 SHIELD	EXTRA SHIELDED CABLE CONNECTOR TO XA22 EXTRA SHIELDED CABLE CONNECTOR TO XA22 EXTRA SHIELDED CABLE CONNECTOR TO XA22 EXTRA SHIELDED CABLE CONNECTOR TO XA22 EXTRA SHIELDED CABLE CONNECTOR TO XA22 EXTRA SHIELDED CABLE CONNECTOR TO XA22			XA22P1-10 XA22P1-28 XA22P1-9 XA22P1-27 XA22P1-16 XA22P1-34																		10 28 9 27	16 24														A62J22 CENTER A62J22 SHIELD A62J23 CENTER A62J23 SHIELD A62J24 CENTER A62J24 SHIELD			A62J22 CENTER A62J22 SHIELD A62J23 CENTER A62J23 SHIELD A62J24 CENTER A62J24 SHIELD

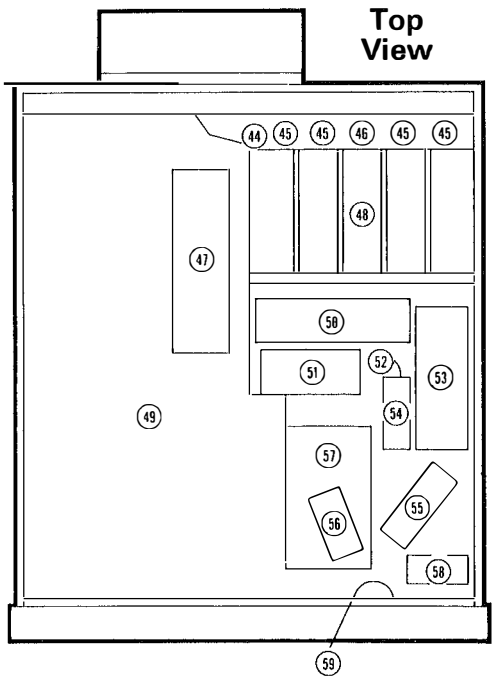
Refer to Table 8E-1. Motherboard Wiring List (7 of 7) for NOTES

NOTES

1. Gnd Plane is located near the RF Section.
2. M/N Assembly Ground Plane (connected to Star Gnd through W45).
3. 20/30 Loops Casting.
4. Star Gnd (Connected to M/N Assembly Ground Plane through W45; connected also to A47W3).
5. Gnd is connected to the HP 8340A chassis.
6. Pretune is routed to this pin from A62J5 through W48 to A62J11.
7. Vswp is routed to this pin from A62J27 through W47 to A62J4.
8. Reserved for future expansion.
9. Open collector bus — multiple sources.
10. Multiple sources.
11. The mnemonics in this table exist on the A62 Motherboard assembly. Other mnemonics contained only within other assemblies such as the YO Loop, M/N Loop and Front Panel assemblies are not shown; to locate these, refer to the Pin I/O Tables and Schematic Diagrams of those assemblies.

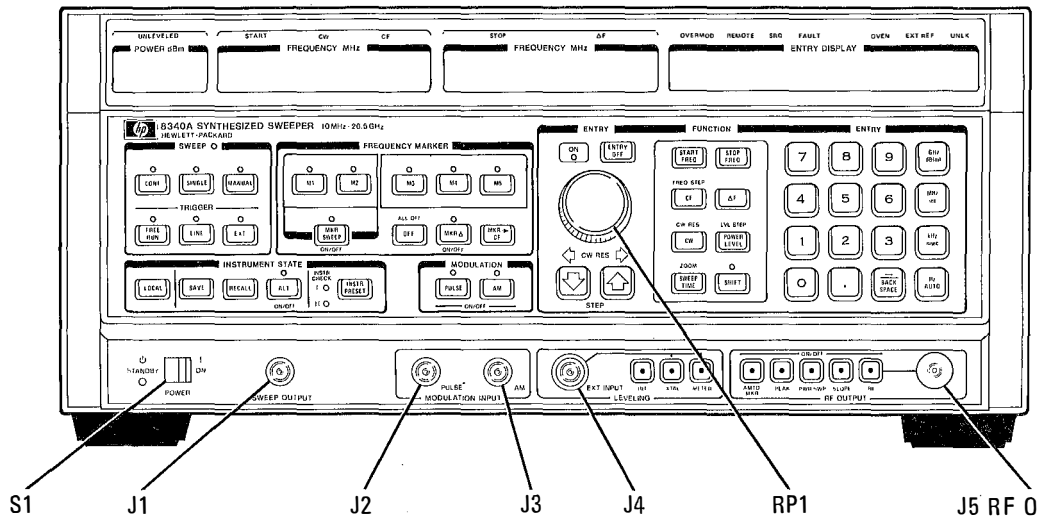
REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 3						Volume 4	
			Ref.-M/N Loops	20-30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	33					•			
A2	Display Driver	33					•			
A3	Display Processor	33					•			
A4	Not Assigned	-								
A5	Keyboard	35					•			
A6	Keyboard Interface	35					•			
A7	Lower Keyboard	35					•			
A8	3.7 GHz Oscillator	57						•		
A9	Band 0 Pulse Modulator	56						•		
A10	Directional Coupler	32						•		
A11	Band 1-4 Detector	31						•		
A12	Band 0 Splitter/Detector	34						•		
A13	SYTM (Switched YIG Tuned Multiplier)	30						•		
A14	Band 1-4 Power Amplifier	53						•		
A15	Band 0 Low Pass Filter	52						•		
A16	Band 1-4 Modulator/Splitter	51						•		
A17	Band 0 Mixer	54						•		
A18	Band 0 Power Amplifier	55						•		
		60						•		
A19	Capacitor Assembly	48								•
A20	RF Section Filter	50						•		
A21	Pulse Modulator Driver	29						•		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						•		
A25	ALC Detector	27						•		
A26	Linear Modulator	26						•		
A27	Level Control	25						•		
A28	SYTM Driver	24						•		
A29	Reference Phase Detector	12	•							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	•							
A31	M/N Phase Detector	14	•							
A32	M/N VCO (Voltage Controlled Osc.)	15	•							
A33	M/N Output	15	•							
A34	Reference-M/N Motherboard	5	•							
A35	Rectifier	4								•
A36	PLL1 VCO (Voltage Controlled Osc.)	36		•						
A37	PLL1 Divider	37		•						
A38	PLL1 IF	38		•						
A39	PLL3 Upconverter	39		•						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		•						
A41	PLL2 Phase Detector	41		•						
A42	PLL2 Divider	42		•						
A43	PLL2 Discriminator	43		•						
A44	YIG Oscillator (YO)	18			•					
A45	Directional Coupler	18			•					
A46	7 GHz Low Pass Filter	18			•					
A47	Sense Resistor Assembly (YO circuit)	47			•					
	(SYTM circuit)	47						•		
A48	YO Loop Sampler	18			•					
A49	YO Loop Phase/Detector	18			•					
A50	YO Loop Interconnect	17			•					
A51	Reference Oscillator	16	•							
A52	Positive Regulator	6								•
A53	Negative Regulator	7								•
A54	YO Pretune/Delay Compensation	8			•					
A55	YO Driver	9			•					
A56	−15V Regulator	10								•
A57	Marker/Bandcross	19				•				
A58	Sweep Generator	20			•					
A59	Digital Interface	21				•				
A60	Processor	22				•				
A61	Not Assigned	23				•				
A62	Motherboard	49					•			
A63	90 dB RF Attenuator	59						•		
AT1	Peripheral Mode Isolator	58						•		
AT2	15 dB Attenuator	18			•					
B1	Fan Assembly	1								•
A62C1-3	Power Supply Filter Capacitors	3								•
FL1	AC Line Module	2								•
A62Q1-4	Power Supply Regulating Transistors	45								•
A62S1	Power Supply Thermal Switch	44								•
T1	Power Supply Transformer	11								•
A62U1	Power Supply Regulator	46								•

FRONT PANEL



REAR PANEL

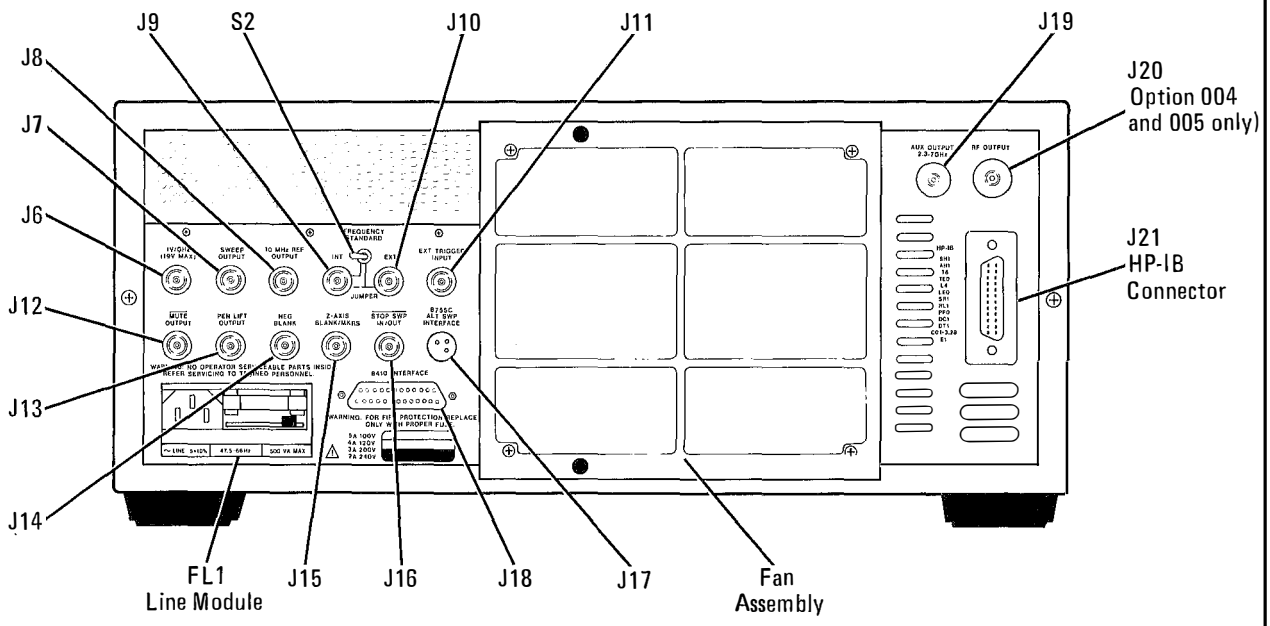


Figure 8F-1. Front and Rear Panels

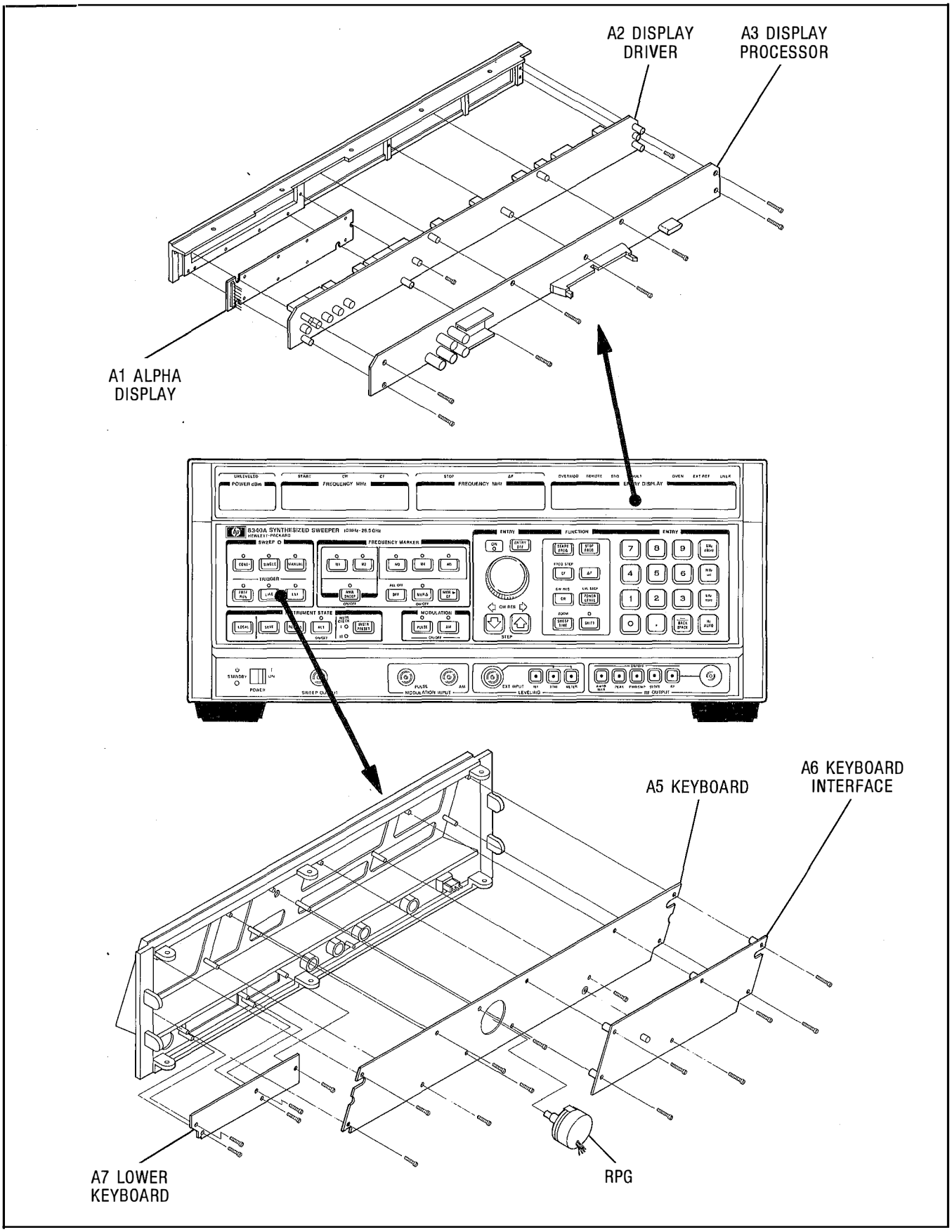


Figure 8F-2. Front Panel Assemblies

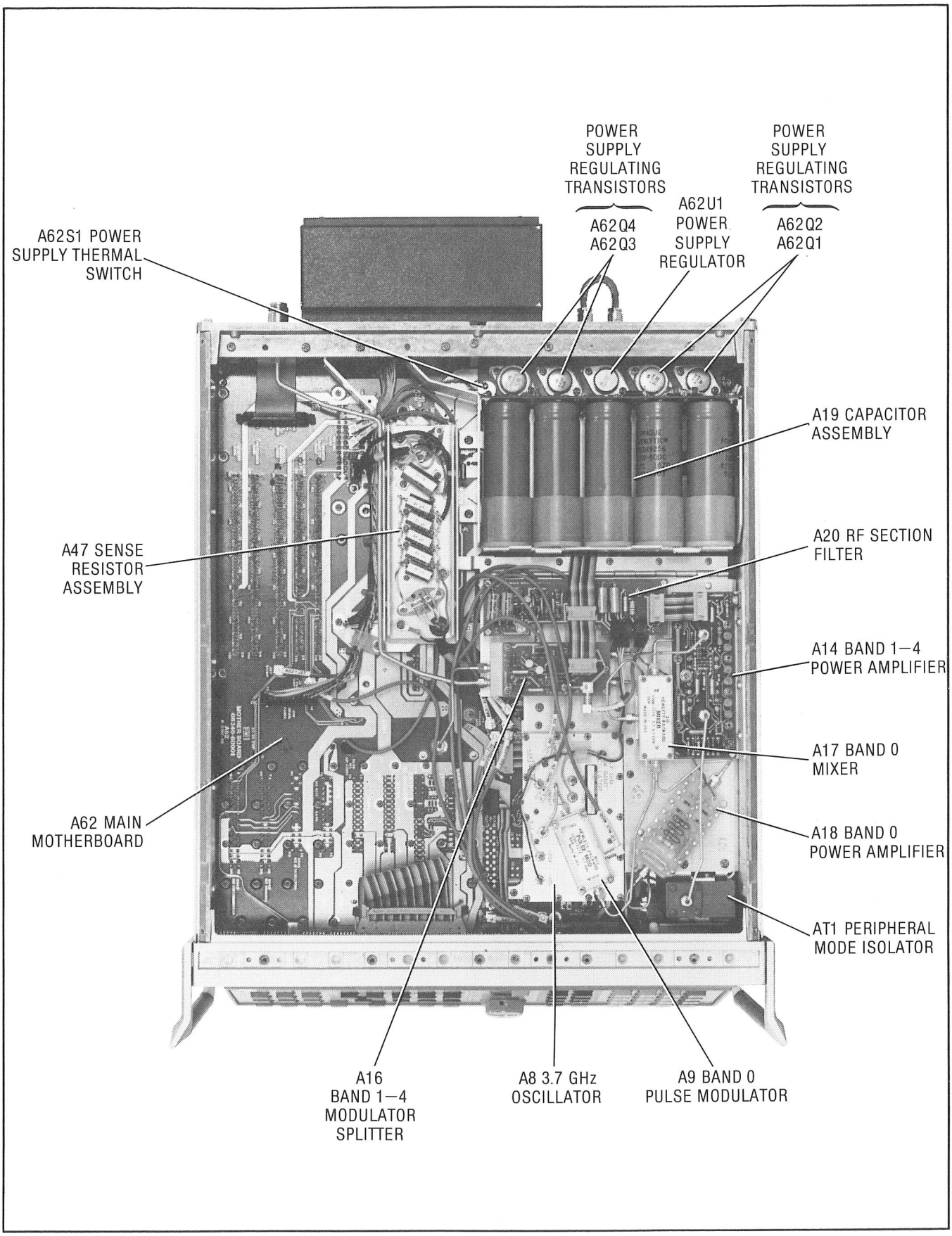


Figure 8F-3. 8340A - Top View (1 of 3)

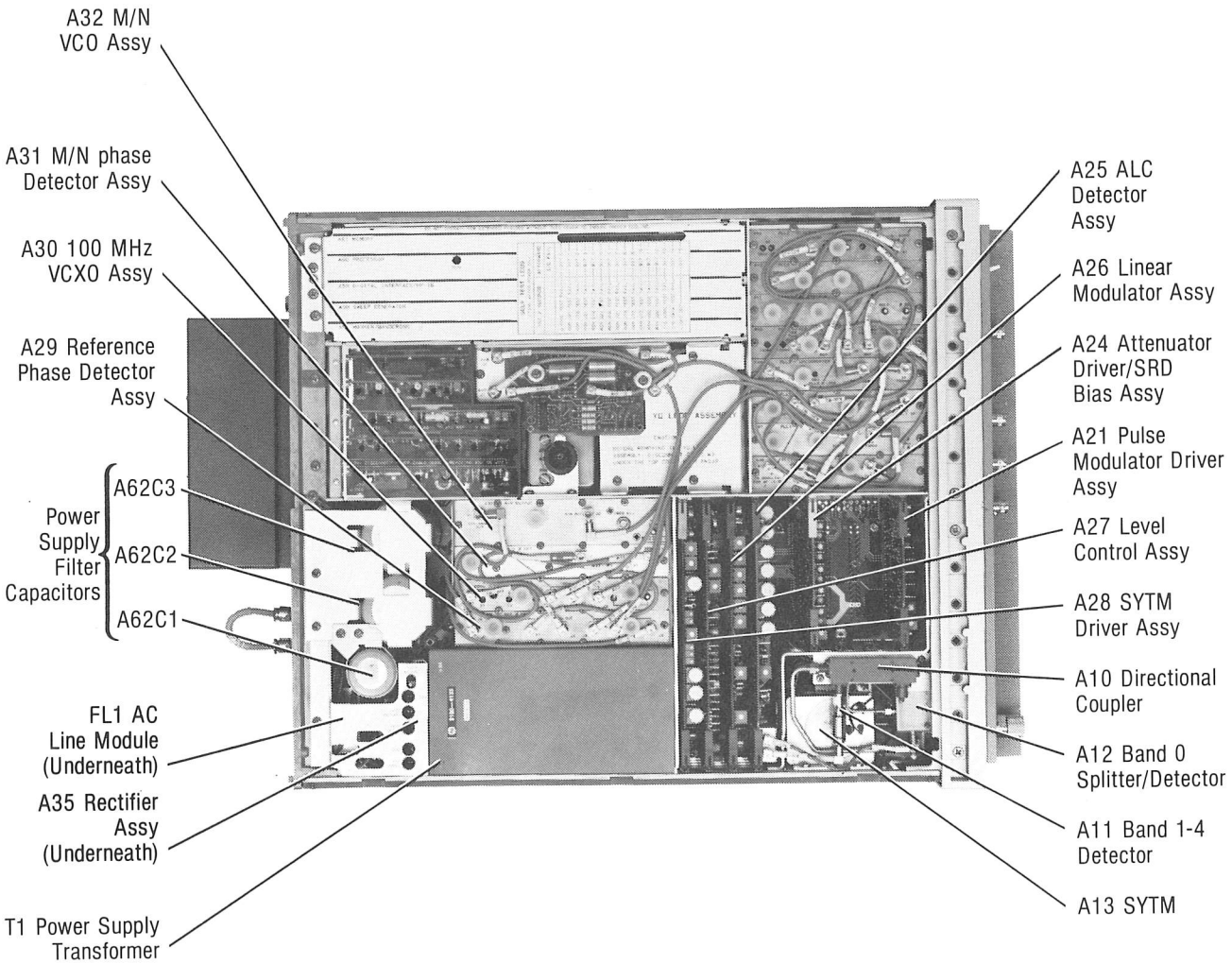


Figure 8F-3. 8340A - Bottom View (2 of 3)

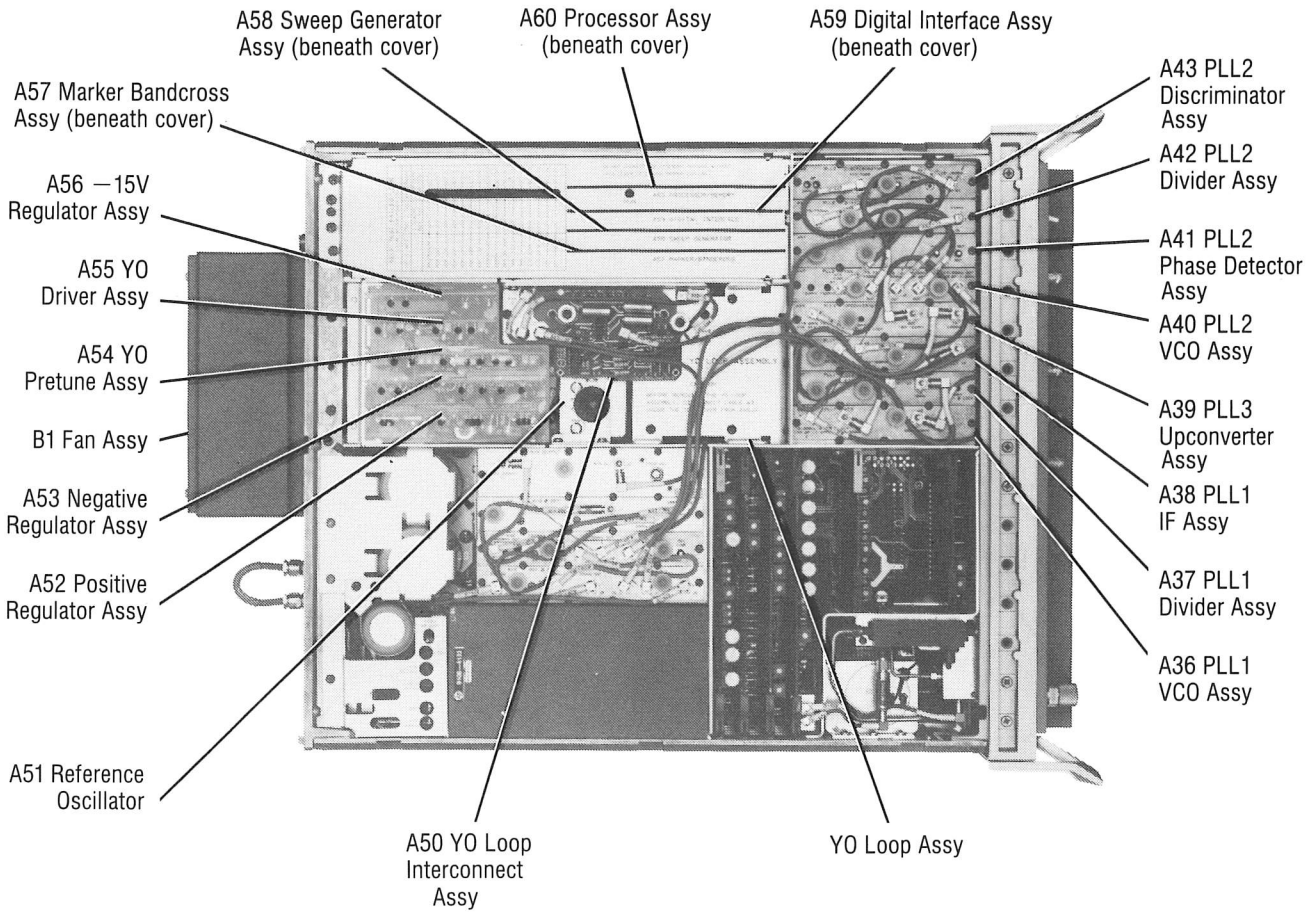
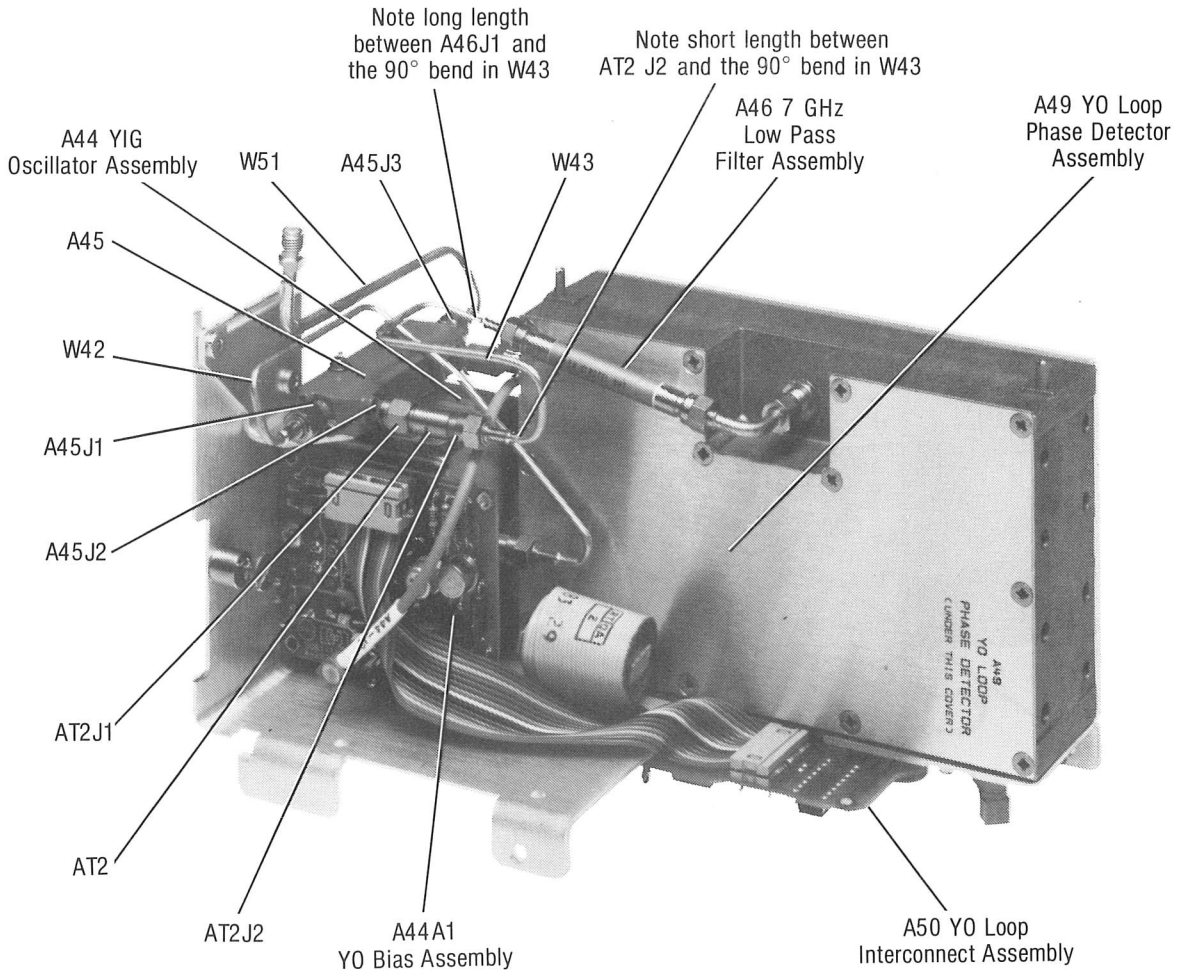


Figure 8F-3. 8340A - Bottom View (3 of 3)



CAUTION: W51 Must be disengaged from W3 before removing the YO Loop from the instrument or damage to these cables will result. Refer to Figure 8I-8, View C, in the RF Section (Volume 4).

Figure 8F-4. YO Loop Assembly (1 of 3)

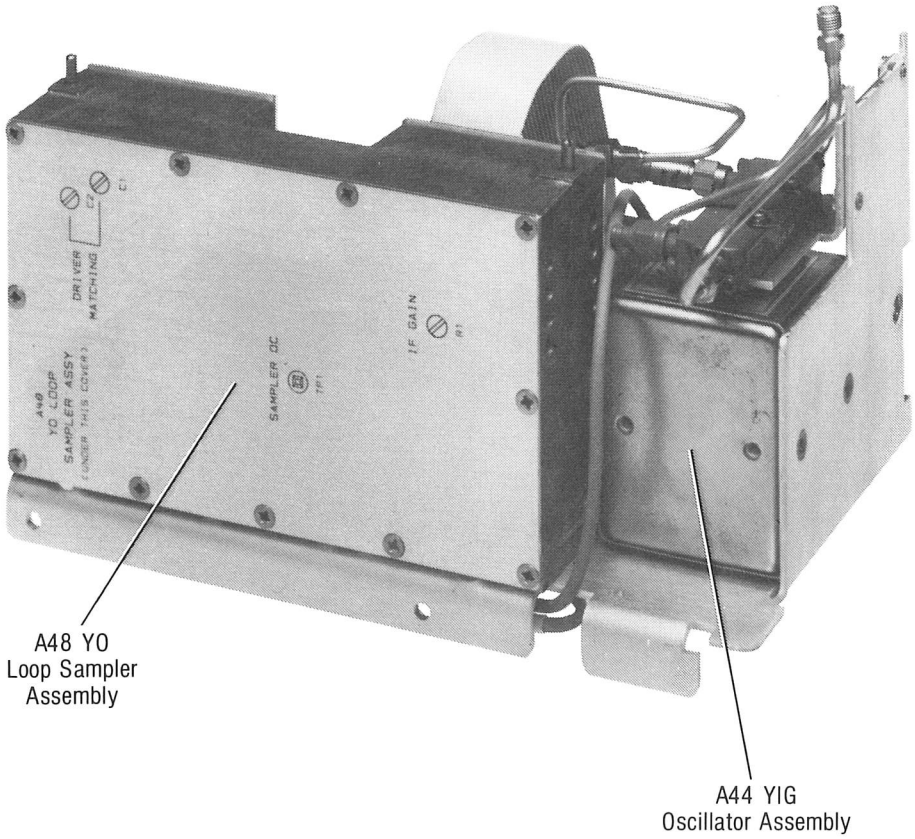


Figure 8F-4. YO Loop Assembly (2 of 3)

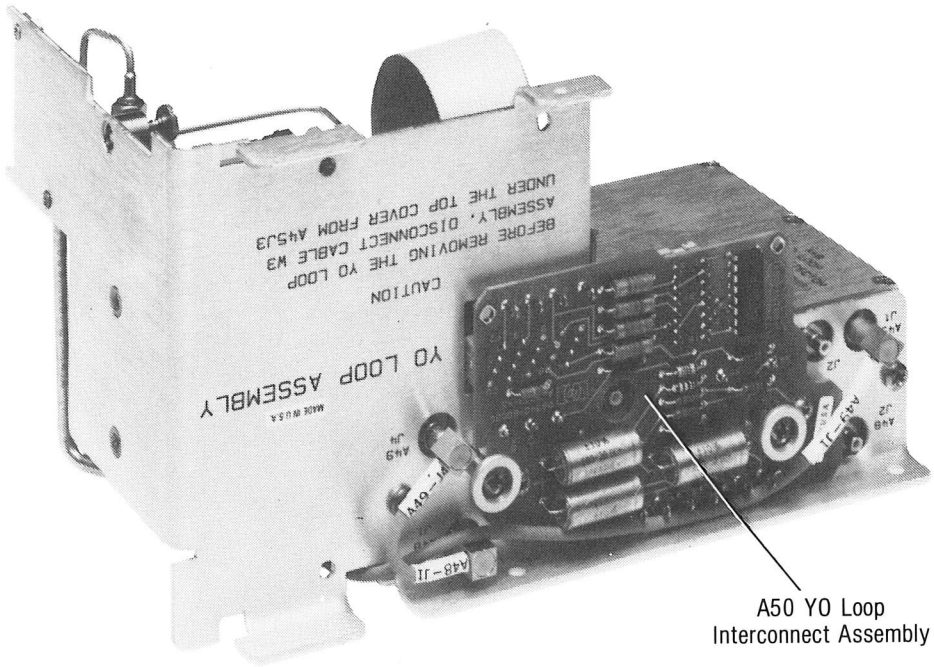


Figure 8F-4. YO Loop Assembly (3 of 3)

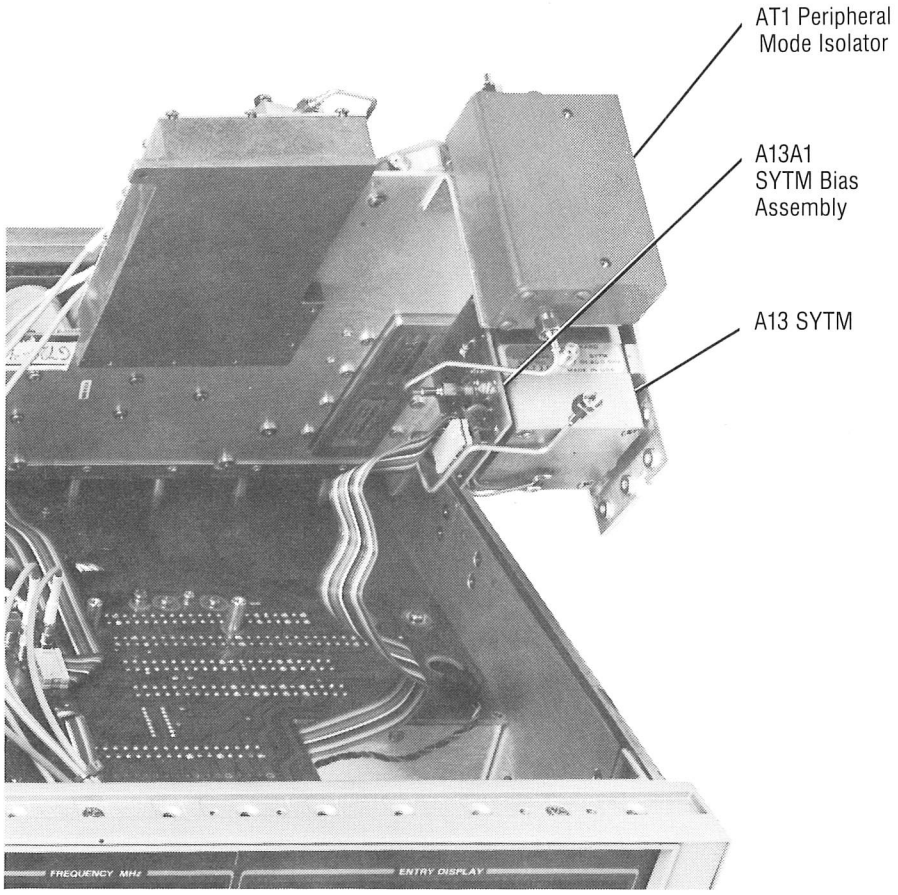


Figure 8F-5. RF Section Swung Out