SERVICE MANUAL

HP 8340A SYNTHESIZED SWEEPER

10 MHz to 26.5 GHz

HEWLETT PACKARD

VOLUME 4 TABLES

SAFETY CONSIDERATIONS

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation. This product has been designed and tested in accordance with international standards.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual (refer to Table of Contents).

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND

This is a Safety Class I product (provided with a protective earthing terminal). An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an autotransformer, make sure the common terminal is connected to the neutral (grounded) side of mains supply.

SERVICING

WARNING

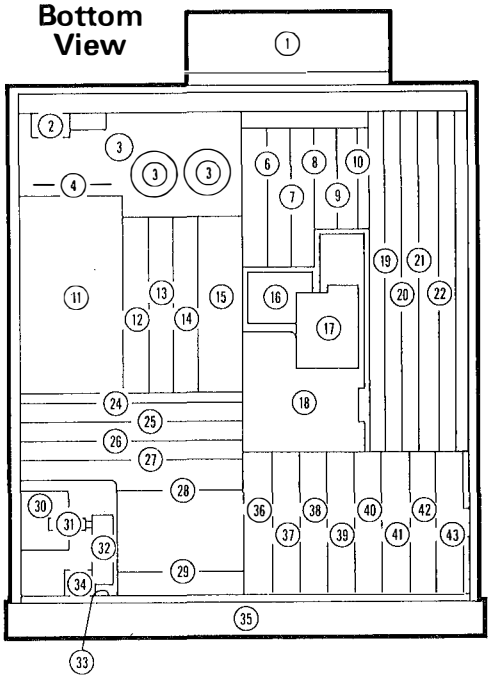
Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

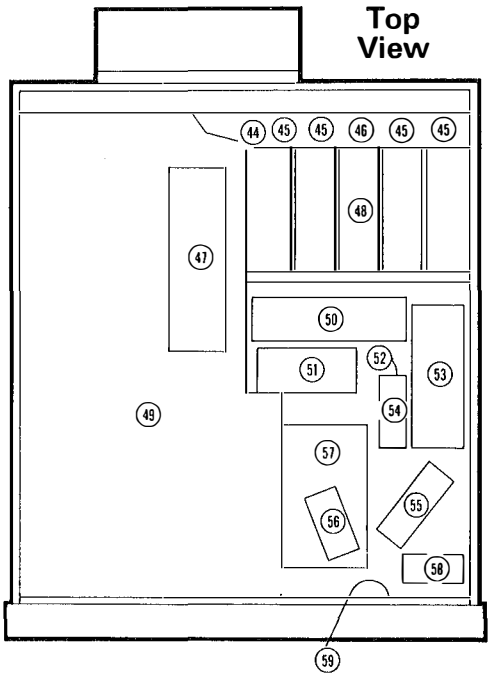
Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 3					Volume 4		
			Ref.-M/N Loops	20-30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	33					•			
A2	Display Driver	33					•			
A3	Display Processor	33					•			
A4	Not Assigned	-								
A5	Keyboard	35					•			
A6	Keyboard Interface	35					•			
A7	Lower Keyboard	35					•			
A8	3.7 GHz Oscillator	57						•		
A9	Band 0 Pulse Modulator	56						•		
A10	Directional Coupler	32						•		
A11	Band 1-4 Detector	31						•		
A12	Band 0 Splitter/Detector	34						•		
A13	SYTM (Switched YIG Tuned Multiplier)	30						•		
A14	Band 1-4 Power Amplifier	53						•		
A15	Band 0 Low Pass Filter	52						•		
A16	Band 1-4 Modulator/Splitter	51						•		
A17	Band 0 Mixer	54						•		
A18	Band 0 Power Amplifier	55						•		
		60						•		
A19	Capacitor Assembly	48								•
A20	RF Section Filter	50						•		
A21	Pulse Modulator Driver	29						•		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						•		
A25	ALC Detector	27						•		
A26	Linear Modulator	26						•		
A27	Level Control	25						•		
A28	SYTM Driver	24						•		
A29	Reference Phase Detector	12	•							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	•							
A31	M/N Phase Detector	14	•							
A32	M/N VCO (Voltage Controlled Osc.)	15	•							
A33	M/N Output	15	•							
A34	Reference-M/N Motherboard	5	•							
A35	Rectifier	4								•
A36	PLL1 VCO (Voltage Controlled Osc.)	36		•						
A37	PLL1 Divider	37		•						
A38	PLL1 IF	38		•						
A39	PLL3 Upconverter	39		•						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		•						
A41	PLL2 Phase Detector	41		•						
A42	PLL2 Divider	42		•						
A43	PLL2 Discriminator	43		•						
A44	YIG Oscillator (YO)	18			•					
A45	Directional Coupler	18			•					
A46	7 GHz Low Pass Filter	18			•					
A47	Sense Resistor Assembly (YO circuit)	47			•					
	(SYTM circuit)	47						•		
A48	YO Loop Sampler	18			•					
A49	YO Loop Phase/Detector	18			•					
A50	YO Loop Interconnect	17			•					
A51	Reference Oscillator	16	•							
A52	Positive Regulator	6								•
A53	Negative Regulator	7								•
A54	YO Pretune/Delay Compensation	8			•					
A55	YO Driver	9			•					
A56	−15V Regulator	10								•
A57	Marker/Bandcross	19					•			
A58	Sweep Generator	20			•					
A59	Digital Interface	21					•			
A60	Processor	22					•			
A61	Not Assigned	23					•			
A62	Motherboard	49				•				
A63	90 dB RF Attenuator	59						•		
AT1	Peripheral Mode Isolator	58						•		
AT2	15 dB Attenuator	18			•					
B1	Fan Assembly	1								•
A62C1-3	Power Supply Filter Capacitors	3								•
FL1	AC Line Module	2								•
A62Q1-4	Power Supply Regulating Transistors	45								•
A62S1	Power Supply Thermal Switch	44								•
T1	Power Supply Transformer	11								•
A62U1	Power Supply Regulator	46								•

CONTROLLER SECTION G

CONTROLLER
INTRODUCTION

The controller functional group consists of three assemblies:

A57 Marker/Bandcross board
A59 Digital Interface board
A60 Processor board

The following service information contains the theory of operation, schematic diagrams, component location diagrams, and troubleshooting information for all of these boards. A table of contents on the binder tab that precedes this section shows the organization of this information.

Several troubleshooting approaches are documented in this section, including:

Self Test
Direct addressing of I/O devices
by front panel key entries. (Direct I/O Addressing)
Checks of individual circuitry

The troubleshooting information in the A60 Processor board service section describes all of these procedures as they apply to the entire functional group, and this is where you should begin. The troubleshooting information in the service section of the other boards applies only to the individual boards.

The first troubleshooting test should always be the 8340A's self test that is run automatically either at power-on, or following an instrument preset.

The second troubleshooting step is to observe the 16 LEDs on the A60 Processor board. A fault diagnostic table that interprets these LEDs is contained in the A60 Processor board troubleshooting section.

The direct I/O method of troubleshooting is useful when other, non-controller group boards are contributing to the service problem; direct I/O methods can check boards throughout the instrument. These methods are described in the general troubleshooting information found at the beginning of Section VIII in the Service Introduction. The A60 Processor troubleshooting section, as mentioned above, has a truncated version of this same information.

THEORY OF OPERATION

CONTROLLER SECTION - OVERALL DESCRIPTION

The controller group contains 3 PC boards:

A57 Marker/Bandcross board
A59 Digital Interface board
A60 Processor board

The A60 Processor will still operate if the A57 and A59 boards have been removed from the instrument.

The HP 8340A has a 16-bit I/O data bus (DB 0-15) and a 5-bit I/O address bus (ADR 0-4) which runs throughout the instrument. The I/O data bus is bidirectional, it sends and receives data from the instrument's various digital circuits.

The **[INSTR PRESET]** key on the front panel activates the Low-Instrument-PreSet signal (LIPS). The LIPS signal is also generated when the instrument is turned on. LIPS initiates several events in the controller, these are:

Override the A59 board's ability to shut down the processor.
Disable access to RAM.
Reset both the instrument and display processors.
Activates all front panel LEDs as well as the 16 self-test LEDs.
The self test LEDs are located on the A60 Processor board.

When LIPS is released the controller performs a self test containing the following steps:

Instrument processor internal registers are checked.
RAM is partially checked.
ROM is checked.
I/O address bus (ADR 1-5) is checked.
I/O data bus (DB 0-15) is checked.
The checksum of the calibration data is verified.
Refer to the **Calibration Constants** description in the Service Introduction.
The Analog-to-Digital Converter (ADC) is checked.
This circuit is located on the A27 Level Control board. The ADC is essentially an internal voltmeter which allows the instrument processor to monitor several dc levels in the instrument. Examples of these are; Modulation level, sweep voltage, and ALC level.

If the self test was initiated by an **[INSTR PRESET]**, the instrument sets all front panel functions to a *preset condition* and begins operation.

If the power switch was just turned on, a signal called "Hi Power UP" (HPUP) goes low. This signal tells the processor that, after self test is completed, it should restore *previous instrument settings*. The current instrument state, as well as all SAVE/RECALL registers, are stored in battery powered RAM for this purpose.

Processor and Memory Description

The heart of the controller is a 16 bit microprocessor. This processor directly interfaces with RAM and ROM.

Memory consists of the following:

UV ERASABLE PROGRAMMABLE ROM - 32k x 16.
The instruments firmware is stored in this memory as well as default calibration data.

ELECTRICALLY ERASABLE PROGRAMMABLE ROM - 2k x 16.
Protected calibration data is stored here.

RAM - 8k x 16.
Working calibration data and SAVE/RECALL register values are stored in RAM. A backup battery provides power to the RAM for at least one year when the instrument is disconnected from ac mains (or if the processor board has been removed from the instrument).

If the backup power to the ram should fail, working calibration data and SAVE/RECALL register information will be lost. When the instrument is turned on, protected calibration data will be placed in RAM and "CALIBRATION RESTORED" will be displayed in the front panel ENTRY display.

A59 Digital Interface Assembly Description

The digital interface links the processor to the sweep generator, M/N oscillator, and the 20-30 synthesizer. The microprocessor read/write strobes are used to enable either buffers that send data to the processor, or clock registers that store data sent from the processor. Several of these strobes operate registers located on other assemblies. For example, the phase-lock indicators allow the controller to determine which of the instrument's phase-lock loops are unlocked, while the M/N controls are registers that operate the M/N oscillator.

The digital interface connects to the 16-bit data bus (DB 0-15). By use of the LSTP (Low STоP) signal, this assembly has the ability to stop all processor operations. When the processor stops, the green "RUN" LED on the processor board is turned off. LSTP stops the processor when it is not needed, or when it is necessary to eliminate all potential sources of digital noise (e.g. during forward sweeps). When the LSTP signal releases the processor to perform a task, the processor defers processing until it determines that the LSRQ (Low Service ReQuest) signal is low. LSRQ can be sent low by the digital interface or by the front panel processor. Once LSRQ is sensed low it can go high again and the processor will still finish all pending tasks before checking this signal again.

By use of the change detectors and the processor SRQ blocks, the controller responds to the following:

Changes in the UNLOCK or OVEN indicators
Changes in OVERMOD or UNLEVELED conditions
Changes in the "EXTERNAL REFERENCE" switch position.
Any keystroke or RPG activity.

The processor also distinguishes between Power On and Instrument Preset, and responds to sweep events as indicated by the marker bandcross assembly.

A57 Marker/Bandcross Assembly Description

The marker bandcross assembly generates markers, controls the start and stop sweep points, and determines bandcrossing points. The marker/bandcross board also provides the front and rear panel sweep signal as well as several other rear panel interface signals. The sweep-event memory stores numbers that correspond to voltages on the 0-10 volt sweep signal. Each number stored in the memory represents a single sweep event. Sweep events are detected by the sweep comparator, which compares them against the 0-10 volt sweep ramp. Sweep events include:

Turning markers on and off.
Stopping the sweep for a bandcrossing.
Stopping the sweep for the end of sweep and retrace.

The manual sweep DAC is used to offset the sweep-out signal when the instrument is in CW or Manual mode. This DAC is also used as part of an algorithm to find the current sweep position when changes are made in frequency parameters during an analog sweep longer than 300 ms.

The sweep control block provides the capability of starting and stopping the sweep either from the rear panel or by the sweep comparator. CRT Z-axis control circuits provide the capability of blanking the sweep on a display for bandcrossings or retrace. Z-axis control is also used to intensify the display for markers.

The marker/bandcross board uses the LBX (Low Bandcross) signal to stop the analog sweep at positions previously loaded in the sweep event memory by the processor. When LBX is low, the A59 Digital Interface causes the processor to run, allowing the processor to perform the tasks necessary for the sweep to proceed. This will be either at a bandcrossing, or at a retrace at the end of a sweep.

CONTROLLER SECTION

TROUBLESHOOTING TO ASSEMBLY LEVEL

The controller functional group consists of the A57, A59, and A60 assemblies. Troubleshooting this section should begin by going to the Overall Instrument Troubleshooting guide in the Service Introduction. There are generally three levels of troubleshooting for these boards.

Self Test
The self test is run on Power-On after pressing **[INSTR PRESET]**. Two front panel LED's, CHECK I and II, give a visual indication of the self test results. These indicators, and their meaning, are explained in in the above mentioned portion of the Service Introduction.

Front Panel Initiated Direct I/O Addressing tests
The front panel can be used to write to or read from any I/O device.

Component Level Troubleshooting
Schematic diagrams, circuit theory, and troubleshooting information are provided.

The component level troubleshooting section associated with the A60 Processor board has the majority of the Controller functional group assembly level troubleshooting. Therefore, some diagnostics for A57 and A59 are also included in this section.

Problems in either the A57 Marker/Bandcross or A59 Digital Interface assemblies show up indirectly in other areas of the instrument's operation. Therefore, most troubleshooting for A57 and A59 should be done first through the overall instrument troubleshooting guide (located in the Service Introduction).

REPAIR PROCEDURES

BATTERY A60B1 REPLACEMENT

A60B1 (HP Part Number 1420-0331) provides backup power to the instrument's RAM IC's. This RAM holds working calibration data and the SAVE/RECALL register values. When the battery is defective or replaced, the above information will be lost. However, as soon as the instrument is reassembled and turned on, the protected calibration data stored in EEROM will be retrieved and placed in RAM. "CALIBRATION RESTORED" will be displayed in the instrument's ENTRY display

This battery will provide backup power for at least two years, and has a shelf life exceeding 10 years. It is not rechargeable.

NOTICE

A60BT1 has a strong outer case. The case has been shown to remain intact even when the battery is shorted or forcibly charged at a rate not exceeding 50 ma. However, if the battery is abused mechanically, electrically, or thermally, the following warning should be taken into account.

WARNING

This battery contains Lithium and Thionyl Chloride ($SOCL_2$), the latter in liquid form. If abused, this battery represents a fire, explosion, and severe burn hazard.

Lithium can burn or explode on contact with moisture in the air or water.

Thionyl Cloride is highly toxic, and on contact with air will partially break down into Hydrochloric acid and Sulfur Dioxide fumes which are also toxic and are extremely repulsive, strongly irritating, and are corrosive to the eyes, skin, lungs, and mucous membranes. CONTACT A POISON CONTROL CENTER OR DOCTOR IMMEDIATELY if a person comes in contact with or breathes this material.

Do not attempt to charge this battery, as this may cause it to rupture.

Do not damage or attempt to open the battery.

Do not heat above 212 degrees Fahrenheit (100 degrees Celsius), expose contents to water, or incinerate. Determine if state and local laws require disposal of Thionyl Chloride or Lithium in a chemical waste disposal site, or return the battery to the Hewlett-Packard Company, 1412 Fountaingrove Parkway, Santa Rosa, Ca. 95401, Attention: Environmental Engineering Department.

Batteries that are dead have converted most of the Lithium and Thionyl Chloride into non-toxic chemicals.

Replacement Procedure

CAUTION

The assembly mentioned below contains static sensitive components. Any work performed on instrument PC board assemblies should be done at a work station equipped with an anti-static surface. Any persons working on this instrument should wear a grounding strap that provides a path to earth ground of no less than 1 Megohm and no more than 2.5 Megohms. All anti-static safeguards must conform to state and federal safety standards and statutes. When handling a PC board always hold it by the edges. Never touch the finger contacts.

1. Disconnect ac mains from the instrument. Wait three minutes before proceeding to step 2.

2. Remove the instrument's top cover and remove the A60 Processor board. Refer to the front of any Service Section tab for an assembly location guide, if necessary, to locate this assembly.

3. Remove the battery and dispose of it in a safe manner, i.e. do not damage or incinerate it. This battery is not rechargeable. Do not attempt to charge it or internal pressure may cause it to rupture. Measure the voltage of the new battery before installing it. The voltage should be about 3.6 Vdc. Test the battery by placing a 10K Ohm resistor across it and measuring the voltage output. The voltage should not drop to less than 3.4 Vdc. If the battery is within voltage tolerance, install it. **Do not set the A60 Processor on bare metal as this may short out the new battery, possibly damaging it.**

4. Reinstall the A60 Processor board. Replace the top cover and turn the power switch ON. "CALIBRATION RESTORED" will be displayed in the front panel ENTRY display.

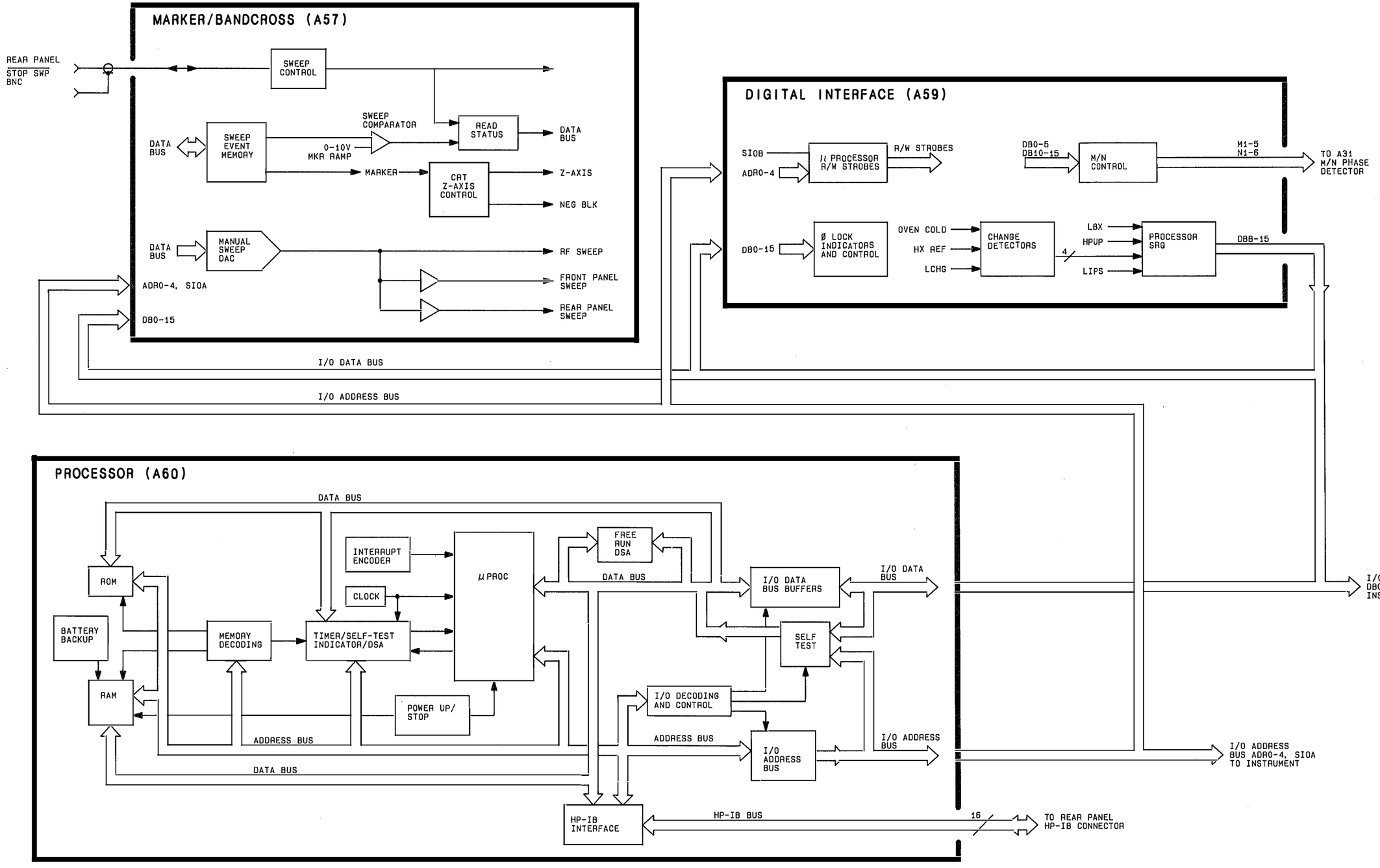


Figure 8G-1. Controller Section Simplified Block Diagram

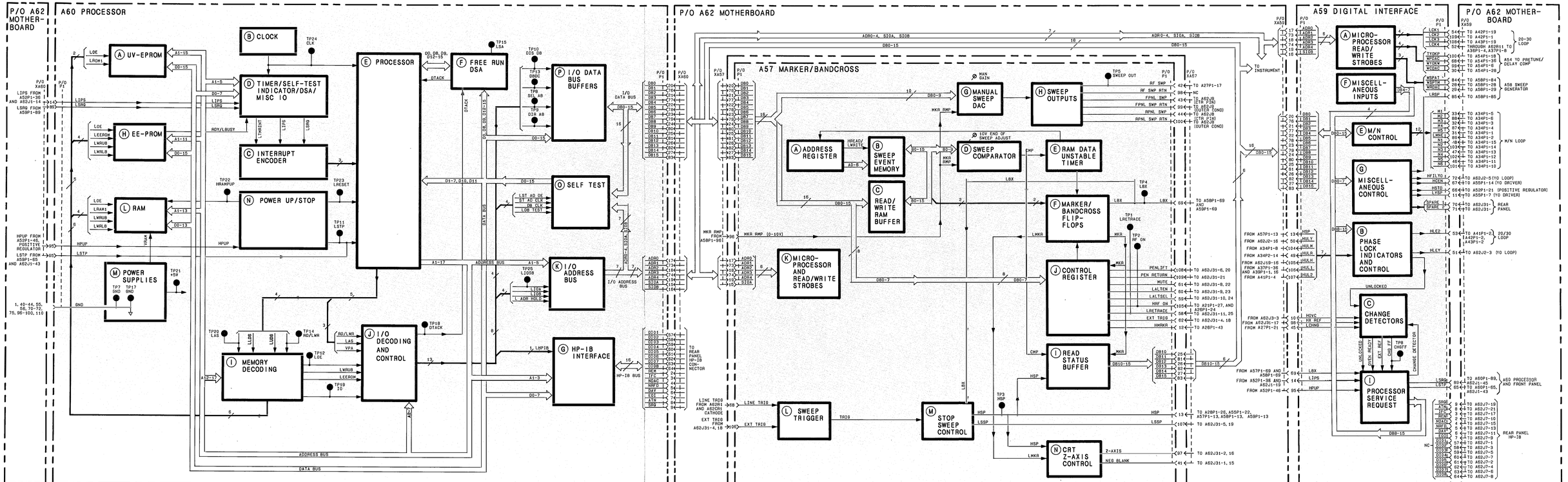


Figure 8G-2. Controller Section Block Diagram

A57 MARKER BANDCROSS ASSEMBLY, CIRCUIT DESCRIPTION

INTRODUCTION

The A57 Marker Bandcross board generates the Z-axis signal required to place intensity markers on a CRT. If enabled by the front panel, amplitude markers will be generated by sending a marker signal to the leveling circuits. The same circuits that detect markers are used to detect band crossings or the end of sweep. These circuits will cause the sweep to be stopped and the microprocessor to be activated. Other circuits interface with rear panel interface connections. Hardware on this board is used during self test to verify the operation of the 16-bit microprocessor data bus.

SWEEP EVENT DETECTION (BLOCKS A, B, C, D, E, AND F)

A sweep event is a Marker, a Band Crossing or the End of Sweep. Prior to the beginning of a sweep, the microprocessor will store in the Sweep Event Memory (Block **B**) a series of numbers which correspond to all the sweep events that are to take place during a sweep. These numbers are loaded in the following manner:

1. The processor sets the Address Register (Block **A**) to 0 (i.e., sets DB0-6 to zero then outputs address 12,R3:)

2. The processor writes into the Sweep Event Memory (Block **B**) a series of numbers corresponding to the sweep events. The Address Register (Block **A**) is automatically incremented after each write to memory (address 12,R0: to U1 pin 5).

3. The processor sets the Address Register (Block **A**) back to 0.

Before a sweep begins, the processor determines how many sweep events there will be in the sweep. For example, for a sweep containing one bandcrossing and a marker, there would be four sweep events: two for the marker, one for the bandcrossing, and one for the end of sweep. The processor then computes at what point in the sweep each event occurs and converts this information to a number from 0-999 which corresponds to the 0-10V sweep. This series of numbers is written into the Sweep Event Memory (Block **B**) via data lines B0-B9. When the Address Register (Block **A**) is set to location 0, the first number stored in the memory appears at the input of the Sweep Comparator DAC U3 (Block **D**). The DAC converts this number to a voltage between 0-10V. This voltage is not available at the output of U3 but is compared internally to the MKR RMP (marker ramp) 0-to-10V signal. When the MKR RMP rises to a voltage equal to the value at which the DAC is set, the output of U3 (pin 15) will fire comparator U6, and the

first sweep event occurs. This causes the Marker and the Bandcross flip flops (Block **F**) to be clocked. The data stored in the flip flops and taken from data bits 10 and 11 of the RAM (Block **B**, U15) determines what kind of sweep event will occur. A marker is created by two sweep events. The first event turns the marker on; the second turns the marker off. Markers are 1/1000 of the display width. When a user attempts to change one of the frequency parameters in the middle of a slow sweep (300 ms or longer), the Sweep Event Detection circuitry (combination of Blocks **A** through **F**) determines the position of the sweep, allowing the instrument to phase-lock to a frequency appropriate to the current sweep position. For faster sweep times, the instrument will wait until the beginning of the next sweep to make frequency changes.

ADDRESS REGISTER A

U1 and U10 comprise a 6 bit counter register. The counter is preset when the microprocessor writes to I/O address 12,R3: via U1 pin 11. The Address Register can be counted or incremented two ways: first by the microprocessor writing to I/O address 12,R0:, and secondly when timer U5B (Block **E**) fires. The signal from U5B indicates that a sweep event has occured and that the Sweep Event Detection circuitry (Blocks **A** through **F**) should get ready for the next sweep event. The outputs of the Address Register (A0 through A6) are used to address the Sweep Event Memory (Block **B**).

SWEEP EVENT MEMORY B

U2 and U15 are RAMs each containing 128 8 bit bytes. They are combined to provide 128 16 bit words of memory. Sweep events are stored into the RAM when the microprocessor does a write to I/O address 12,R0:. U8 and U16 (Block **C**) are buffers through which the microprocessor reads or writes RAM data. The RAM is addressed by the Address Register (Block **A**). In normal operation of the instrument, only about 15 of the 128 words of RAM are used. Each location used corresponds to a single sweep event that is to occur during the sweep. The RAM has stored in it, the position along the sweep where each event is to occur, as well as informaton indicating what kind of sweep event each one is.

READ/WRITE RAM BUFFER C

U8 and U16 make a 16 bit bidirectional buffer which connects the microprocessor with the Sweep Event Memory (Block **B**). When the microprocessor sends I/O Address 12,R0:, the buffer transfers data from the instrument data bus (DB0 thru DB15) to B0 thru B15. When the microprocessor sends I/O Address 12,R2: data is transfered the opposite direction (i.e., from the Sweep Event Memory to the microprocessor).

SWEEP COMPARATOR D

U3 is a 10 bit DAC which compares the 0-to-10V MKR RMP (marker ramp) to the binary number placed at its input by the Sweep Event Memory (Block **B**). The MKR RMP (0-10V) is connected to the V-Feedback input of U3 (pin 16). At the beginning of a sweep, the output of the DAC will be below 0 volts. When the voltage applied by the MKR RMP (0-10V) is equal to the corresponding digital number at the DAC's input, the output will go above 0 volts. Comparator U6 is set to trip when the output of the DAC rises above 0 volts. For example if a Sweep Event is to occur at mid-sweep, the following conditions would exist: the DAC would have the number 500 decimal or 111110100 binary placed at its digital input. Before the Marker Ramp gets to 5 volts, which represents the exact middle of the sweep, the DAC output would be below 0 volts and Comparator U6 output (pin 7) would be LOW. As the MKR RMP approaches 5 volts, the output of the DAC would approach 0 volts. When this occurs, the comparator will fire, causing its output to go HIGH. When the comparator fires, R28, R26 and R27 cause a 2 mV offset to be made to the positive input of the comparator (pin 2). This ensures that the comparator that just fired will not change states due to noise on the MKR RMP. R32 (10V END OF SWP ADJ.) is adjusted to make the end of sweep voltage equal 10.000 V.

RAM DATA UNSTABLE TIMER E

This circuit debounces the output of the Sweep Comparator (Block **D**) and causes the Address Register (Block **A**) to be incremented after each sweep event has been detected. U5B is triggered by the comparator firing and outputs a 700 ns pulse. The pulse sets timer U5A and also clocks the Marker/Bandcross Flip-Flops (Block **F**). Timer U5A resets after 5.7 us and is used to keep Timer U5B from being fired again until the circuits in Blocks A, B, C, and D have had time to settle following a sweep event. U20B controls the reset input of Timer U5B. The inputs of U20B are used to disable the timer. pin 5 of U20B is connected to U12B pin 6 (Block **M**) and is HIGH when the sweep is stopped. This keeps the timer from firing after the sweep has been stopped. pin 6 of U20B is controlled by the microprocessor through register U18 (Block **L**). This is set HIGH to disable the timer when the instrument does its self-test.

MARKER/BANDCROSS FLIP-FLOPS F

U11B and U11A are used to store B10 and B11 from the Sweep Event Memory (Block **B**). These two signals indicate what kind of sweep event is to take place. Bit 10 is connected to U11B pin 12 and sets the state of the MKR control line connected to its output

(pin 9). When a Bandcrossing occurs the sweep will be stopped so that the microprocessor can initiate phase-lock for that bandcrossing. This is done by the LBX signal. When a Marker occurs, the sweep is not stopped and the marker is generated as the sweep progresses.

MANUAL SWEEP DAC G

The manual sweep DAC U4 is used only in MANUAL SWEEP mode. A binary number between 0-1000 is written to the DAC. The digital input of the DAC is connected to registers U9 and U17. The microprocessor is connected to U9 and U17 via the I/O Data Bus. Data is clocked into these registers by strobe 13,R2: (Block **K**). In MANUAL SWEEP mode the MKR RAMP should always be at 0 volts. The U4 DAC converts its digital input to a voltage (0 to -10 V) at its output, U4 pin 15. The Op Amp, U7, will invert this signal to provide the 0 to +10V SWEEP OUT at TP5 (Block **H**).

The SWEEP OUT of Block **G** (U7 pin 6) is the result of either the manual sweep DAC, U4, when MANUAL SWEEP mode is selected, or the MKR RAMP when MANUAL SWEEP is not selected.

When the instrument is not in MANUAL SWEEP mode the input of the DAC is set to 0 by the microprocessor and the MKR RAMP is simply buffered by Op Amp U7.

The MAN GAIN (manual gain) adjustment, R33, is adjusted to obtain 10.000V at the sweep output when in MANUAL SWEEP and the manual frequency is set to the maximum possible value for a given sweep. For example: Set R33 to obtain 10.000V at TP4 when MANUAL SWEEP is on and the rotary knob is turned clockwise until the manual frequency is equal to the STOP frequency.

SWEEP OUTPUTS H

The SWEEP OUT is buffered by U30 and U27 which are connected to the front and rear panel Sweep Output connectors. Floating grounds are needed to eliminate ground loops which would cause 60Hz signals to appear on the sweep outputs. The front and rear panel sweep output connectors are floating. Any low frequency noise found on the floating front or rear panel sweep output connectors is connected by the RTN lines to the non inverting inputs of the buffer Op Amps. This allows the Op Amps to sense and remove this unwanted noise. C21 and C22 are provided to eliminate high frequecy noise.

READ STATUS BUFFER I

Buffer U24 enables the processor to monitor the state of the following signals by doing a read from I/O address 12,R1:

1. The Sweep Comparator (CMP) pin 12

2. The Marker flip flop (MKR) pin 14

3. The High Sweep (HSP) line, pin 2

CONTROL REGISTER J

Register U23 enables the processor to directly control the state of the various interface lines connected to the register. This is done when the microprocessor writes data to I/O address 13.R3:. The data is then available continuously at the output of the register.

AND gate U29A is used to control the RF Marker signal. When the RF Marker signal is HIGH, it causes the RF Power Control circuits to slightly increase the RF power. This is used as a marker. U29A pin 1 is used to turn this feature on or off.

MICROPROCESSOR READ AND WRITE STROBES K

The instrument processor outputs I/O address information on the I/O Address Bus (ADR0 thru ADR4 plus ADR5 which becomes SIOA). U28 decodes the address and generates the appropriate strobe.

These strobes are used throughout this assembly to either clock registers causing them to store data found on the I/O data bus or to enable buffers to place data on the I/O data bus so that the Microprocessor can read it.

The outputs of U28 are LOW true pulses of about 500 ns.

SWEEP TRIGGER L

Multiplexer U19 selects either LINE or EXT (external) trigger when the processor outputs the appropriate bits to the instrument Data Bus (DB 10 thru DB 13), and U28 outputs address 13,R0: (Block **K**). The output of U18 pins 5 or 7 will select the appropriate U19 input (i.e., U18 pin 7 HIGH selects Line Trigger, U18 pin 5 HIGH selects External Trigger). U18 pin 10 is used to disable the RAM Data Unstable Timer (Block **E**).

The ZON (Z axis ON) line is also controlled by U18 in a similar manner. The ZON signal when HIGH will force the Z-Axis line (Block **N**) to be +5V. U25 is a 3 to 8 decoder which generates 500 ns pulses at its output each time the microprocessor writes to I/O address 13,R1:. By writing appropriate numbers to this register, the following events can occur:

- Start the Sweep (U25 pin 11)
- Stop the Sweep (U25 pin 12)
- Trigger Enable (U25 pin 10)
- Clear the Bandcross Flip-Flop (Block **F**), (U25 pin 15).

U26B pin 9 is used to stop the sweep, or keep it stopped when it has already been stopped by a sweep event. The sweep is stopped when the signal is LOW.

STOP SWEEP CONTROL M

The sweep can be stopped by any of the following:

1. The Bandcross signal (LBX) applied to U12B pin 5 from the Sweep Event Detection (Block **F**).
2. The Bandcross signal (LBX) applied to U12B pin 5 when driven LOW by the Sweep Generator board. (NOTE: This will only occur if the Marker Bandcross board fails to stop the sweep before it gets to 12 volts.)
3. The Sweep Trigger (Block **L**, U12B pin 4) is told to stop by the processor.
4. The Low Stop Sweep (LSSP) BNC on the rear panel is held LOW.

The Low Stop Sweep (LSSP) is an IN/OUT signal. As an input signal, LSSP is applied to U12C pin 9 and is used to generate HSP. As an output signal, it is taken from U13A pin 1 which is an open collector line pulled up to +5V.

The HSP signal goes to all devices in the instrument that need to respond to the sweep starting and stopping.

CRT Z-AXIS CONTROL N

The Z-AXIS signal is normally used to drive the Z-axis input of a CRT display. When this signal is 0 volts, the display will turn its beam on with normal brightness. When it is at +5 volts, the display turns its beam off (ie. blanks). When it is at -5 volts, the display intensifies its beam. The 8340A Z-AXIS signal may be used to turn the display off for bandcrossings, when the sweep is being reset (sweeper retrace), or at other times when the instrument is waiting for a sweep to start. Z-AXIS is also used to show markers by brightening the display. During all other times the Z-AXIS output is at 0 volts.

U21 is a TTL NOR gate. The outputs (U21C and U21D) are pulled up to +5 volts in the high state by R37 and R38. U21B is used to provide Op Amp U14 with a LOW TTL reference voltage. U21D pin 13 is LOW when either HSP or ZON is high. This output is connected thru R19 to Op Amp U14 that will put 0 volts on the NEG BLANK (negative blanking) output. When both HSP and ZON are low, U21D pin 13 will be HIGH and the NEG BLANK output will be at -5 Volts. When U21 pins 10 and 13 are both LOW the Z-AXIS will be 0 Volts. When pin 10 is HIGH and pin 13 is LOW Z-AXIS should be -5 Volts. Pins 10 and 13 should never both be HIGH in normal operation. When pin 10 is LOW and pin 13 is HIGH, Z-AXIS should be +5 Volts. VR1, VR2, and VR3 provide protection against a DC voltage that might be applied to the output connector. C23 and C24 provide frequency compensation to keep the Op amps stable.

INTERFACE SIGNALS

1. 8410B INTERFACE: The following signals from this board are needed when the 8340A is connected to the 8410B:

   a. 0-to-10v SWEEP (Drives the X-axis of the Display)
   b. STOP SWP (Allows the 8410B/C to stop the Sweep)
   c. NEG BLANK (Does Display blanking)
   d. Z-AXIS (Used to generate markers on the Display)
   e. 8410 EXT TRIG (Used to initiate 8410B/C to phase-lock every time the 8340 phase-locks i.e., new CW frequency or start of sweep.)

2. 8755C INTERFACE: The following signals from this board are needed when the 8340A is connected to the 8755C and it is desired to use ALTERNATE SWEEP:

   a. 0-to-10V SWEEP (Drives the X-axis on a Display)
   b. Z-AXIS (Controls Blanking and Marker generation)
   c. LALTEN (Low indicates Alternate Mode Enabled)
   d. LALTSEL (Low indicates Alternate State Active)
   e. LRETRACE (Low indicates Retrace used to synchronize with the start of sweep)

3. PLOTTER INTERFACE:

   a. MUTE bar (Used to freeze the servo for Bandcrossings)
   b. PEN LIFT (Used to raise the pen for retrace and, optionally, for bandcrossings)
   c. 0-to-10V SWEEP (Used to drive the X-axis)

A57 MARKER BANDCROSS ASSEMBLY, TROUBLESHOOTING

CHECKING MICROPROCESSOR I/O ADDRESS STROBES

U28 (Block **K**) is connected to the I/O address bus and generates all of the I/O strobes used on this assembly. The strobes on the output of U28 can be checked using the front panel to write directly to U28's I/O address while monitoring the IC's outputs. This would be done as follows: Press **[INSTR PRESET]**, then **[MANUAL]** sweep key. Connect a Logic probe to the output that is to be checked. At the front panel, enter the corresponding I/O address. The I/O address is written on the lines connected to the output of U28. For example, the WRITE RAM signal is marked, 12,R0:. The number 12 is called the CHANNEL and the number 0 is called the SUBCHANNEL. This is entered in the front panel as follows: **[SHIFT] [GHz] [1] [2] [Hz]** -.setting the I/O channel and **[SHIFT] [MHz] [0] [Hz]** - setting the I/O subchannel. Once this has been done, Press **[SHIFT] [KHz]**. Make entries by pressing the step keys, using the RPG or by making data pad entries. Each entry will cause the WRITE RAM strobe to be generated. This will be a LOW True signal, approximately 500 ns wide, that can be monitored with the logic probe. It can also be seen on a storage scope. Refer to "Direct I/O Addressing" in Section VIII, Service Introduction, for more informaion.

CHECKING MICROPROCESSOR OUTPUT DEVICES

The following devices are microprocessor output devices: U1, U10, U8, U16, U18, U25, U9, U17 and U23. These can be checked by using the front panel to write directly to the I/O addresses as described above. To do this, the I/O channel and subchannel must be entered at the front panel. These numbers can be found by reading the I/O address from the schematic on the write input of the device. After the address has been entered, Press **[SHIFT] [KHz]**. Entries can now be made directly to the device you are interested in. Monitor the outputs at the same time you enter numbers that will affect the signals of interest. For example, if the signal of interest is taken from DB2 of the I/O data bus, enter the number 0 and observe the register output; it should go LOW. Then enter the number 4 and observe that DB2 goes High. Note that if U8 and U16 are being checked, the outputs are only valid during the time the write strobe is LOW. Note that the instrument should be in MANUAL sweep mode so that the normal operation of the instrument does not cause the devices being tested to be written into.

CHECKING MICROPROCESSOR INPUT DEVICES

Input devices can be checked in a similar manner as the output devices. The front panel is used to set up the I/O channel and subchannel as before. U24, U8, and U16 are the only input devices on this assembly. After setting the correct address on the front panel, press **[SHIFT] [Hz]**. Each time **[Hz]** is pressed, the instrument will read from the addressed I/O device and display the results in the entry display in both decimal and octal formats. By shorting each input of the input devices to +5v or ground, each input can be checked.

VERIFICATION

Power On Checks

When the 8340A goes through Power On or Instrument Preset, the Marker Bandcross board is partially checked out. The instrument processor uses the circuitry in Blocks **A**, **B**, **C**, and **K** to verify the I/O data bus. This is done by sending data to the Sweep Event Memory (Block **B**) and then reading it back. In this manner, it can determine if any of the 16 data bits are open or shorted. If the Instrument Check light II goes off following Power On or Instrument Preset, this indicates that the above test has passed.

If the light is on, a problem is indicated. Further information about the problem can be obtained by decoding the 16 self test LEDs on the processor board. (Refer to the A60 Processor board documentation). When the Marker Bandcross board is removed from the instrument, the front panel Instrument Check light II should go on indicating that this test has failed.

Isolating the Problem

To help verify that the problem is on the A57 MARKER/BANDCROSS board, it may be usefull to remove the A57 assembly and observe the instrument behavior. With A57 removed, the following should occur:

1. Following Power ON or Instrument Preset, Instrument Check light II should stay on and instrument Check light I should go off. All 16 self test LEDs on the processor board should remain on.

2. When sweeping, the sweep should stop at 12 volts before resetting. NOTE: the sweep will not be measurable at the front or rear panel connectors since the buffers for these signals are on the A57 board which has been removed. The sweep can be checked on the A58 Sweep Generator.

3. The instrument should lock up properly in CW or MANUAL and perform normally except for the absence of sweep output and display blanking.

4. In a multi band sweep, bandcrossings will all occur when the sweep gets to 12 volts instead of the correct places.

SWEEP DETECTION CIRCUITS: (Blocks A through F)

Verification of Blocks A Through F

Press the following controls: **[INSTR PRESET] [SWEEP TIME] [2] [0] [SEC] [SHIFT] [M2]**. Observe the left most front panel display. This should indicate the band number as the instrument goes from band to band. Observe that the green SWEEP LED goes out at band crossings. If the numbers are not changing, this indicates that LBX (Block **F**) is not being generated. If the numbers seem to rapidly count from 1 through 5 , this indicates that LBX (Block **F**) is not being pulled LOW as it should when the sweep progresses. LBX is the main output of the SWEEP DETECTION circuits.

Troubleshooting Blocks A Through F

Once deterimined that the problem is in Blocks **A** through **F**, perform the following tests:

Block **D:**

1. Press the following keys: **[INSTR PRESET] [delta F] [1] [Mz] [SWEEP TIME] [1] [0] [sec].**

2. Verify that U3 pin 16 has a 10 second 0-to-10V ramp present.

3. Check the B9 through B0 inputs of DAC U3 for the following:
   (B9) 1 1 1 1 1 0 1 0 0 0 (B0).

4. U3 pin 15 should be below 0 volts until the sweep gets to 10 volts. As the sweep rises above 10 volts, the voltage at pin 15 should rise above 0 volts, and comparator U6 should fire, forcing CMP (U6 pin 7) HIGH for about 50 ms.

Block **E:**

1. Press the following keys: **[INSTR PRESET] [delta F] [1] [MHz].**

2. Trigger a scope on the rising edge of CMP (U6 pin 7) and observe that U5B should have a 700 ns positive pulse at pin 5 and an inverted identical pulse at pin 12.

3. Observe that each time U5B fires, U5A should also fire, creating a 5.7 us positive pulse at U5A pin 13.

4. Make sure that U5B pin 11 is not stuck LOW. It should only go LOW when the 8340A is not sweeping.

Block **F:**

1. Press the following Keys: **[INSTR PRESET] [START FREQ] [1] [GHz] [STOP FREQ] [1] [3] [GHz] [SWEEP TIME] [1] [0] [0] [msec] [M1] [8] [GHz] [M2] [1] [1] [GHz] [MKR delta].**

2. U11B pin 9 MKR should be a HIGH for 30 ms, then LOW for about 100 ms repetitively.

3. U11A pin 5 should go HIGH for about 50 ms when the SWEEP OUT TP5 gets to about 4 volts. When the SWEEP OUT gets to 10 volts, there should be another 50 ms pulse.

4. U11A pin 1 should have a single 500 ns pulse applied by U25 at the end of each sweep. If not present, check U25 (Block **L**) using direct I/O addressing. Refer to the direct I/O addressing description in the Service Introduction.

Block **C:**

Bi-directional buffers U8 and U16 are thoroughly verified by the Instrument Preset/Power On tests. If Instrument Check Led II is off, the buffers are good. Use direct I/O addressing to verify that data can be sent from DB0-DB15 to B0-B15. To verify the other direction from B0-B15 to DB0-DB15, do the following:

1. Press **[INSTR PRESET]** then **[SINGLE]** SWEEP. Do a read from address 12,R2: (reads sweep event from RAM). Press **[SHIFT] [GHz]**, enter address **[1] [2]** and press any terminator (i.e., **[GHz], [MHz], [kHz], [Hz]**), press **[SHIFT] [MHz]**, enter subchannel **[2]**, press any terminator, press **[SHIFT] [Hz]** (read).

NOTE

Pressing [SHIFT] [XTAL] will cause the 8340A to pause at the next band crossing. Pressing [SHIFT] [Hz] may read a different value. Then press [SHIFT] [INT] to advance to the next band crossing and [SHIFT] [Hz] to read.

2. The entry display should show an octal number and its decimal

equivalent. Convert the octal number to binary. This is the number that should be setting on B0 through B15. It is important to realize that in order for B0 through B15 to be correct, the SWEEP EVENT MEMORY must have been properly loaded with this number. This loading is done through U8 and U16. It is therefore necessary to first check to see if U8 and U16 can transfer data from the instrument Data Bus to the Marker Bandcross Bus (B0 through B15). Before Replacing U8 or U16, verify that the two I/O strobes 12,R2: and 12,R0 are being generated by U29 (Block **K**). If the problem only involves a few bits, the self test leds on the A60 Processor board can be used to indicate which bits are incorrect. If all leds are on, this indicates that the problem may have to do with Blocks **A, B, E,** or **K.**

Block **A:**

1. Do the following: Press **[INSTR PRESET], [SINGLE] SWEEP, [SHIFT] [XTAL], [SHIFT] [GHz],** enter **[1] [2]** and press any terminator, **[SHIFT] [MHz],** enter **[3]** and press any terminator, **[SHIFT] [KHz]** (write), enter **[0]** and press **[Hz].** This should Clear U1 and U10. Verify that lines A0 through A6 are LOW.

2. Enter the numbers **[1], [2], [4], [8], [1] [6], [3] [2], [6] [4],** using the front panel. These entries should be latched into U1 and U10 and appear on the A0 through A6 lines. For example, when the number 16 has been entered, the A bus should be (A6) 0 0 1 0 0 0 0 (A0).

3. Press **[0] [Hz] [SHIFT] [MHz] [0] [Hz].** The A Bus should be all LOW. Note that each time a **[STEP]** key is pressed, the number on the A Bus should be incremented by 1. The numbers should be 0 = (A6) 0 0 0 0 0 0 0 (A0); 32 = (A6) 0 1 0 0 0 0 0 (A0); 15 = (A6) 0 0 0 1 1 1 1 (A0). U29B pin 5 should be HIGH throughout this entire test. U29B pin 6 should follow U29B pin 4.

Block **B:**

Use direct I/O addressing to check that the READ/WRITE RAM BUFFER (Block **C**) is able to place data on the B-BUS (B0 through B15). Use this Test for Block A to verify that the A-BUS can be controlled properly. Make sure that U8 and U16 can read the B-Bus as follows:

1. Press **[INSTR PRESET], [SINGLE]** SWEEP, **[SHIFT] [GHz],** enter **[1] [2]** and press any terminator, press **[SHIFT] [MHz],** enter **[2]** and press any terminator, press **[SHIFT] [Hz]** to read, then **[SHIFT] [MHz] [2] [SHIFT] [Hz].**

2. Alternately short each B-BUS line to + 5V and ground. After each short is made, press **[SHIFT] [Hz]**, and note that the octal number in the entry display should indicate the appropriate bit forced HIGH for shorts to +5V, and LOW for shorts to ground.

3. In the above check, if all pass, it should be possible to store and read back numbers in the SWEEP EVENT RAM by doing the following:

   Press **[INSTR PRESET] [SHIFT] [XTAL] [SHIFT] [SINGLE] SWEEP [SHIFT] [GHz] [1] [2] [Hz]**

   Locations in RAM can now be written as follows:

   Press **[SHIFT] [MHz] [3] [Hz] [SHIFT] [kHz]** to write then:

   [a] [a] [a] [Hz] (aaa = RAM address from 0 through 127)

   Then press **[SHIFT] [MHz] [0] [Hz] [SHIFT] [kHz]** to write then:

   [d] [d] [d] [Hz] (ddd = data to be written to RAM)

   It is only necessary to check through address 15. Use the above commands to write into RAM a sequece of numbers. Then verify that the numbers are properly stored in the RAM by pressing:

   [SHIFT] [MHz] [3] [Hz] [SHIFT] [kHz] [a] [a] [a] [Hz] [SHIFT] [MHz] [2] [Hz] [SHIFT] [Hz]

   Note: aaa is the RAM address. The read data from the RAM will be displayed in decimal and octal in the entry display. Verify that it matches the sequence of numbers entered.

VERIFICATION AND TROUBLESHOOTING OF BLOCKS G THROUGH N

The Manual Sweep DAC (Block **G**) and the Sweep Outputs (Block **H**) can be checked simply by putting the front panel in MANUAL and while monitoring the sweep outputs on the front or rear panel turn the rotary control and observe that the voltage is 10 volts when the MANUAL frequency is as high as possible and that it is 0 volts when the frequency is adjusted as low as possible. It should be continuously variable in between. Note: for this test to work, the MKR RAMP must be at 0 volts. This should always be the case in MANUAL sweep.

The Sweep Trigger (Block **L**) can be checked from the front panel. Press **[INSTR PRESET]** and observe the green SWEEP LED. It should

be on during the sweep and go out momentarly for each bandcrossing and for the end of sweep. Press the EXT (external) Trigger button, make sure there is no external trigger signal, and observe that the sweep stops. Then use a logic pulser or other means to create a single external trigger. Verify that the instrument makes a complete sweep but does not continue to sweep. To check the line trigger, select **[delta F]** and enter **[1] [MHz]** so the instrument will be able to make 10 ms sweeps. Observe that the sweep repitition rate is slower when in **[LINE]** trigger.

The Sweep Event Detection circuitry can be verified by making the following set up:

[INSTR PRESET] [START] [3] [GHz] [STOP] [6] [GHz] [M1] [4] [GHz] [M2] [5] [GHz] [MKR delta] [1]

Monitor the Sweep Output and the Z-axis signal on a scope. The Sweep Output should stop at 10 volts before being reset for the next sweep. If the sweep goes to 12 volts, something is wrong. Observe the Z-axis signal to see if the **[MKR delta]** is on for the middle portion of the sweep. Now turn off the Delta Marker and observe if two markers are indicated by the Z-axis signal. U6 pin 7 should have a pulse on it for each sweep event. If this does not occur, slow down the sweep to 200 sec and turn all markers off. Measure the inputs of U3 to see if the binary number that is input is correct. It should be 1000 decimal or in binary it should be: (bit 10) 1 1 1 1 1 0 1 0 0 0 (bit 0). This number represents a 10V set point for the comparator.

The Ram Data Unstable Timer (Block **E**) should be checked for the 5.7 us and 200 ns pulse widths. Make this check by clocking a scope on the CMP signal (Block D, U6 pin 7). The instrument should be in Instrument Preset state.

If U2 and U15 are suspected, A0 through A6 can be checked via DSA using the I/O data test found with the A60 Processor documentation. If these signatures are incorrect, make sure that the Ram Data Unstable Timer (Block **E**) is not clocking the Address Register. This should be disabled by putting the instrument in MANUAL sweep while performing the test.

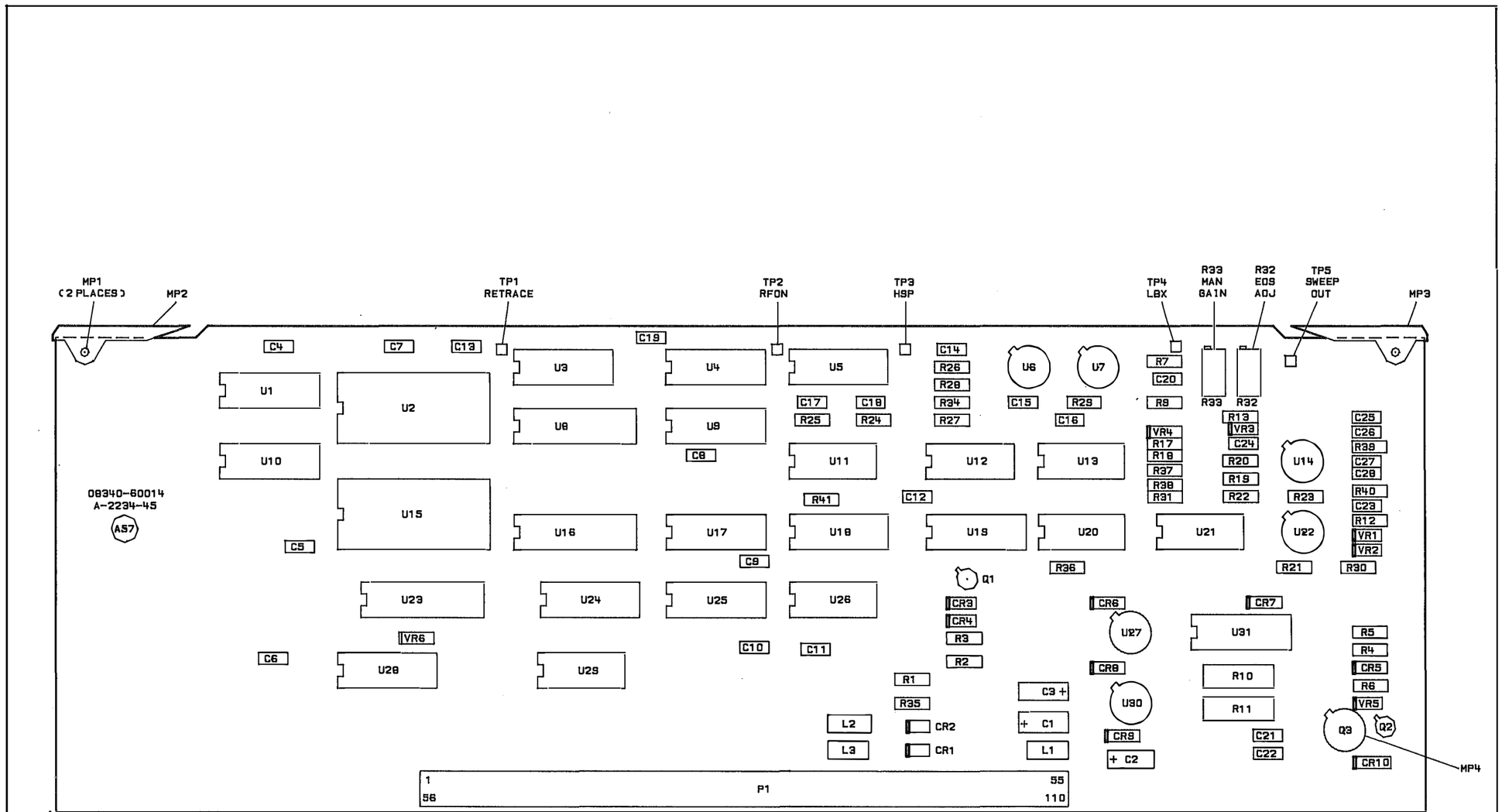


Figure 8G-3. A57 Marker/Bandcross, Component Location Diagram

A57 Marker/Bandcross P1 Pin I/O (1 of 3)

Pin	Mnemonic	Levels	Source	Destination
1 56	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*O *O
2 57	HMRKR LINE TRIG	TTL (HIGH TRUE) LINE FREQ 7 TO 10V	J A62-CR1 CATHODE/A62R1	XA26P1-43 L
3 58	LRETRACE	TTL (LOW TRUE)	J	F A62J31-11, 25
4 59	LALTSEL	TTL (LOW TRUE)	J	A62J31-10, 24
5 60	LALTEN	TTL (LOW TRUE)	J	A62J31-9, 23
6 61	MUTE	TTL (HIGH TRUE)	J	A62J31-8, 22
7 62	8410 TRIG	TTL	J	A62J31-7
8 63				
9 64				
10 65				
11 66				
12 67	HMRKR	TTL (HIGH TRUE)	J	XA26P1-43
13 68	HSP LINE TRIG	TTL (HIGH TRUE) LINE FREQ 7 TO 10V	M A62-CR1 CATHDDE/A62R1	*I N L
14 69	LIPS LBX	TTL (LOW TRUE) TTL (LOW TRUE)	XA52P1-36/A62J1-19 *F	*NOT USED M XA59-69
15 70	SIDA GND PLANE	TTL (LOW TRUE) 0V	XA60P1-15 INSTRUMENT GROUND	*K *O
16 71	SIOB GND PLANE	TTL (LOW TRUE) 0V	XA60P1-16 INSTRUMENT GROUND	*NOT USED *O
17 72	ADR0 GND PLANE	TTL 0V	XA60P1-17 INSTRUMENT GROUND	*K *O
18 73	ADR2 ADR1	TTL TTL	XA60P1-18 XA60P1-73	*K *K
19 74	ADR4 ADR3	TTL TTL	XA60P1-19 XA60P1-74	*K *K

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A57 Marker/Bandcross P1 Pin I/O (2 of 3)

Pin	Mnemonic	Levels	Source	Destination
20 75	DB0 GND PLANE	TTL 0V	*C XA60P1-20 INSTRUMENT GROUND	*A C G J *O
21 76	DB2 DB1	TTL TTL	*C XA60P1-21 *C XA60P1-76	*A C G J *A C G J
22 77	DB4 DB3	TTL TTL	*C XA60P1-22 *C XA60P1-77	*A C G J *A C G J
23 78	DB6 DB5	TTL TTL	*C XA60P1-23 *C XA60P1-78	*A C G J *A C G J
24 79	DB8 DB7	TTL TTL	*C XA60P1-24 *C XA60P1-79	*C G *C G J
25 80	DB10 DB9	TTL TTL	*C I XA60P1-25 *C XA60P1-80	*C L *C G
26 81	DB12 DB11	TTL TTL	*C I XA60P1-26 *C I XA60P1-81	*C L *C L
27 82	DB14 DB13	TTL TTL	*C I XA60P1-27 *C I XA60P1-82	*C L *C L
28 83	DB15	TTL	*C I XA60P1-83	*C L
29 84	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*O *O
30 85	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*O *O
31 86	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*O *O
32 87				
33 88				
34 89	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*O *O
35 90	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*O *O
36 91	+5.2V +12V	+5.2V +12V	XA52P1-17, 18, 41, 42 XA52P1-9, 33	*O *NOT USED
37 92	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*O *O

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A57 Marker/Bandcross P1 Pin I/O (3 of 3)

Pin	Mnemonic	Levels	Source	Destination
38 93	−15V −5.2V	−15V −5.2V	XA56P1-15, 30 XA53P1-18, 36	*O *O
39 94	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*NOT USED *NOT USED
40 95	GND PLANE	0V	INSTRUMENT GROUND	*O
41 96	NEG BLANK MKR RMP	0, +5V 0 TO 10V SWEEP	N XA58P1-96	A62J31-1, 15 D G
42 97	RFSWP Z-AXIS BLANK	10V/SWEEP +5V/−5V	H N	XA27P1-17 A62J31-2, 16
43 98	FPNLSWP	10V/SWEEP	H	A62J9-SMC CENTER
44 99	RPNLSWP FPNLSWP RTN	10V/SWEEP 0V	H H	A62J8-SMC CENTER
45 100	RGND RPNLSWP RTN	0V 0V	STAR GND POINT H	*O *
46 101	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*O *O
47 102				
48 103				
49 104	HULH HULH	TTL (HIGH TRUE) TTL (HIGH TRUE)	A62J19-16 A62J19-16	*NOT USED *NOT USED
50 105	HRFON	TTL (HIGH TRUE)	J	*
51 106	EXT TRIG	EXTERNAL SOURCE LEVEL	A62J31-4, 18	L A62J31-4, 18
52 107	LSSP	TTL (LOW TRUE)	M	A62J31-5, 19
53 108	PEN LIFT	CLAMP AT 56V	J	A62J31-6, 20
54 109	LSRQ PEN LIFT RTN	TTL (LOW TRUE) 0V	* J	*NOT USED A62J31-21
55 110	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*O *O

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

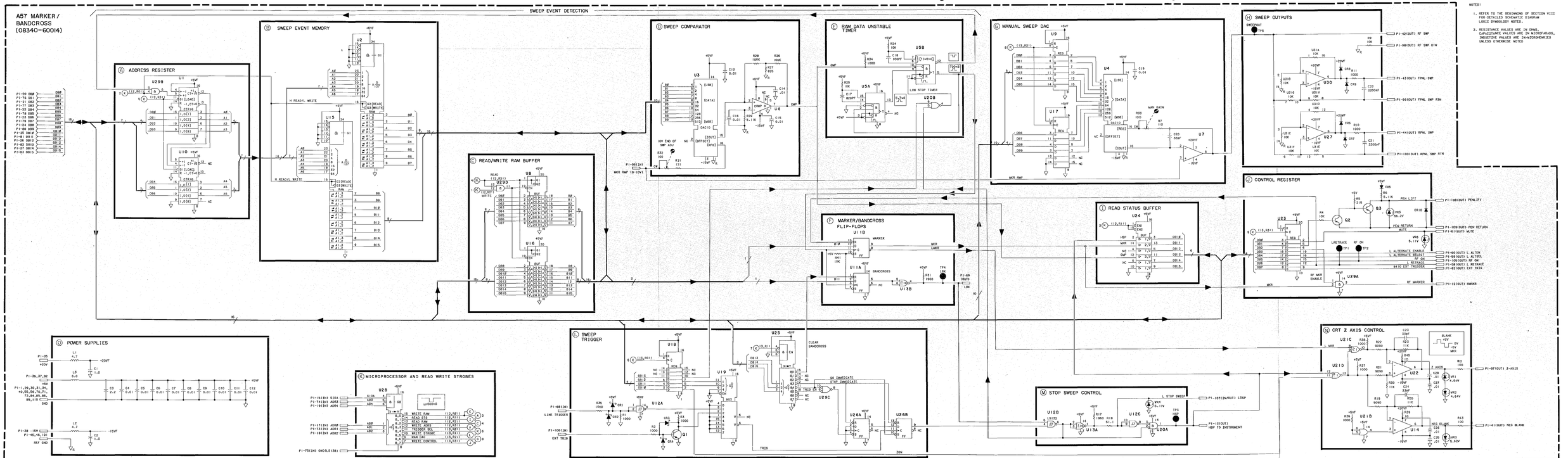


Figure 8G-4. A57 Marker/Bandcross, Schematic Diagram

A59 DIGITAL INTERFACE ASSEMBLY, CIRCUIT DESCRIPTION

INTRODUCTION

The Digital Interface board communicates to the Microprocessor the tasks which need to be performed. In normal operation of the instrument, the Microprocessor stops running when all tasks are completed. This control (when the processor runs) is done via the LSTP (Low STop Processor) control line (Block **H**). Many I/O addresses are decoded on the board that are used to latch data from the I/O data bus for several assemblies that are external to this board. Some signals are latched on the A59 Digital Interface and then sent to other assemblies via the motherboard. An example is Block **E**.

Phase Lock Indicators and Control (Block **B**) also reside on the board.

MICROPROCESSOR READ/WRITE STROBES A

The three decoders (U12, U19, and U26) decode 24 possible I/O addresses. The outputs of these 3-to-8 line decoders are used by circuits both on and off the A59 board to clock latches connected to the I/O bus or to enable buffers connected to the bus for input operations. There are also several decoders on other PC boards where additional addresses are decoded. SIOB is a 500 ns pulse which enables the three decoders. While they are enabled, the logic signals on ADR0 through ADR4 are used to select specific I/O addresses. For example, I/O address 3,R3: (Channel 3, Subchannel 3) causes a 500 ns strobe at U19 pin 7 when lines ADR4 through ADR0 are (ADR4) 0 1 1 1 1 (ADR0) and at the same time SIOB is LOW.

PHASE LOCK INDICATORS AND CONTROL B

The six Phase-lock loops in the instrument can be monitored to determine if they are locked by writing into the U24 register a mask that will select individual Lock Indicator signals and allow the processor to test them via U18 Processor Service Request circuits (Block **H**). During instrument operation, the instrument processor sends data to U24 register that sets up U25 and U11 to monitor the Phase Lock Indicators. These indicate either a locked or unlocked condition for a particular 8340A function. The outputs of U24, pins 2 and 12, are inverted by U22A and U22B. U22A and U22B are RS flip-flops wired as inverters. These inverted signals are used to set flip-flops U22C and U22D. The outputs of these flip-flops control the LOCK/ROLL signals for the 20-30 Loop and the YO Loop. Once these flip-flops are set, the corresponding phase-lock loop will try to lock. This condition will persist until the set signals are removed and the High Sweep signal (HSP)

goes True indicating the start of a sweep. This will cause the appropriate oscillator to switch from LOCK to ROLL mode. When the instrument is sweeping, either the YO or the 20-30 oscillator will be allowed to sweep by having its LOCK/ROLL control line set to ROLL. The 20-30 is swept when the YO Delta F is < 5 mHz. NOTE: The YO Delta F is the overall sweep width divided by the harmonic number (1 thru 4). The remaining outputs of U24 are ANDed with the corresponding Oscillator LOCKED signals and ORed together by U11 and U25 to generate the UNLOCKED signal.

The DLI (TP4) test point can be pulled to +5 Volts for troubleshooting to cause the processor to think all oscillators are locked up when they are not. This should cause the front panel UNLOCKED light to go out.

CHANGE DETECTOR C

Several conditions need to be continuously monitored and responded to by the Instrument Controller when they change state. Since the Controller stops running when it has completed its tasks, this circuit detects changes in instrument conditions and causes the controller to run again so that the changes can be responded to. The changes that are detected are:

1. OVEN becoming cold or up to temperature.

2. Change in enabled Phase LOCK indicators.

3. Rear panel frequency reference switch set to EXT.

4. LCHNG line being driven LOW due to one of the following conditions:

    a. Change in the OVERMODULATION indicator.
    b. Change in UNLEVELED indicator.
    c. Service request from the ADC.

When the control signal from the OVEN HOVC falls below 3.5 volts, the output of comparitor U13 goes HIGH. This signal is buffered by U7A which drives U6B. U6B immediately produces a LOW at pin 4 in response to the positive-going change at input pin 6. When C2 is charged up some 100 us later, pin 5 of U6B goes HIGH, forcing the exclusive OR gate to return its output to a HIGH. The resulting negative-going pulse from U6B will cause flip-flop U4C to be Set. The output of U4C goes to Block H and causes the instrument processor to check for a change in one of the conditions listed above. When the OVEN control signal changes in the opposite direction (i.e., rises above 3.5 volts), U13 will change states again. This change will again cause U6B to create a LOW-going pulse about 100 us wide. Changes in the UNLOCKED and External

Reference signals also cause LOW-going pulses on the LCHNG line. The LCHNG line runs on the A62 Motherboard so that other circuits in the instrument can indicate the need for service from the instrument controller. Where this is done an exclusive OR gate similar to U6B is also used to create LOW-going pulses on LCHNG.

M/N CONTROL E

Two registers, U10 and U17, are used by the processor to latch control signals necessary to program the M/N Oscillator. This is done when the processor does a WRITE to I/O address 3,R3:. The M/N off signal could be used to turn the M/N oscillator off. Currently the oscillator is never turned off.

MISCELLANEOUS INPUTS F

The buffer, U7B, is used to allow the processor to determine if any options are set. Currently none are used. The input on I/O bit 4 (DB4) is tied LOW and can be used by the processor to determine that the digital interface is present.

MISCELLANEOUS CONTROL G

The register, U23, is used by the processor to latch eight bits of information that are sent to the motherboard to control various functions. This is done when the processor does a WRITE to I/O address 1,R3:. The control signals are:

HSTD (High STandarD) A HIGH indicates the Internal Frequency Standard has been selected. The rear panel switch should cause this signal to change state.

HFILYO (High FILtered YO) A HIGH places a large filter capacitor across the YO coil. This is done in the CW or MANUAL mode.

LRSP (Low Reset SweeP) A LOW causes the Sweep Generator to reset the sweep. This is done at the end of every sweep. The reset signal is removed before the sweep starts.

LYSP (Low YO SweeP) This signal goes to the A55 YO Driver board. It is a TTL signal that is LOW for YO sweep widths greater than 5 MHz. This signal switches out a filtering capacitor on the driver board so that it does not add any swept frequency delay.

HCEN (High Compensation ENable) This signal goes to the A55 YO Driver board. It is a TTL signal that, when HIGH, allows the ramp voltage VCOMP to be added to PRETUNE on the driver board. This compensates for the swept frequency delay of the YO.

PROCESSOR SERVICE REQUESTS H

Buffer/Register U18 is used by the processor to determine which tasks need to be performed. All conditions that need the processor's attention are communicated through this register except for the front panel, which can generate its own service request. All possible reasons for service are ORed by U5 and the result is sent to the processor on the LSRQ line, indicating that service is requested. The LSTP line is driven by flip-flop U4D that is used to stop the processor from running when all tasks have been completed. U9B in an inverting open collector output buffer. Flip-flop U4D is set when the processor does a WRITE to I/O address 5,R0:. This is done to stop the processor when all pending tasks have been completed. U4D is reset to cause the controller to run again any time LSRQ is driven LOW. LSRQ can be driven LOW by U5 through U3E and U9F, or by the front panel to indicate a key has been pushed or the rotary control has been turned.

The Following conditions can be monitored when the processor does a READ from I/O address 4,R3: through U18:

- BANDCROSS - This line is driven by the LBX from A57 Marker Band Cross board. After being inverted by A59U3C, A59TP6 "BC" will go HIGH whenever a sweep event occurs. The Sweep Generator can also drive the LBX line if the sweep ever excedes 13 volts.

- UNLOCKED - An oscillator is unlocked

- EXT. REF. - External Reference is selected by the rear panel Frequency Standard INT/EXT Switch.

- OVEN Ready

- POWER FAIL - This indicates that a Power On has just occured. This is used by the processor to determine whether to do an Instrument Preset or a Power On restore of the last state. The processor cannot otherwise distinguish between Power On and Instrument Preset.

- CHANGE FF - One of the Change Detector inputs has changed.

POWER SUPPLY I

The only supply for the board is +5V. L1 and C1 through C18 provide required digital filtering.

A59 DIGITAL INTERFACE ASSEMBLY, TROUBLESHOOTING

CHECKING MICROPROCESSOR I/O ADDRESS STROBES (BLOCK A).

U12, U19, and U26 (Block **A**) are connected to the I/O address bus and generate 24 I/O strobes which are used either on this assembly or are sent via the motherboard to other assemblies. These strobes on the outputs of U12, U19, and U26 can be checked using the front panel to write directly to the I/O addresses (Direct I/O), while monitoring the outputs of the 3-to-8 line decoders. This can be done as follows: Press **[INSTR] [PRESET]**, then **[MANUAL]** sweep key. Connect a logic probe to the output that is to be checked. Enter into the front panel the corresponding I/O address. The I/O address is shown on the schematic printed above the outputs of U12, U19, and U26 in the following form: m,Rn: Where "m" is called the I/O CHANNEL and "n" is the I/O SUBCHANNEL. For example, assume that we wish to test U19 pin 7. The I/O address is 3,R3: This is entered into the front panel as follows: **[SHIFT] [GHz] [3] [Hz]** sets the I/O channel, and **[SHIFT] [MHz] [3] [Hz]** sets the I/O subchannel. Pressing **[SHIFT] [KHz]** activates the selected I/O address. Make entries by pressing the step keys, using the RPG, or by making data pad entries. Each entry will cause the M/N Oscillator Control strobe to be generated. This will be a LOW-True signal approximately 500 ns wide that can be monitored with the logic probe. It can also be seen on a storage scope.

Refer to Direct I/O Addressing in Section VIII, "Service Introduction", for more information.

CHECKING MICROPROCESSOR OUTPUT DEVICES (BLOCKS B, E, AND G)

The following devices are microprocessor output devices: U24 (Block **B**), U10 and U17 (Block **E**) and finally U23 (Block **G**). These can be checked using the front panel in a similar manner as above. To do this, the I/O channel and subchannel numbers must be entered at the front panel. These numbers can be found by reading the I/O address on the write input of the device. After the address has been entered, press **[SHIFT] [KHz]**. Number entries can now be made directly to the device you are interested in. Monitor the outputs at the same time you enter numbers which will affect the signals of interest. For example, if the signal of interest is taken from DB2 of the I/O data bus, enter the number 0 and observe the register output; it should go LOW. Then enter the number 4, and observe that DB2 goes HIGH. Note that if U16 is being checked, the outputs are only valid during the time the write strobe is LOW. Note that the instrument should be in MANUAL sweep mode so that the normal operation of the instrument does not cause the device being tested to be written to.

CHECKING MICROPROCESSOR INPUT DEVICES (BLOCKS F, AND H)

Input devices can be checked in a similar manner as the output devices. The front panel is used to set up the I/O channel and subchannel as before. U7 and U18 are the only input devices on this assembly. After setting the correct address on the front panel, press **[SHIFT] [Hz]**. Each time **[HZ]** is pressed, the instrument will read from the addressed I/O device and display the results in the entry display in both decimal and octal formats. By shorting each input of the input devices to +5V or ground, each input can be checked. Note that U18 is an inverting buffer so that a LOW at its input should appear as a HIGH at its output.

CHANGE DETECTORS (BLOCK C)

Connect a logic probe or storage scope to TP8 "CHGFF" (Block **C**). Observe that a LOW-True pulse is generated each time the rear panel Frequency Standard INT/EXT switch is switched. This should happen for both INT or EXT positions. Also note that the front panel EXT REF LED should go on when EXT is selected and off when INT is selected. The UNLOCKED input can be checked by putting the 8340A into CW and then disconnecting one of the snap on cables that is part of the phase-locked loop. This should cause a pulse at TP8 and also cause the front panel UNLOCKED LED to go on. Reconnecting the cable should make the LED go out. HOVC can be checked by unplugging the 8340A from the AC mains for five minutes and then quickly plugging it in and turning it on. The OVEN light should go on and then after a few minutes, the light should go off.

PROCESSOR SERVICE REQUEST (BLOCK H)

U18 can be checked out as indicated in the general troubleshooting of input devices. To check the basic function press the following front panel keys: **[INSTR PRESET] [CW]**. Note that the RUN light on the processor board should be out. If it is not, something is pulling down the LSRQ line, or U4D is not being set by the processor as it should. LSTP must be LOW for the processor run light to go out. NOTE: If the instrument is UNLOCKED due to some hardware problem, the processor will run continously, and in this case, LSTP should remain HIGH.

Note that by grounding the LBX test point on the Marker Bandcross board, TP6 should go HIGH, LSRQ should go LOW, and LSTP should go HIGH. By doing a direct READ using Direct I/O, U18 Bit 14 should appear HIGH in the entry display. This is done by pressing the following sequence: **[INSTR PRESET] [SHIFT] [GHz] [4] [HZ] [SHIFT] [MHZ] [3] [Hz] [SHIFT] [Hz]**. Note that the entry display will have two numbers, the one on the right will be in the form dddddd. This is an OCTAL (ie. base 8) number. The second digit from the LEFT

must be a 4, 6, or 7 in order for BIT 14 to be HIGH.

ISOLATING A PROBLEM BY REMOVING THE A59 DIGITAL INTERFACE BOARD

To help verify that the problem is on the A59 DIGITAL INTERFACE board, it may be useful to remove the A59 assembly and observe the instrument behavior. With A59 missing, the instrument should do the following:

1. Following Power On or Instrument Preset, Both Instrument Check lights should go off. All 16 self test leds on the processor board should go off.

2. When the POWER is turned to STANDBY and then ON, the instrument should do an Instrument Preset instead of restoring the prior state.

3. The OVEN annunciator should be on and the EXT. REF, UNLOCKED, SRQ and REMOTE annunciators should be off.

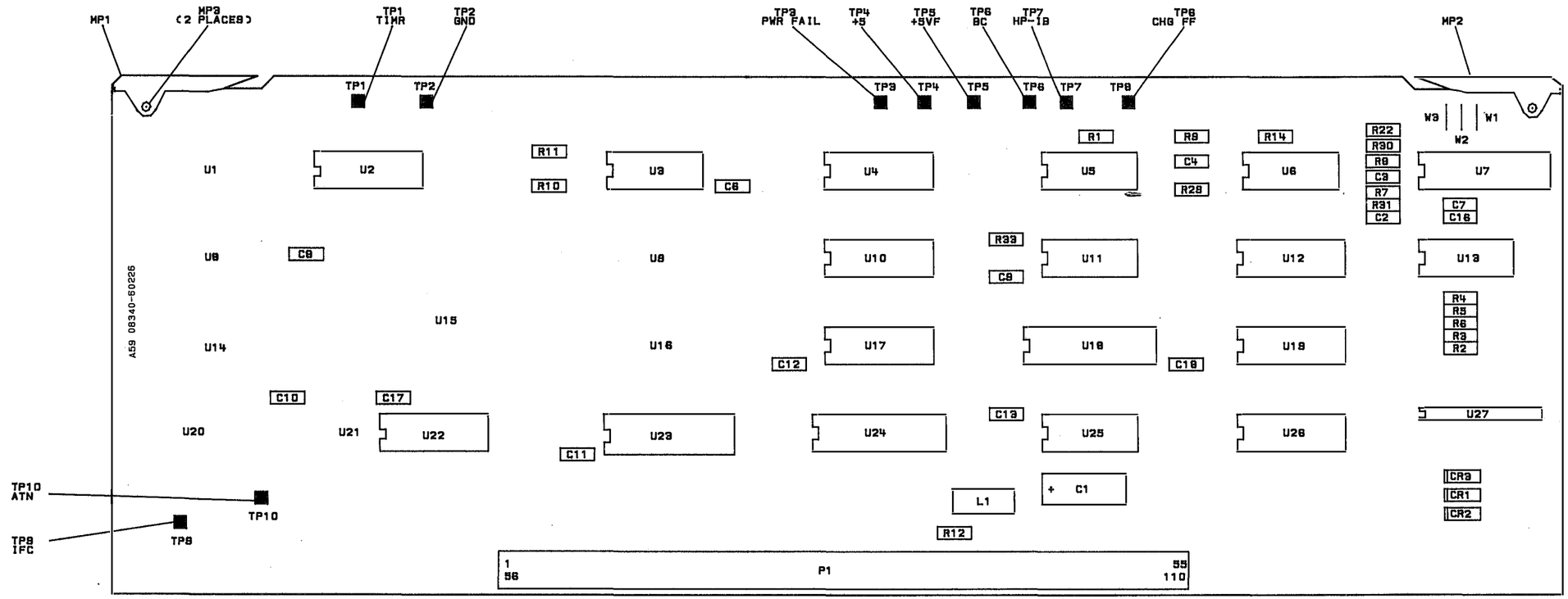


Figure 8G-5. A59 Digital Interface, Component Location Diagram

A59 Processor P1 Pin I/O (1 of 3)

Pin	Mnemonic	Levels	Source	Destination
1 56	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*J *J
2 57				
3 58				
4 59				
5 60				
6 61				
7 62				
8 63				
9 64				
10 65	HOVC LSTP	+3 VOLTS - OVEN WARM TTL (LOW TRUE)	A62J3-3 I	C XA6101-85 *
11 66	LYSP HSTD	TTL (LOW TRUE) TTL (HIGH TRUE)	G G	XA55P1-7 XA52P1-21
12 67	HCEN	TTL (HIGH TRUE)	G	XA55P1-14
13 68	HSP WPDAC	TTL (HIGH TRUE) TTL (LOW TRUE)	XA57P1-13 A	*B XA54P1-36
14 69	LIPS LBX	TTL (LOW TRUE) TTL (LOW TRUE)	XA52P1-36/A62J7-19 *	*I I
15 70	SIOA	TTL (LOW TRUE)	XA60P1-15	*NOT USED
16 71	SIOB	TTL (LOW TRUE)	XA60P1-16	*A
17 72	ADR0 HFILYO	TTL TTL	XA60P1-17 G	*A *XA58P1-47, 72
18 73	ADR2 ADR1	TTL TTL	XA60P1-18 XA60P1-73	*A *A
19 74	ADR4 ADR3	TTL TTL	XA60P1-19 XA60P1-74	*A *A

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A59 Digital Interface P1 I/O (2 of 3)

Pin	Mnemonic	Levels	Source	Destination
20 75	DB0 GND PLANE	TTL 0V	*D XA60P1-20 INSTRUMENT GROUND	*D E G *J
21 76	DB2 DB1	TTL TTL	*D XA60P1-21 *D XA60P1-76	*D E G *D E G
22 77	DB4 DB3	TTL TTL	*D F XA60P1-22 *D XA60P1-77	*D E G *D E G
23 78	DB6 DB5	TTL TTL	*D F XA60P1-23 *D F XA60P1-78	*D G *D E G
24 79	DB8 DB7	TTL TTL	*XA60P1-24 *D F XA60P1-79	*B D I *D G
25 80	DB10 DB9	TTL TTL	*XA60P1-25 *XA60P1-80	*B E I *B I
26 81	DB12 DB11	TTL TTL	*XA60P1-26 *XA60P1-81	*B E I *B E I
27 82	DB14 DB13	TTL TTL	*XA60P1-27 *XA60P1-82	*B E I *B E I
28 83	WSPTM DB15	TTL (LOW TRUE) TTL	A *XA60P1-83	XA58P1-28 *B E I
29 84	WRDAC WSPAT	TTL (LOW TRUE) TTL (LOW TRUE)	A A	XA58P1-29 XA58P1-84
30 85	WCDAC LRSP	TTL (LOW TRUE) TTL (LOW TRUE)	A G	XA54P1-28 XA58P1-85
31 86	M5 LMNE	TTL (HIGH TRUE) TTL (LOW TRUE)	E E	XA34P1-1 XA34P1-2
32 87	M3 M4	TTL (HIGH TRUE) TTL (HIGH TRUE)	E E	XA34P1-3 XA34P1-4
33 88	M1 M2	TTL (HIGH TRUE) TTL (HIGH TRUE)	E E	XA34P1-5 XA34P1-6
34 89	5 MHZ CLK LSRQ	TTL TTL (LOW TRUE)	XA60P1-34 *I	D *
35 90	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*NOT USED *NOT USED
36 91	+5.2V +12V	+5.2V +12V	XA52P1-17, 18, 41, 42 XA52P1-9, 33	*J *NOT USED
37 92	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*J *J

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A59 Digital Interface P1 I/O (3 of 3)

Pin	Mnemonic	Levels	Source	Destination
38	−15V	−15V	XA56P1-15, 30	*NOT USED
93	−5.2V	−5.2V	XA53P1-18, 36	*NOT USED
39	−10V	−10V	XA53P1-12, 13, 31, 32	*NOT USED
94	−10V	−10V	XA53P1-12, 13, 31, 32	*NOT USED
40	GND PLANE	0V	INSTRUMENT GROUND	*J
95	HPUP	TTL (HIGH TRUE)	XA52P1-46	*D
41	GND PLANE	0V	INSTRUMENT GROUND	*J
96	GND PLANE	0V	INSTRUMENT GROUND	*J
42	GND PLANE	0V	INSTRUMENT GROUND	*J
97	GND PLANE	0V	INSTRUMENT GROUND	*J
43	GND PLANE	0V	INSTRUMENT GROUND	*J
98	HXREF	TTL (HIGH TRUE)	A62J31-17	*C
44	GND PLANE	0V	INSTRUMENT GROUND	*J
99	WYOKW	TTL (LOW TRUE)	A	XA54P1-6
45	LCHNG	TTL (LOW TRUE)	*	C
100	TYOKP	TTL (LOW TRUE)	A	*
46	N5	TTL	E	XA34P1-11
101	N6	TTL	E	XA34P1-10
47	N3	TTL	E	XA34P1-13
102	N4	TTL	E	XA34P1-12
48	N1	TTL	E	XA34P1-15
103	N2	TTL	E	XA34P1-14
49	HULR	TTL (HIGH TRUE)	XA34P2-14	B
104	HULM	TTL (HIGH TRUE)	XA34P1-8	B
50	HULY	TTL (HIGH TRUE)	A62J2-16	B
105	HULH	TTL (HIGH TRUE)	A62J19-16	*B
51	HLEY	TTL (HIGH TRUE)	B	A62J2-3
106	HUL1	TTL (HIGH TRUE)	XA37P1-26; XA39P1-1, 16	B
52	LCK4	TTL (LOW TRUE)	A	*
107	HUL2	TTL (HIGH TRUE)	XA41P1-4	B
53	HLE2	TTL (HIGH TRUE)	B	*
108	LCK3	TTL (LOW TRUE)	A	XA43P1-19
54	LCK1	TTL (LOW TRUE)	A	XA42P1-19
109	LCK2	TTL (LOW TRUE)	A	XA42P1-1
55	GND PLANE	0V	INSTRUMENT GROUND	*J
110	GND PLANE	0V	INSTRUMENT GROUND	*J

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

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Delete **Block D** from *Figure 8G-6. A59 Digital Interface Schematic Diagram*

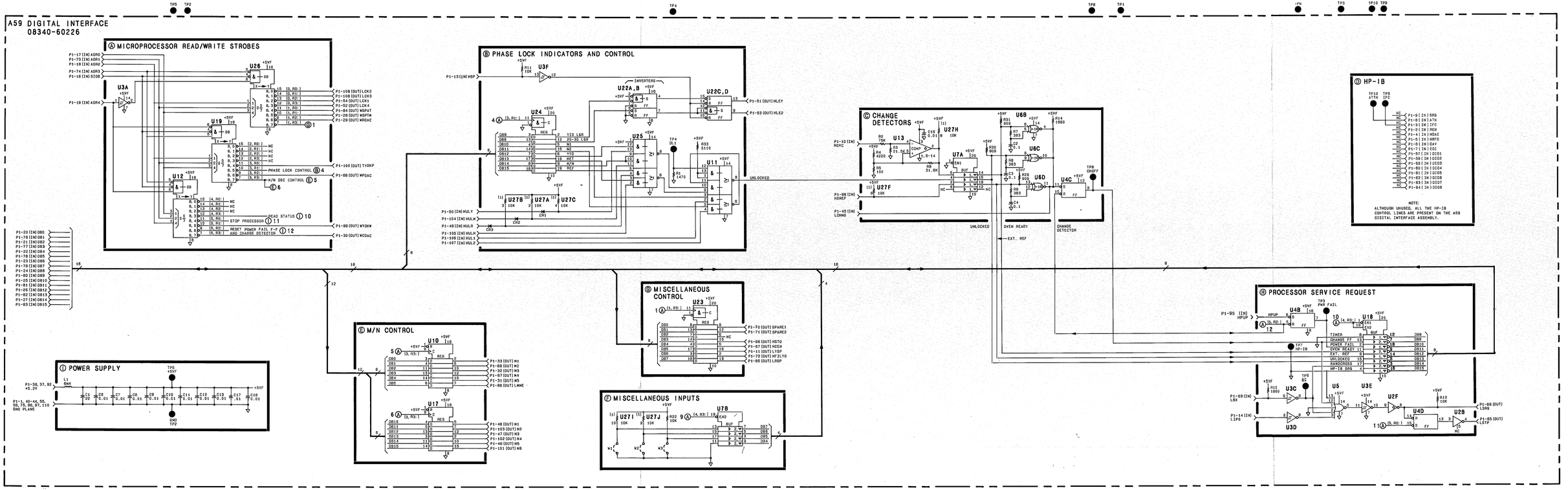


Figure 8G-6. A59 Digital Interface, Schematic Diagram

A60 PROCESSOR ASSEMBLY, TROUBLESHOOTING

INTRODUCTION

There are four levels of troubleshooting:

1. Self Test. The Self Test is run after switching the power on or pressing **[INSTR PRESET]**. Two front panel LEDs, INSTR CHECK I and II, give a visual indication of the Self Test results.
2. Input Signal Verification. This test checks several of the Processor's input signals. The Input Signal Verification should be performed prior to in-depth troubleshooting of the Processor.
3. Signature Analysis (SA). Signature analysis is used when Self Test fails to run or to verify a portion of the Self Test results. SA allows component level troubleshooting on the A60 Processor.
4. HP-IB Verification. This test allows verification of the HP-IB circuitry on the A60 Processor.

SELF TEST

Introduction

The Self Test is run after switching the power on or pressing **[INSTR PRESET]**. Self Test automatically performs Test Numbers 0 through 6 and 9 through 13 which are described in **SHIFT M4** below. Test Numbers 7 and 8 are also performed if the Desctructive RAM Test (descsribed below) is activated.

Three methods are available for viewing the results of Self Test. They are as follows:

- INSTR CHECK LEDs I and II
- A60 Processor Self Test LEDs
- SHIFT M4.

All three methods are described in the following paragraphs. Of the three methods, the most accurate is the A60 Processor Self Test LEDs. In the case of the INSTR CHECK LEDs and SHIFT M4, a failure could occur which would cause the failure indication to be invalid. When beginning to troubleshoot a Self Test failure, the failure indication given by the A60 Processor Self Test LEDs should be determined prior to any in-depth troubleshooting.

INSTR CHECK LEDs I and II

INSTR CHECK LEDs I and II, located on the front panel adjacent to the **[INSTR PRESET]** key, indicate the results of Self Test. After switching the power on or pressing **[INSTR PRESET]**, the following will occur:

1. Both LEDs will turn on.
2. LED I will be turned off when it is determined that the processor, memory, and Peripheral Interface Timer on the A60 Processor are operating (SHIFT M4 Test Numbers 0 through 6, 10 and 11).
3. LED II will be turned off when it is determined that the I/O Address Bus, I/O Data Bus, and the Marker RAM are operating (SHIFT M4 Test Numbers 9, 12, and 13).

If no failure occurs during Self Test, both INSTR CHECK LEDs will be turned off after approximately 1 second. If either of these LEDs remain on, examine the 16 LEDs on the A60 Processor assembly. Note that it is possible for a failure to occur which would cause both INSTR CHECK LEDs to go off when they shouldn't. This failure can be confirmed by examining the LEDs on the A60 Processor.

A60 Processor Self Test LEDs

The 16 A60 Processor Self Test LEDs, located on top of the A60 Processor assembly, give the most accurate indication of the Self Test results. After switching the power on or pressing **[INSTR PRESET]**, all 16 LEDs will turn on. If no failure occurs during the Self Test, all 16 LEDs will turn off after approximately 1 second (NOTE: If all sixteen LEDs remain on, immediately refer to the Signature Analysis troubleshooting below). If a failure does occur, the following will happen:

1. All 16 LEDs will initially turn on.
2. A60DS15 and A60DS16 (closest to the front of the instrument) will turn OFF, indicating that Self Test is in its first two seconds of operation. A60DS1 through A60DS14 will then indicate what failure occurred (see Table 8G-1).
3. A60DS9 through A60DS15 will turn OFF and A60DS16 will turn ON, indicating that Self Test is in its second two seconds of operation. A60DS1 through A60DS8 will then indicate which I/O Address Bus line failed (see Table 8G-1).
4. After step 3 above is complete, A60DS1 through A60DS16 will indicate which I/O Data Bus line failed (see Table 8G-1).

Table 8G-1. LED Indication When Self Test Fails

A60 Processor Self Test LEDs (Time After Power On or [INSTR PRESET])				
A60 Processor LED	First 2 Seconds		Second 2 Seconds	Afterward
	SHIFT M4 Test #	Test Name	I/O Address Bus Test	I/O Data Bus Test
DS1	0	PROCESSOR	ADR0	DB0
DS2	1	ROM U37	ADR1	DB1
DS3	2	ROM U36	ADR2	DB2
DS4	3	ROM U35	ADR3	DB3
DS5	4	ROM U34	ADR4	DB4
DS6	5	RAM U39	SIOA	DB5
DS7	6	RAM U38	SIOB	DB6
DS8	7	EEROM U33	SIOA	DB7
DS9	8	EEROM U32	OFF	DB8
DS10	9	MKR BX RAM	OFF	DB9
DS11	10	TMR LEDS U4	OFF	DB10
DS12	11	TMR U4	OFF	DB11
DS13	12	I/O ADRS	OFF	DB12
DS14	13	I/O DATA	OFF	DB13
DS15		OFF	OFF	DB14
DS16		OFF	ON	DB15

If Self Test fails, Self Test should be re-initiated by either cycling the line power or pressing **[INSTR PRESET]**. While Self Test is running, the A60 Processor Self Test LEDs should be examined to determine where the failure occurred. After the failure mode has been determined, read the corresponding Test Number description given in SHIFT M4 below. The description indicates what circuitry was tested (i.e., failed) and will assist in isolating the failure.

Destructive RAM Test

NOTE

This test should only be activated if a failure has occurred with the instrument state Save/Recall registers or the calibration data has been defaulted (CAL FAULT) or is continually exhibiting incorrect values.

The Destructive RAM Test serves two purposes; the first is to exhaustively test RAM and the second is to completely verify the operation of EE-PROM. This test is normally not performed during Self Test due to the limited write lifetime of EE-PROM and also because **it totally erases the instrument state Save registers in RAM.** If this test is activated during Self Test, the Self Test results will now also indicate the condition of EE-PROM (not done during normal Self Test) and also if RAM failed in a mode which was not detected during the normal Self Test.

To activate the Destructive RAM test, perform the following:

1. Connect a jumper from A60TP1 (RAM) to A60TP7 (GND).
2. Cycle the line power or press **[INSTR PRESET]**.
3. Remove the jumper installed in step 1 upon completion of Self Test.

Performing steps 1 and 2 above will cause the Destructive RAM Test to be peformed during Self Test. To determine if a failure has occurred, examine the A60 Processor Self Test LEDs as described above. Note that if a failure occurs in RAM, the EE-PROM will not be tested. The EE-PROM test requires that the RAM test passes before it will be performed.

SHIFT M4

Press **[SHIFT] [M4]** activates a service diagnostic which tests the DACS and control circuitry on the A27 Level Control, A28 SYTM Driver, A57 Marker Bandcross, and A58 Sweep Generator. This diagnostic routine also allows the results of the Self Test to be displayed in the front panel ENTRY DISPLAY.

The DAC tests which are performed are not exhaustive (a small error will not generate a failure indication). However, if a test does fail, the indication should direct troubleshooting to a specific device or circuit path.

While the tests are running, the front panel ENTRY DISPLAY will display "DIAGNOSTIC TESTS IN PROGRESS." Upon completion of the tests, "TEST: ? FULL DIAGNOSTIC" and then PASS or FAIL will be displayed. Pass indicates that all of the tests related to this diagnostic passed. Fail indicates that one or more of the tests failed. If the indication is FAIL, use the RPG or step keys to view the test results and determine which test(s) failed. The tests which are run are shown in Table 8G-3 below.

Of the 32 tests performed by the SHIFT M4 diagnostic routine, only one test (Test #0, PROCESSOR TST) is not dependent upon the test results of one or more of the other tests. Table 8G-2 below shows this inter-dependency. The vertical axis (Test #) in this table lists the test numbers from 0 through 31. The horizontal axis (Test Dependency) lists the test numbers again and indicates which tests must pass for a specific test result to be valid. An "X" in the Test Dependency column indicates that the specific Test # is valid only if the test in that column passed. For example, Test #9 (vertical axis) is only valid if Test #s 0, 5, and 6 (horizontal axis) indicate a PASS. If test number 9 failed, first verify that tests 0, 5, and 6 passed before troubleshooting the circuitry exercised by this test.

Table 8G-2. Test Number vs Test Dependency

Test #	Test Dependency (Test #)											
	0	5	6	9	11	12	13	14	15	17	20	31
0												
1	X											
2	X											
3	X											
4	X											
5	X											
6	X											
7	X	X	X									
8	X	X	X									
9	X	X	X			X	X					
10	X	X	X									
11	X	X	X									
12	X	X	X									
13	X	X	X									
14	X	X	X			X	X	X				
15	X	X	X			X	X	X				X
16	X	X	X			X	X	X	X			X
17	X	X	X			X	X	X	X			X
18	X	X	X			X	X	X	X			X
19	X	X	X			X	X	X	X			X
20	X	X	X			X	X	X				X
21	X	X	X			X	X	X	X			X
22	X	X	X			X	X	X	X			X
23	X	X	X			X	X	X	X			X
24	X	X	X			X	X	X	X			X
25	X	X	X			X	X	X	X			X
26	X	X	X			X	X	X	X			X
27	X	X	X			X	X	X	X			X
28	X	X	X			X	X	X	X			X
29	X	X	X	X	X	X	X	X		X	X	X
30												
31	X											

NOTE

The results displayed for Tests 0 through 13 are the stored results of Self Test, which is run at power on and after an [INSTR PRESET].

Table 8G-3. Tests Performed by the SHIFT M4 Diagnostic (1 of 3)

Number	Name	Description
0	PROCESSOR TST	Verifies the operation of the Processor (A60 Block E), the Free Run DSA (A60 Block F), A60U25A, A60U25D, the processor's data and address bus, and a portion of the UV-EROM (A60 Block A) and A60U29.
1	ROM 1 CKSUM	Verifies the operation (checksum) of A60U37.
2	ROM 2 CKSUM	Verifies the operation (checksum) of A60U36.
3	ROM 3 CKSUM	Verifies the operation (checksum) of A60U35.
4	ROM 4 CKSUM	Verifies the operation (checksum) of A60U34.
5	RAM 1 RD/WR	Verifies the operation (read/write) of A69U39 and a portion of A60U29.
6	RAM 2 RD/WR	Verifies the operation (read/write) of A69U38 and a portion of A60U29.
7	EEROM 1 RD/WR	Verifies the operation (read/write) of A60U33 and a portion of A69U29. Note that this test is only performed if A60TP1 RAM is grounded (initiates the Destructive RAM test).
8	EEROM 2 RD/WR	Verifies the operation (read/write) of A60U32 and a portion of A60U29. Note that this test is only performed if A60TP1 RAM is grounded (initiates the Destructive RAM test).
9	MKR RAM RD/WR	Verifies the operation (read/write) of the Address Register (A57 Block A), the Sweep Event Memory (A57 Block B), the Read/Write RAM Buffer (A57 Block C), and the Microprocessor Read/Write Strobes (A57 Block K).
10	PIT (LED Registers)	Verifies the operation of A60U4 and a portion of A60U29.
11	PIT RESPONDS	Verifies the operation of A60U4 and a portion of A60U29.
12	I/O ADDR BUS	Verifies the operation of the I/O address Bus (A60 Block K), A60U22, the I/O Address bus, and a portion of the I/O Decoding and Control (A60 Block J) and A60U29.
13	I/O DATA BUS	Verifies the operation of the I/O Data Bus Buffers (A60 Block P), A60U14, A60U16, the I/O Data Bus, and a portion of the I/O Decoding and Control (A60 Block J) and A60U29.
14	A-D CONVERTER	Verifies the operation of the ADC Control Latch (A27 Block L), the ADC Clock/Control (A27 Block M), the ADC Input Multiplexer (A27 Block N), the Test ADC (A27 Block O), the ADC Window Comparator (A27 Block P), the Conversion Complete Timer/SRQ Latch (A27 Block Q), and the Status Buffer (A27 Block R). The Address Decoding (A27 Block B) is partially verified.

Table 8G-3. Tests Performed by the SHIFT M4 Diagnostic (2 of 3)

Number	Name	Description
15	LEVEL REF DAC	Verifies the operation of the ALC Reference Generator (A27 Block H) and a portion of the Address Decoding (A27 Block B). Monitors LVL (A27 Block H output) to determine the test results.
16	MAN SWP DAC	Verifies the operation of the Manual Sweep Dac (A57 Block G) and a portion of the Microprocessor And Read Write Strobes (A57 Block K). Monitors LVL SWP (A27 Block I output) to determine the test results.
17	MARKER RAMP	Verifies the operation of the A58 Sweep Generator assembly. Monitors BVSWP (A58 Block O Output) to determine the test results.
18	RESET DAC	Verifies the operation of the A58 Sweep Generator assembly. This test specifically exercises the Reset DAC (A57 Block C) and monitors BVSWP (A58 Block O output) to determine the test results.
19	LEVEL SWP DAC	Verifies the operation of the Power Sweep Generator (A27 Block I) and a portion of the Address Decoding (A27 Block B). Monitors LVL SWP (A27 Block I output) to determine the test results.
20	BND CROSS DAC	Verifies the operation of the Sweep Comparator (A57 Block D) and a portion of A57U24 and A57U28. Monitors CMP (A57 Block I input) to determine the test results.
21	SWP WIDTH DAC	Verifies the operation of the A58 Sweep Generator assembly. This test specifically exercises the Sweep Width DAC (A58 Block M) and monitors BVSWP (A58 Block O output) to determine the test results.
22	SWP RANGE ATN	Verifies the operation of the A58 Sweep Generator assembly. This test specifically exercises the Sweep Width Register (A58 Block E) and monitors BVSWP (A58 Block O output) to determine the test results.
23	V/GHz CIRCUIT	Verifies the operation of the −0.25 V/GHz circuitry (A28 Block E) and a portion of the Programmable Scalar (A28 Block D) and the Digital Control (A28 Block I). Monitors −.25 V/GHz (A28 Block E output) to determine the test results.
24	V/GHz BND ATN	Verifies the operation of the Programmable Scalar (A28 Block D), A28U19 and a portion of A28U16. Monitors −.25 V/GHz (A28 Block E output) to determine the test results.
25	BRK PNT 1 DAC	Verifies the operation of the 9 GHz Breakpoint Slope Compensation (A27 Block D), the Compensation Summing Amplifier (A27 Block G), and a portion of the Address Decoding (A27 Block B). Monitors LVL COR (A27 Block G output) to determine the test results.

Table 8G-3. Tests Performed by the SHIFT M4 Diagnostic (3 of 3)

Number	Name	Description
26	BRK PNT 2 DAC	Verifies the operation of the 20 GHz Breakpoint Slope Compensation (A27 Block C), the Compensation Summing Amplifier (A27 Block G), and a portion of the Address Decoding (A27 Block B). Monitors LVL COR (A27 Block G output) to determine the test results).
27	ATN SLOPE DAC	Verifies the operation of the Attenuator Slope Compensation (A27 Block E), the Compensation Summing Amplifier (A27 Block G), and a portion of the Address Decoding (A27 Block B). Monitors LVL COR (A27 Block G output) to determine the test results.
28	YO PRETUN DAC	Verifies the operation of the Pretune Register (A54 Block A), the Pretune DAC (A54 Block B), and the Summing Amplifier (A54 Block C). Monitors −.25 V/GHz (A28 Block E output) to determine the test results.
29	SWEEPTIME DAC	Verifies the operation of the A58 Sweep Generator assembly. This test specifically exercises the Sweep Time DAC (A58 Block G) and uses the A57 Marker Bandcross assembly and the PIT (A60U4) to determine the test results.
30	NOT USED	
31	A27 INSTALLED	Verifies that the A27 Level Control Assembly is installed.

INPUT SIGNAL VERIFICATION

The purpose of the Input Signal Verification is to determine if a Self Test failure is being caused by the A60 Processor assembly rather than one of the other assemblies in the instrument. this verification should be performed if Self Test fails to run (i.e., the A60 Processor Self Test LEDs turn on and remain on) or Self Test runs and the results indicate a failure on the A60 Processor assembly (i.e., Test Number 0 through 8, 10 or 11), described in SHIFT M4 above, is the indicated failure). It should also be performed prior to in-depth troubleshooting of the A60 Processor.

The verification consists of measuring all of the input signals to the A60 Processor in addition to a few key signals which are required for Self Test to run. To perform the measurements, the A60 Processor assembly should be placed on an extender board and A60TP7 (GND) or A60TP17 (GND) used as the reference.

Procedure

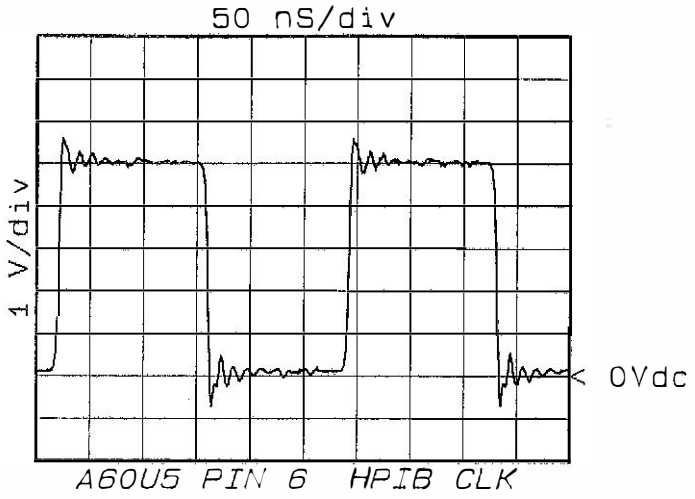
NOTE

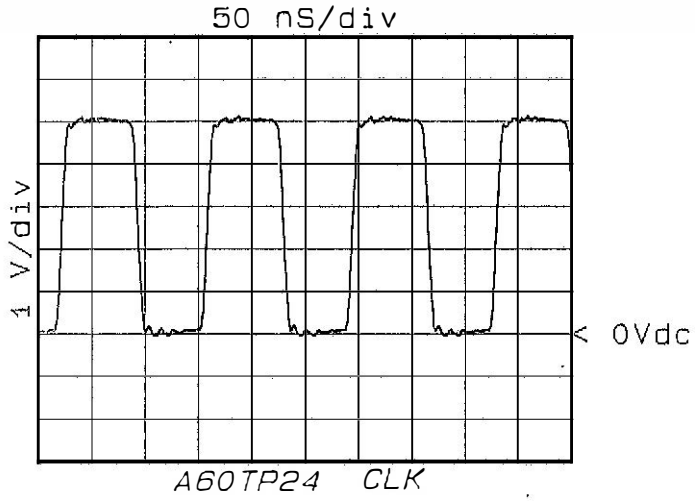
A60 Processor is a static sensitive assembly. Repair of this assembly should be performed at an anti-static work station.

1. Switch the line power off, remove the A60 Processor assembly, place the assembly onto an extender board and re-install it into the instrument.
2. Switch the power line on.
3. Using a DVM or an oscilloscope, measure the following points and verify that the voltages are correct.

A60TP11 (LSTP) – +5V
A60TP21 (+5V) – +5V
A60TP22 (HRAMPUP) – +5V
A60TP23 (LRESET) – +5V
A60P1-33 (Vpp) – +4.5V
A60U38 Pin 23 (VRAM) – +5V
A60U1 Pin 8 (VREF) – +1.2V
+5PF – +5V

4. Using an oscilloscope, verify that the following waveforms are correct.





SIGNATURE ANALYSIS

Signature Analysis described in this section is for component level troubleshooting of the A60 Processor assembly. It should be used when Self Test fails to run (i.e., when the Self Test LEDs turn on and remain on) and after the Input Verification procedure has been performed. The signatures given below in Figure 8G-7 are used to test the address decoding circuitry which is required for Self Test to run. This test does not verify the operation of the microprocessor's data bus, the UV-EPROM, nor does it completely verify the operation of the microprocessor. If all of the signatures are found to be correct, the Self Test failure is due to one of these items.

Procedure

1. Switch the instrument's POWER switch to STANDBY.
2. Remove the A60 Processor assembly from the instrument and then remove A60U40 from the assembly.
3. Place the A60 assembly onto an extender board and re-install it into the instrument.
4. Attach a jumper wire from A60TP15 (LSA) to A60TP17 (GND).
5. Connect an HP 5005A Signature Multimeter (or equivalent) to the A60 Processor as follows:

   START – A60TP16 (RS)
   STOP – A60TP16 (RS)
   CLOCK – A60TP24 (CLK)
   GND – A60TP7 (GND)

   Set the START for falling edge triggering and both the STOP and CLOCK for rising edge triggering. Set the THRESHOLD for TTL.
6. Verify the signatures given in Figure 8G-7 and troubleshoot as appropriate.
7. When troubleshooting is complete, remember to re-install A60U40.

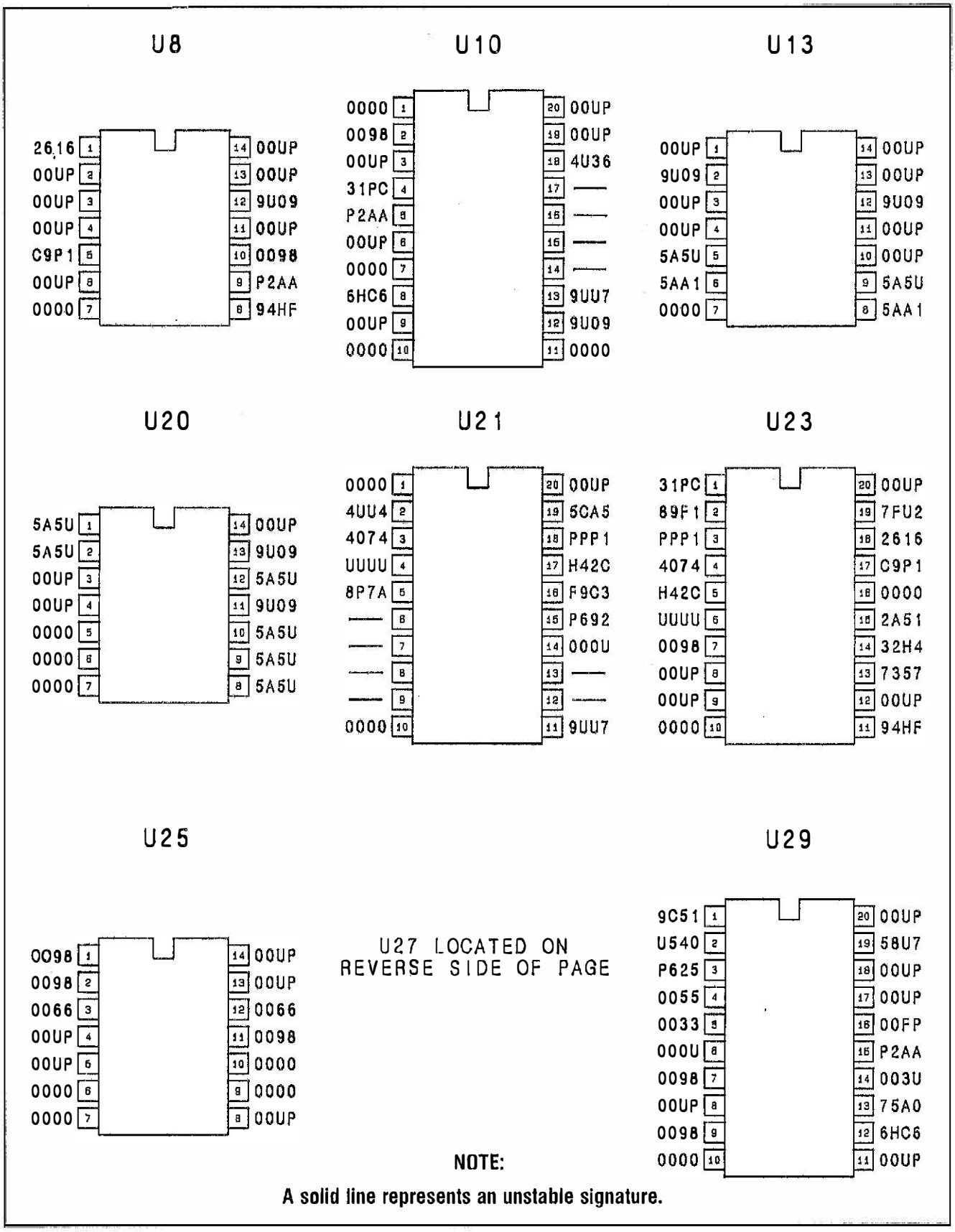


Figure 8G-7. A60 Processor Signatures (1 of 2)

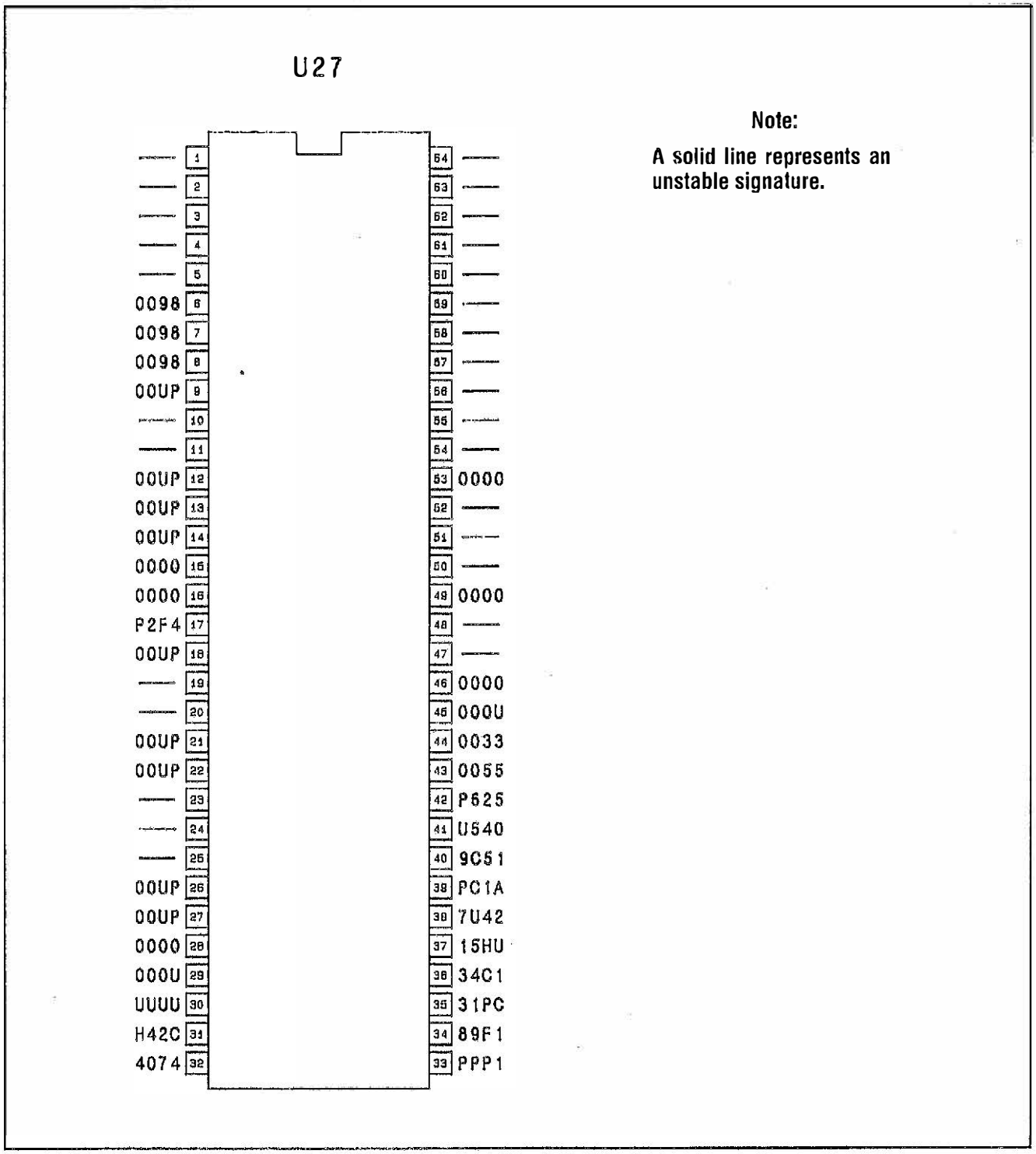


Figure 8G-7. A60 Processor Signatures (2 of 2)

HP-IB VERIFICATION

The HP-IB circuitry consists of the HP-IB Interface (A60 Block G). This circuitry is connected to the rear panel HP-IB connector (J21) via a ribbon cable (J21W1, part of the connector) and the HP-IB Bus on the A62 Motherboard.

The HP-IB operation of the instrument can be verified by performing the HP-IB Verification in the Performance Test section, Volume 1, Section IV. Failure to pass this verification can only be caused by the circuitry and interconnects mentioned above.

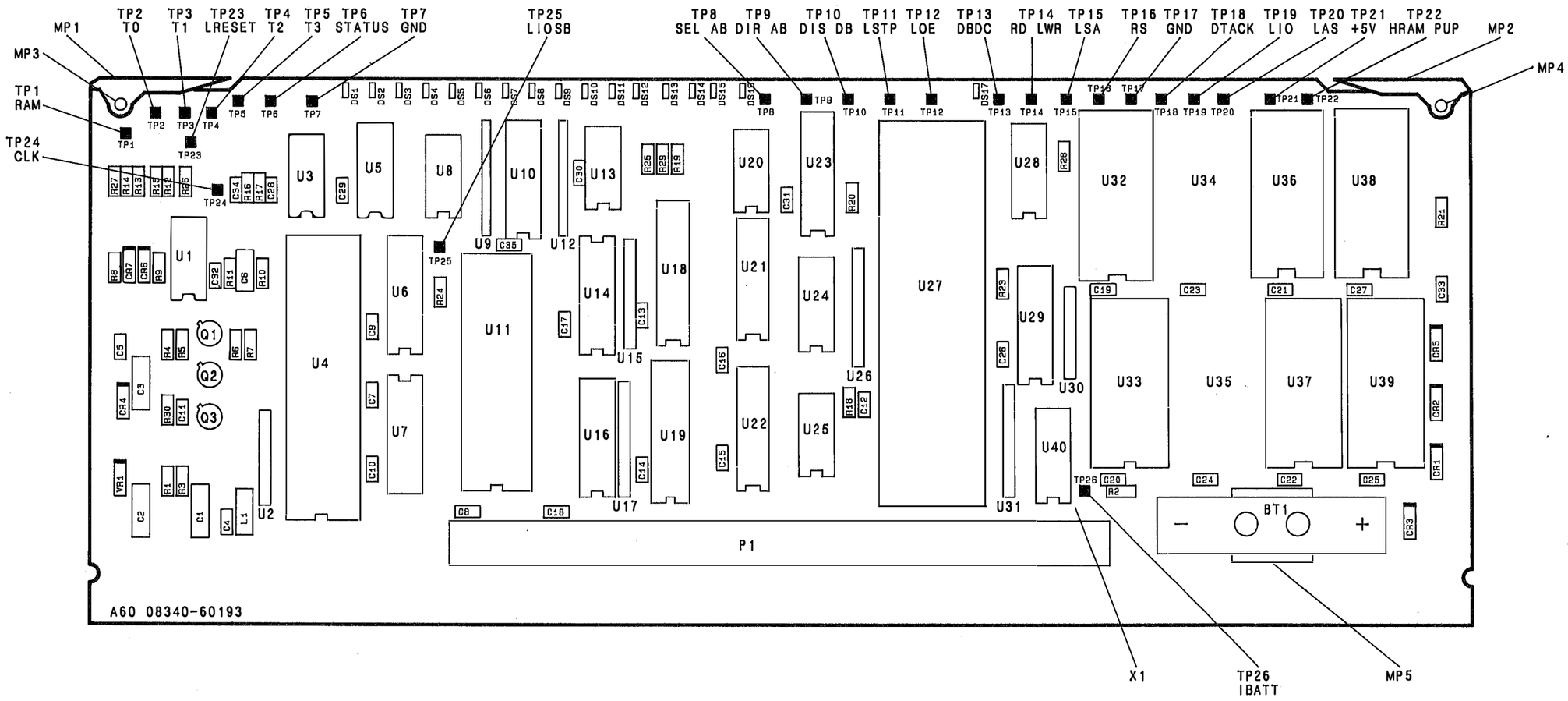


Figure 8G-11. A60 Processor, Component Location Diagram

A60 Processor P1 Pin I/O (1 of 3)

Pin	Mnemonic	Levels	Source	Destination
1 56	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*L *L
2 57	REN DI01	TTL (LOW TRUE) TTL	A62J7-10 D	D A62J7-1
3 58	IFC DI02	TTL (LOW TRUE) TTL	A62J7-17 D	D A62J7-3
4 59	NDAC DI03	TTL TTL	D D	A62J7-15 A62J7-5
5 60	NRFD DI04	TTL TTL	D D	A62J7-13 A62J7-7
6 61	DAV DI05	TTL TTL	D D	A62J7-11 A62J7-2
7 62	EOI DI06	TTL TTL	D D	A62J7-9 A62J7-4
8 63	ATN DI07	TTL TTL	D D	A62J7-21 A62J7-6
9 64	SRQ DI08	TTL TTL	A62J7-19 D	D A62J7-8
10 65	LSTP	TTL (LOW TRUE)	XA59P1-65	D A62J1-43
11 66				
12 67				
13 68				
14 69	LIPS	TTL (LOW TRUE)	XA52P1-36/A62J1-19	*E
15 70	SIOA GND PLANE	TTL (LOW TRUE) 0V	*G INSTRUMENT GROUND	*J *L
16 71	SIOB GND PLANE	TTL (LOW TRUE) 0V	*G INSTRUMENT GROUND	*J *L
17 72	ADR0 GND PLANE	TTL 0V	*G INSTRUMENT GROUND	*J *L
18 73	ADR2 ADR1	TTL TTL	*G *G	*J *J
19 74	ADR4 ADR3	TTL TTL	*G *G	*J *J

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A60 Processor P1 Pin I/O (2 of 3)

Pin	Mnemonic	Levels	Source	Destination
20 75	DB0 GND PLANE	TTL 0V	*J K I INSTRUMENT GROUND	*I K *L
21 76	DB2 DB1	TTL TTL	*I K *I K	*I K *I K
22 77	DB4 DB3	TTL TTL	*I K *I K	*I K *I K
23 78	DB6 DB5	TTL TTL	*I K *I K	*I K *I K
24 79	DB8 DB7	TTL TTL	*J K I *I K	*I K *I K
25 80	DB10 DB9	TTL TTL	*J K I *J K I	*I K *I K
26 81	DB12 DB11	TTL TTL	*J K I *J K I	*I K *I K
27 82	DB14 DB13	TTL TTL	*J K I *J K I	*I K *I K
28 83	DB15	TTL	*J K I	*I K
29 84				
30 85				
31 86				
32 87				
33 88				
34 89	5 MHZ CLK LSRQ	TTL TTL (LOW TRUE)	B *	C F XA59P1-34 *I
35 90	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*NOT USED *NOT USED
36 91	+5.2V +12V	+5.2V +12V	XA52P1-17, 18, 41, 42 XA52P1-9, 33	*L *L
37 92	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*L *L

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A60 Processor P1 Pin I/O (3 of 3)

Pin	Mnemonic	Levels	Source	Destination
38	−15V	−15V	XA56P1-15, 30	*NOT USED
93	−5.2V	−5.2V	XA53P1-18, 36	*L
39	−10V	−10V	XA53P1-12, 13, 31, 32	*NOT USED
94	−10V	−10V	XA53P1-12, 13, 31, 32	*NOT USED
40	GND PLANE	0V	INSTRUMENT GROUND	*L
95	HPUP	TTL (HIGH TRUE)	XA52P1-46	*NOT USED
41	GND PLANE	0V	INSTRUMENT GROUND	*L
96	GND PLANE	0V	INSTRUMENT GROUND	*L
42	GND PLANE	0V	INSTRUMENT GROUND	*L
97	GND PLANE	0V	INSTRUMENT GROUND	*L
43	GND PLANE	0V	INSTRUMENT GROUND	*L
98	GND PLANE	0V	INSTRUMENT GROUND	*L
44	GND PLANE	0V	INSTRUMENT GROUND	*L
99	GND PLANE	0V	INSTRUMENT GROUND	*L
45	HSTM	TTL (HIGH TRUE)	H	XA61P1-45
100	GND PLANE	0V	INSTRUMENT GROUND	*L
46	LSOB	TTL (LOW TRUE)	H	XA61P1-46
101	LWRT	TTL (LOW TRUE)	H	XA61P1-101
47	LIDA14	TTL (LOW TRUE)	I	XA61P1-47
102	LIDA15	TTL (LOW TRUE)	I	XA61P1-102
48	LIDA12	TTL (LOW TRUE)	I	XA61P1-48
103	LIDA13	TTL (LOW TRUE)	I	XA61P1-103
49	LIDA10	TTL (LOW TRUE)	I	XA61P1-49
104	LIDA11	TTL (LOW TRUE)	I	XA61P1-104
50	LIDA8	TTL (LOW TRUE)	I	XA61P1-50
105	LIDA9	TTL (LOW TRUE)	I	XA61P1-105
51	LIDA6	TTL (LOW TRUE)	I	XA61P1-51
106	LIDA7	TTL (LOW TRUE)	I	XA61P1-106
52	LIDA4	TTL (LOW TRUE)	I	XA61P1-52
107	LIDA5	TTL (LOW TRUE)	I	XA61P1-107
53	LIDA2	TTL (LOW TRUE)	I	XA61P1-53
108	LIDA3	TTL (LOW TRUE)	I	XA61P1-108
54	LIDA0	TTL (LOW TRUE)	I	XA61P1-54
109	LIDA1	TTL (LOW TRUE)	I	XA61P1-109
55	GND PLANE	0V	INSTRUMENT GROUND	*L
110	GND PLANE	0V	INSTRUMENT GROUND	*L

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A60 PROCESSOR
08340-60193

Ⓐ UV-EPROM

Ⓑ CLOCK

Ⓒ INTERRUPT ENCODER

Ⓓ TIMER/SELF-TEST INDICATOR/ DSA/MISC IO

Ⓔ PROCESSOR

Ⓕ FREE RUN DSA

Ⓖ HP-IB INTERFACE (SEE NOTE 2)

Ⓗ EE-PROM

Ⓘ MEMORY DECODING

Ⓙ I/O DECODING AND CONTROL

Ⓚ I/O ADDRESS BUS

Ⓛ RAM

Ⓜ POWER SUPPLIES

Ⓝ POWER UP/STOP

Ⓟ SELFTEST

Ⓟ I/O DATA BUS BUFFERS

NOTES

1. THESE SIGNALS ARE CONNECTED TO ASOPS FOR FACTORY ON BOARD PROGRAMMING CAPABILITY. THESE SIGNALS ARE NOT CONNECTED ANYWHERE ELSE IN THE INSTRUMENT.
2. ALTHOUGH UNUSED, ALL THE HP-IB CONTROL LINES ARE PRESENT ON THE A60 DIGITAL INTERFACE ASSEMBLY.

Figure 8G-12. A60 Processor, Schematic Diagram

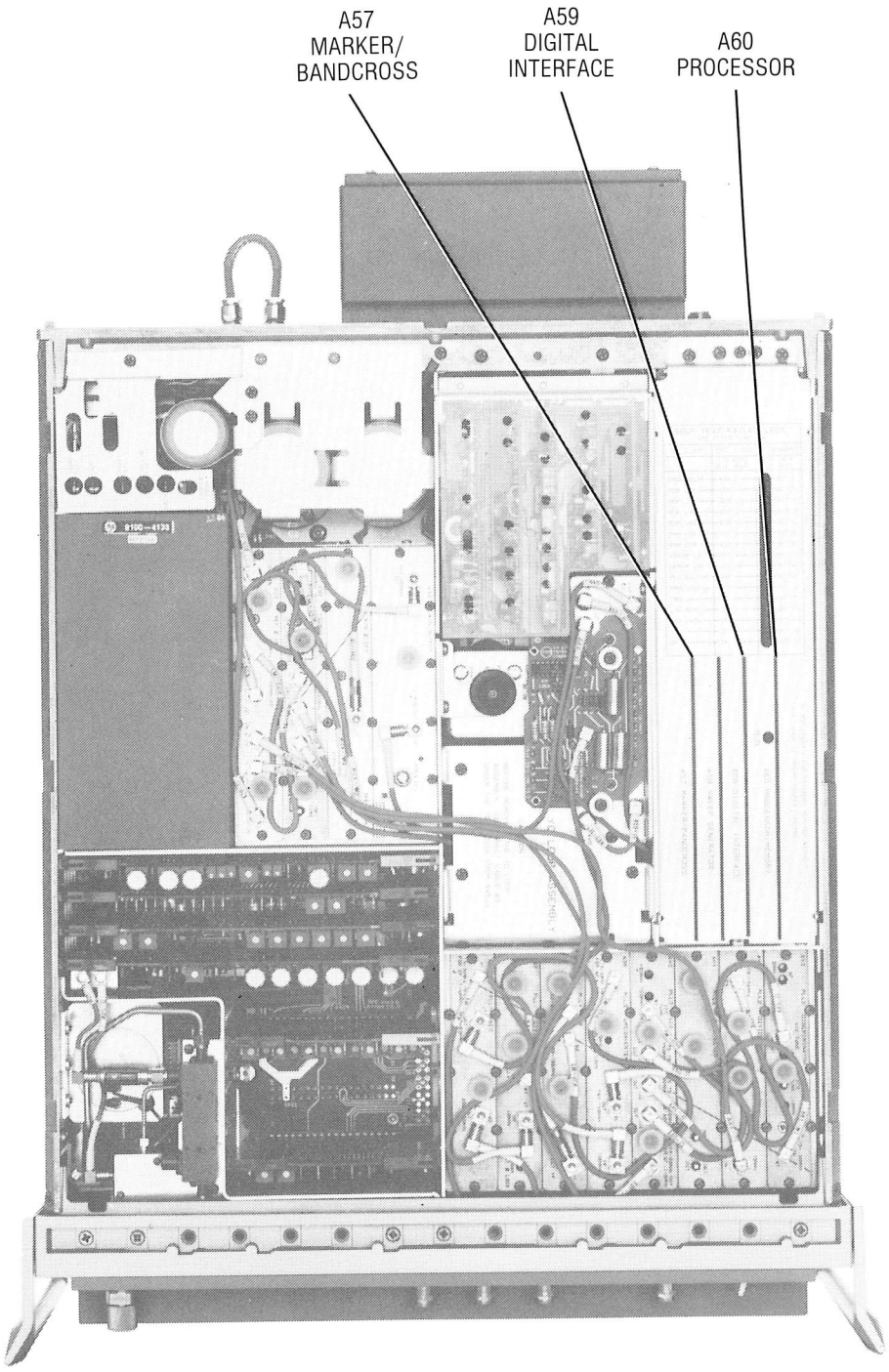
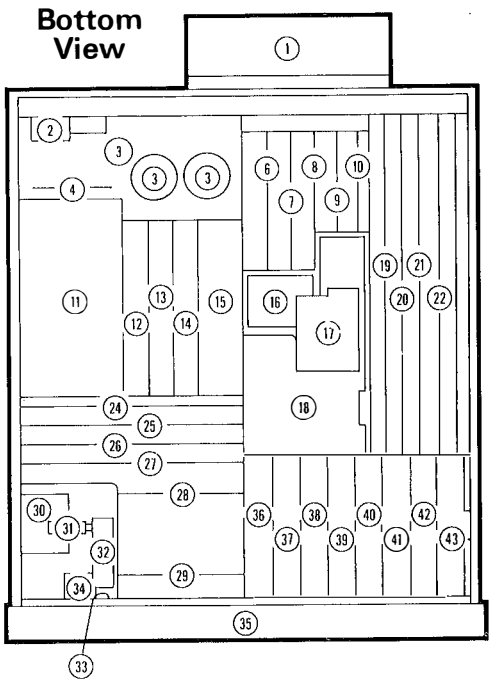
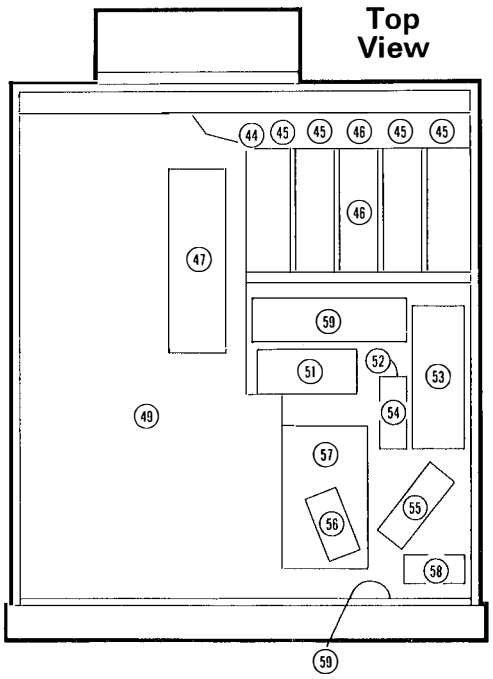


Figure 8G-16. Controller Section Major Assemblies Location Diagram

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 3					Volume 4		
			Ref.-M/N Loops	20-30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	33					•			
A2	Display Driver	33					•			
A3	Display Processor	33					•			
A4	Not Assigned	-								
A5	Keyboard	35					•			
A6	Keyboard Interface	35					•			
A7	Lower Keyboard	35					•			
A8	3.7 GHz Oscillator	57						•		
A9	Band 0 Pulse Modulator	56						•		
A10	Directional Coupler	32						•		
A11	Band 1-4 Detector	31						•		
A12	Band 0 Splitter/Detector	34						•		
A13	SYTM (Switched YIG Tuned Multiplier)	30						•		
A14	Band 1-4 Power Amplifier	53						•		
A15	Band 0 Low Pass Filter	52						•		
A16	Band 1-4 Modulator/Splitter	51						•		
A17	Band 0 Mixer	54						•		
A18	Band 0 Power Amplifier	55						•		
		60						•		
A19	Capacitor Assembly	48								•
A20	RF Section Filter	50						•		
A21	Pulse Modulator Driver	29						•		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						•		
A25	ALC Detector	27						•		
A26	Linear Modulator	26						•		
A27	Level Control	25						•		
A28	SYTM Driver	24						•		
A29	Reference Phase Detector	12	•							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	•							
A31	M/N Phase Detector	14	•							
A32	M/N VCO (Voltage Controlled Osc.)	15	•							
A33	M/N Output	15	•							
A34	Reference-M/N Motherboard	5	•							
A35	Rectifier	4								•
A36	PLL1 VCO (Voltage Controlled Osc.)	36		•						
A37	PLL1 Divider	37		•						
A38	PLL1 IF	38		•						
A39	PLL3 Upconverter	39		•						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		•						
A41	PLL2 Phase Detector	41		•						
A42	PLL2 Divider	42		•						
A43	PLL2 Discriminator	43		•						
A44	YIG Oscillator (YO)	18			•					
A45	Directional Coupler	18			•					
A46	7 GHz Low Pass Filter	18			•					
A47	Sense Resistor Assembly (YO circuit)	47			•					
	(SYTM circuit)	47						•		
A48	YO Loop Sampler	18			•					
A49	YO Loop Phase/Detector	18			•					
A50	YO Loop Interconnect	17			•					
A51	Reference Oscillator	16	•							
A52	Positive Regulator	6								•
A53	Negative Regulator	7								•
A54	YO Pretune/Delay Compensation	8			•					
A55	YO Driver	9			•					
A56	–15V Regulator	10								•
A57	Marker/Bandcross	19					•			
A58	Sweep Generator	20			•					
A59	Digital Interface	21					•			
A60	Processor	22					•			
A61	Not Assigned	23					•			
A62	Motherboard	49				•				
A63	90 dB RF Attenuator	59						•		
AT1	Peripheral Mode Isolator	58						•		
AT2	15 dB Attenuator	18			•					
B1	Fan Assembly	1								•
A62C1-3	Power Supply Filter Capacitors	3								•
FL1	AC Line Module	2								•
A62Q1-4	Power Supply Regulating Transistors	45								•
A62S1	Power Supply Thermal Switch	44								•
T1	Power Supply Transformer	11								•
A62U1	Power Supply Regulator	46								•

FRONT PANEL – REAR PANEL H

FRONT PANEL

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- Functional Group Contents

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- Simplified Block Diagram of Front Panel Assemblies
- Front Panel Troubleshooting Block Diagram

REPAIR PROCEDURES
- Front Panel Disassembly
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A1, A2, A3 TROUBLESHOOTING

KEYBOARD AND KEYBOARD CONTROLLER CIRCUIT DESCRIPTION

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REAR PANEL FEATURES

FRONT AND REAR PANEL INTRODUCTION

This section provides information for servicing the front and rear panel keys, connectors, switches, RPG, annunciators, and displays, and is organized as follows:

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A1 ALPHA DISPLAY TROUBLESHOOTING

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A3 DISPLAY PROCESSOR DSA TROUBLESHOOTING

A5 KEYBOARD AND A7 LOWER KEYBOARD, CIRCUIT DESCRIPTION

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REQUIRED EQUIPMENT

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SYMPTOMATIC TROUBLESHOOTING

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RF CONNECTORS

REAR PANEL BNC CONNECTORS

8410 INTERFACE CONNECTOR

8755 ALT SWP INTERFACE CONNECTOR

HP-IB INTERFACE CONNECTOR

REAR PANEL FEATURES

REAR PANEL SCHEMATIC

FRONT PANEL OVERALL DESCRIPTION

INTRODUCTION

The front panel includes the following assemblies:

A1 Alpha Display
A2 Display Driver
A3 Display Processor
A5 Upper Keyboard
A7 Lower Keyboard

The A4 Assembly is unassigned.

OVERALL DESCRIPITON

The front panel assembly contains a separate microprocessor (A3U1) used to refresh the displays. The main instrument processor sends data to be displayed to the front panel processor via the Instrument Data Bus and Instrument Address Bus. The front panel processor stores this data in an internal RAM buffer. The front panel processor has 2K of internal ROM which contains a program to generate the necessary control signals to display the data.

There are two types of displays. The ENTRY DISPLAY includes 28 5X7 dot matrix characters. Both alpha and numeric data can be displayed in the dot matrix ENTRY DISPLAY. The frequency and POWER dBm displays are 7 segment/character displays. Only numeric data is normally displayed in the segment displays.

The front panel processor determines what segments and/or dots to illuminate and then outputs the appropriate digital signals to the circuitry that illuminates the displays. The processor continuously refreshes the displays about 80 times per second.

The main instrument processor controls the LED annunciators via the Instrument Data Bus and Instrument Address Bus.

The two keyboards (A5 Upper Keyboard and A7 Lower Keyboard) and the RPG (Rotary Pulse Generator) communicate with the main instrument processor via the A6 Keyboard Interface. When a key is pressed, a low true column and a low true row signal are generated. These signals are encoded by the Keyboard Interface. A service request to the main instrument processor is generated. The processor then reads the encoded signal via the Instrument Data Bus and Instrument Address Bus.

When the RPG is rotated, a counter is either incremented or decremented, a service request is generated and the main insturment processor reads the counter output.

The front panel POWER STANDBY/ON switch is an open circuit in the

ON position. In STANDBY a ground is supplied to the yellow STANDBY LED and to the fan relay (A62K1). This ground is also LSBY (Low StanBY). In STANDBY, the fan relay is energized and the power to the fan is removed. The LSBY signal is fed to the +20V regulator which shuts down the +20V supply. Since the +20V supply is used as a reference for all other regulated supplies, all of the regulated supplies are shut down as well. In the STANDBY mode, line power is still applied to the power transformer primary and to the unregulated supplies.

TROUBLESHOOTING TO ASSEMBLY LEVEL

8340A TROUBLESHOOTING SETUP

1. Disconnect all cables from the HP 8340A. It is especially important that any HP-IB controller be removed.

2. Cycle the power - turn the POWER switch to STANDBY, wait several seconds for all power supply capacitors to discharge, turn the POWER switch to ON.

3. Press **[INSTR PRESET]**, and compare the resultant instrument configuration with this expected configuration:

   Start Frequency - 10 MHz

   Stop Frequency - 26.5 GHz.

   Power level - 0.0 dBm (this is the factory-set value and may have been changed by the user by changing calibration constant 56).

   Sweep Time - AUTO (44.15 msec, seen by pressing **[SWEEP TIME]** if in doubt).

   Sweep - CONT

   Trigger - FREE RUN.

   RF - on.

   LEVELING - INT.

INSTR CHECK LEDs should be off. If either or both of these LEDs remain lit after power-on or an INSTR PRESET refer to the Overall Instrument Troubleshooting in Section VIII Service Introduction.

If upon power on the front panel goes into the front panel diagnostic mode (i.e., same as pressing **[SHIFT] [FREE RUN]**), suspect the main instrument processor. At power on, the instrument processor should initiate the self test. One of the first things the self test does is a write to the front panel processor. If upon power on the front panel processor does not receive a write from the main instrument processor, and does not receive a LOW instrument preset, the front panel processor will automatically go into the diagnostic mode.

If upon power on, all front panel LED's are on (similar to holding **[INSTR PRESET]**) check the negative power supplies. The main instrment processor requires both the positive and negative supplies. The front panel LED's require only the positive supplies.

LED AND ANNUNCIATOR TEST

1. Turn the POWER switch to ON. Press and hold **[INSTR PRESET]**. All the LED's and annunciators should light and remain lighted for as long as **[INSTR PRESET]** is pressed. If any LED or annunciator fails to light, use Figures 8H-2 and 8H-3 to identify the affected boards for subsequent disassembly and repair.

ALPHANUMERIC DISPLAY TEST

1. Press **[SHIFT] [FREE RUN]** to activate the display self-test diagnostic mode. The following should be observed in a correctly operating instrument:

   The ENTRY DISPLAY shows "DISPLAY RAM TEST PASSED," for 3 seconds.

   "DISPLAY CHECKSUM = 3A" is shown in the ENTRY DISPLAY for another 3 seconds.

   All segments of the numeric displays will light, and all dots in the ENTRY DISPLAY will flash, for 6 seconds.

   The entire available character set will be scrolled across the displays, and will continue scrolling until this diagnostic routine is terminated.

2. If any discrepancies are noted, refer to "A1, A2, A3 DISPLAY TROUBLESHOOTING." After examining the display for failures, press **[SHIFT] [M5]** to terminate this diagnostic routine.

KEY AND RPG TEST

1. With the POWER switch set to STANDBY (no fan noise), examine the mechanical action of each key. Check for height differences, unusual sounds when pressed, and differences in the force required to depress each key. Check the RPG for smoothness of rotation.

2. Turn the POWER switch ON and press each key on the front panel. Check for the proper ENTRY DISPLAY message and for the lighting of the appropriate annunciators and LEDs.

3. Press **[INSTR PRESET] [POWER LEVEL]**. Rotate the RPG very slowly in both directions, watching for a 0.05 dB increment (clockwise rotation) or decrement (counter-clockwise) in the power level. Rapid rotation of a quarter-turn in either direction should cause a large change in power level.

4. Examine the connectors for contamination or deformation.

Any display or keyboard problems should be evident after the above tests. If the problem appears to be in the front panel, disassemble the front panel as described in **DISASSEMBLY** and then refer to either the display troubleshooting or keyboard troubleshooting following the appropriate circuit description. If the displays and keyboard appear to work correctly, go to the Overall Instrument Troubleshooting in the Section VIII Service Introduction to determine if some other malfunctioning circuit assembly could be causing the problem.

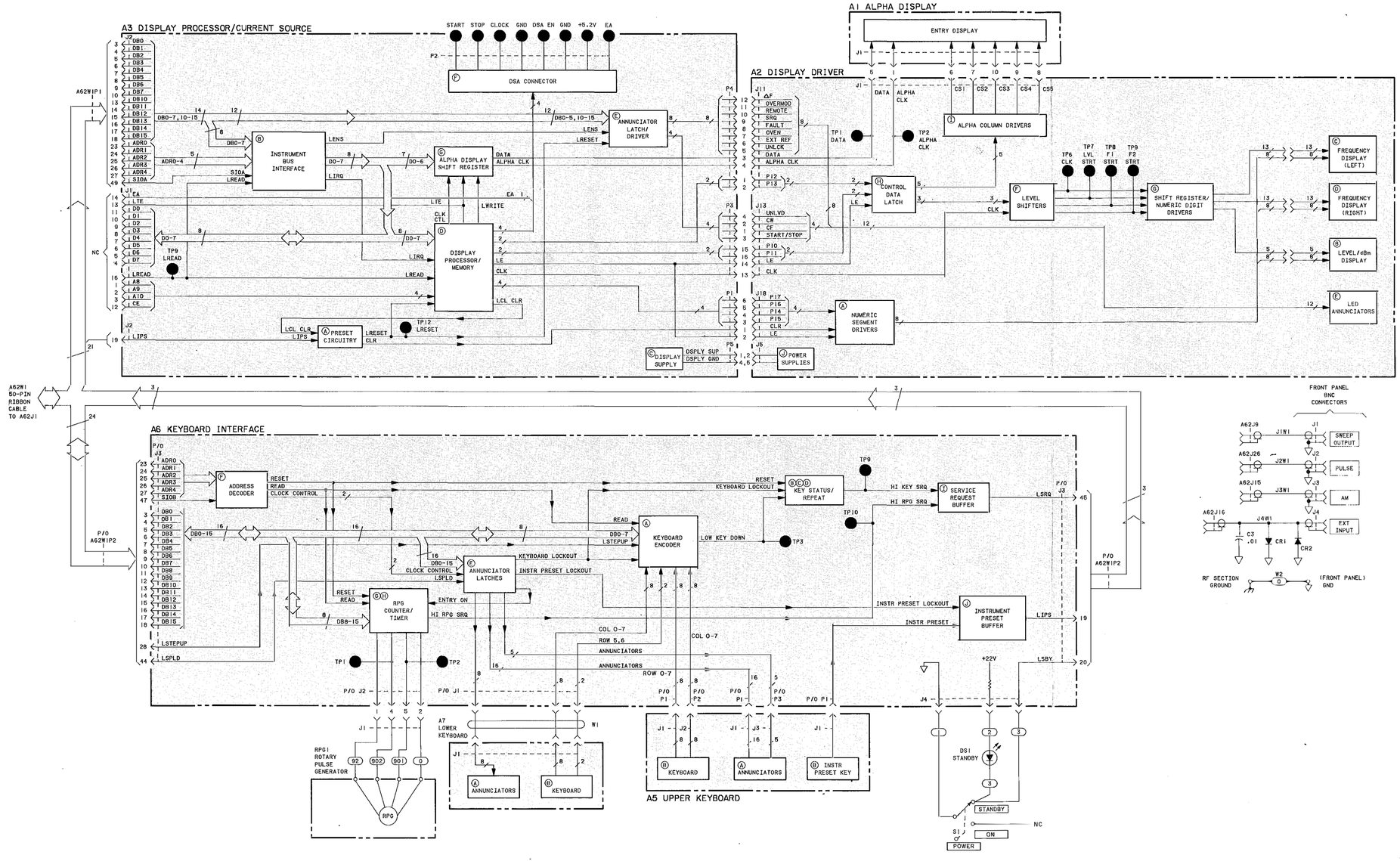
DISASSEMBLY

Figures 8H-4 through 8H-9 show the disassembly procedures for the front panel boards and components. Begin by performing the minimum disassembly necessary to expose the boards and associated cables, then check the integrity of the cable connections before continuing. Typically, faulty connectors cause many service problems and, because they are difficult to see and tend to be intermittent, such faults can be extremely difficult to identify. If faulty connections might be the cause of the problem, separate the connectors, examine the contacts for obvious damage, then reassemble the connectors and see if the symptoms have changed. Clean or replace the connectors as needed.

NOTE

Incorrect cleaning procedures can damage connector contacts. When cleaning contacts, observe these three precautions: 1) Avoid any rubbing motion that might generated static electricity, with subsequent ESD destruction of semiconductor components. 2) Avoid solvents that might chemically react with the contacts - halogenated compounds (containing chlorine or bromine) are especially hazardous. Common rubbing alcohol (70% isopropyl alcohol, 30% water) is generally recognized as a safe and effective cleaning agent. Use a lintless cloth with the solvent. 3) Do not use rubber erasers for abrasive cleaning because they remove part of the very thin gold plating, and they deposit a residue on the metal surfaces.

Continue the disassembly to obtain two, 3-board clusters - the keyboard cluster and the display cluster (note the "service position" for the display cluster in Figure 8H-6) - and proceed with the appropriate troubleshooting procedure (Display or Keyboard).



NOTES:

1. REFER TO THE SERVICE SECTION INTRODUCTION FOR A DESCRIPTION OF THE SYMBOLOGY USED FOR THIS BLOCK DIAGRAM.
2. NOT ALL POWER SUPPLY INTERCONNECTIONS ARE SHOWN ON THIS BLOCK DIAGRAM.

Figure 8H-1. Detailed Block Diagram

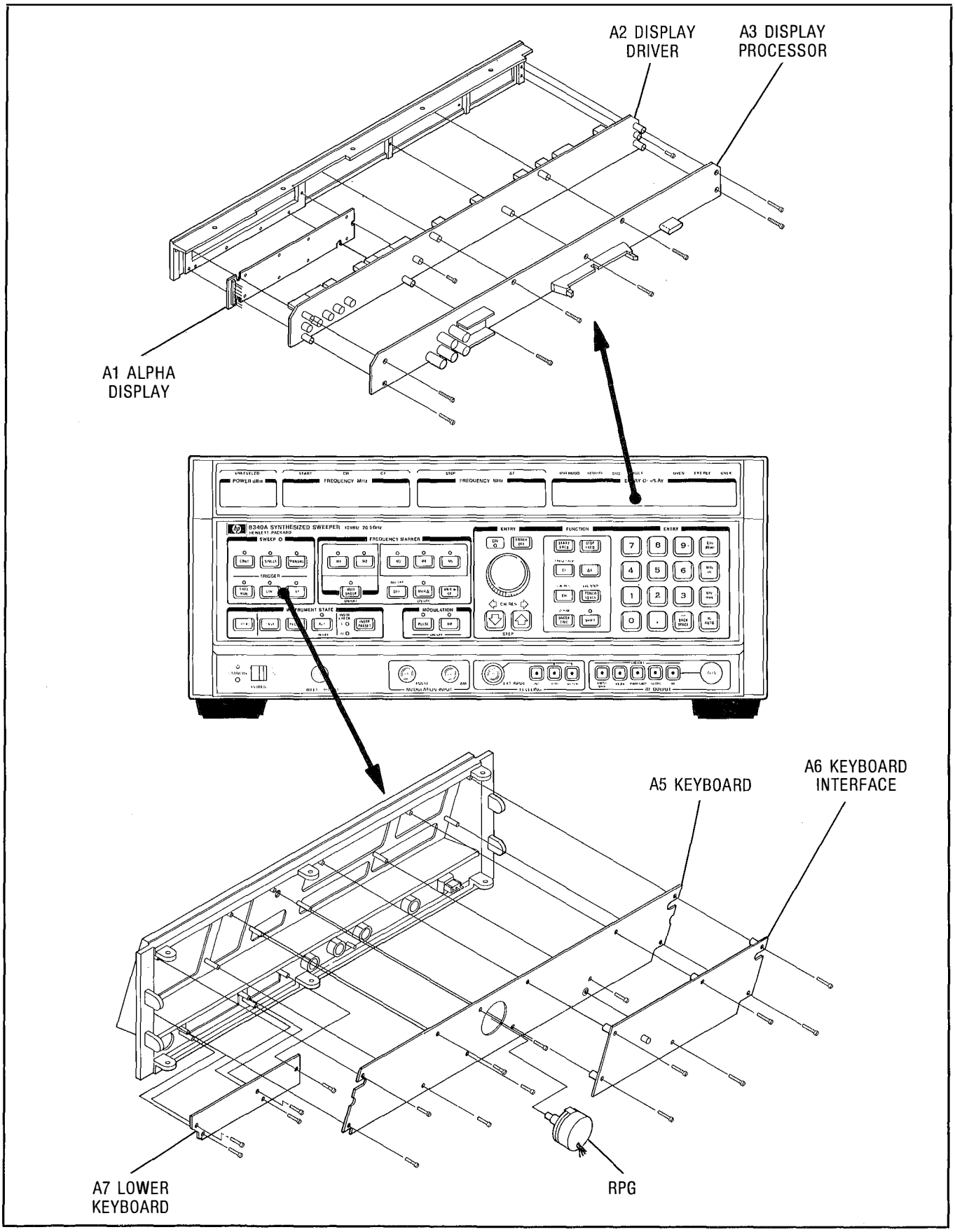


Figure 8H-2. Placement of Front Panel Assemblies

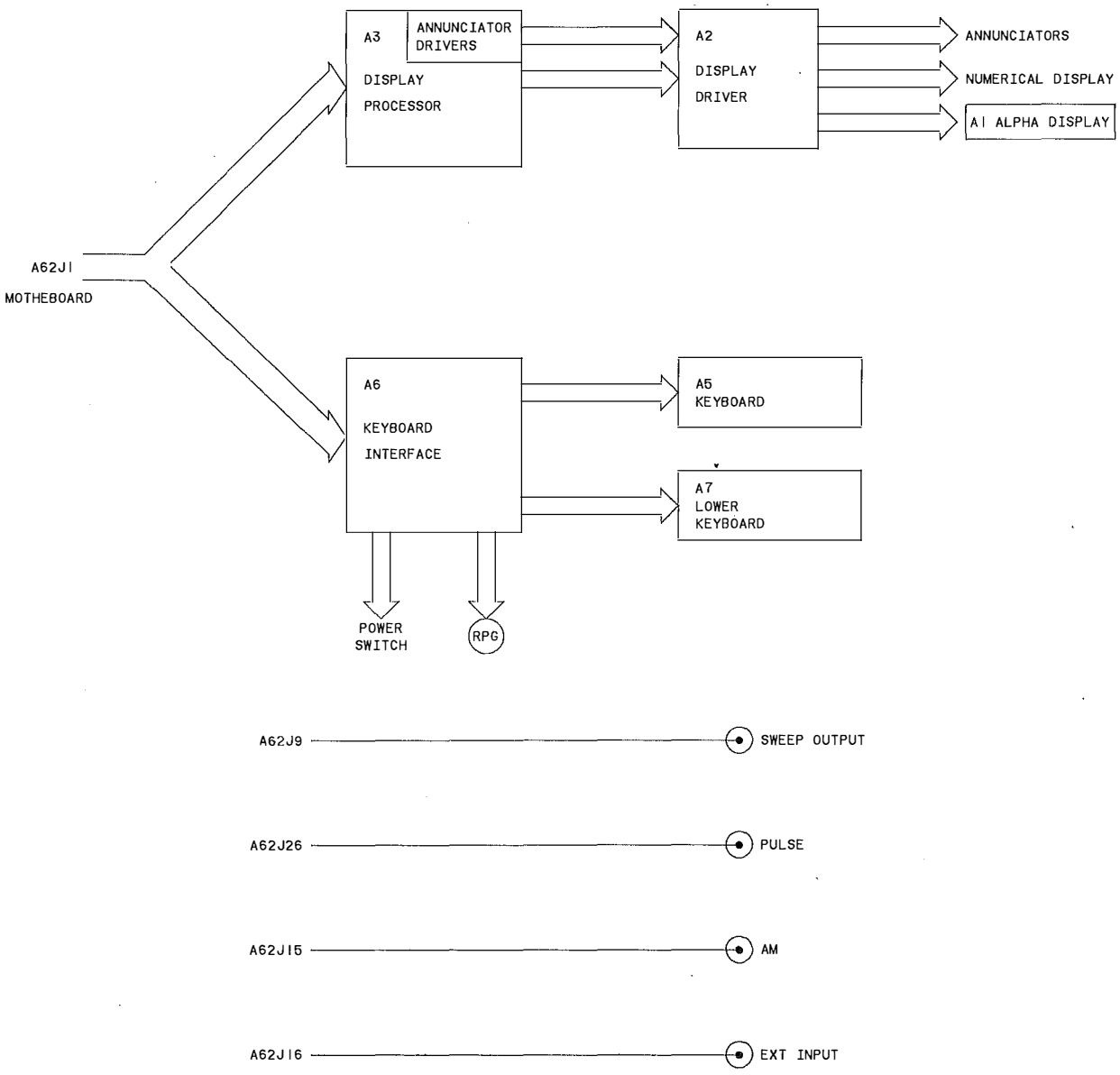
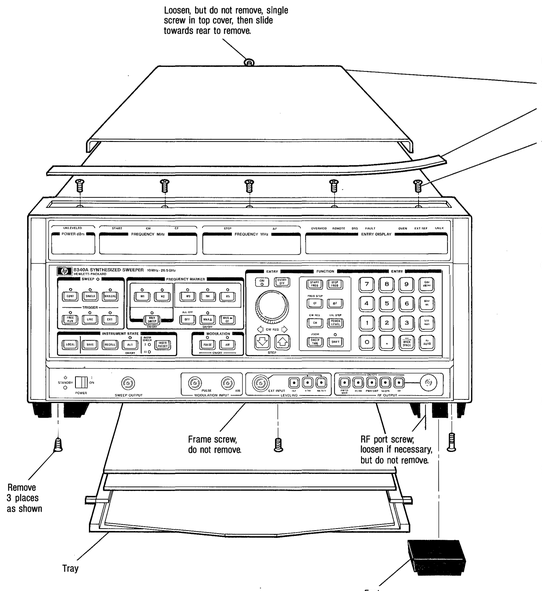


Figure 8H-3. Simplified Block Diagram of Front Panel Assemblies



1. Disconnect ac power line cord.
2. Remove top cover to facilitate subsequent cable removal.
3. Remove vinyl trim from the top, front edge of instrument by prying a corner loose and gently peeling the trim from the bezel.
4. Remove all five screws that are visable under the trim.

NOTE

It is important that screws of the correct length be used in these five locations. Longer screws protrude through the display casting and damage the display driver board.

5. Remove either front foot (instructions are on the foot) to release the information cards tray. Remove the tray.
6. Five screws will be seen on the lower, front frame edge: remove 3, as shown, and loosen a fourth if necessary.

NOTE

The loosened screw centers the RF connector in the front panel opening. Be sure that the RF connector is recentered and secured during re-assembly of the front panel.

7. Gently pry the front panel and display assembly from the frame. It may be necessary to apply pressure from behind against the display assembly.
8. If you intend to remove the entire front panel then you must disconnect the two 50-wire ribbon cables, and the four coaxial cables (the coaxial cables that connect the front panel BNC connectors to the motherboard SMB connectors). If you intend to only troubleshoot the display and/or keyboard assemblies then you only need to disconnect the ribbon cable that is attached to the display assembly.
9. Separate the keyboard assembly from the display assembly by removing the three screws between the panel castings.
10. To work on the keyboard, reconnect the ribbon cables and attach the display to the top of the front casting for support.
11. To work on the display, configure the display boards into the service position (Figure 8H-6), reconnect the ribbon cables, lay the display board on the reinstalled top cover, and attach the keyboard to the front panel for support.

Figure 8H-4. Front Panel Disassembly

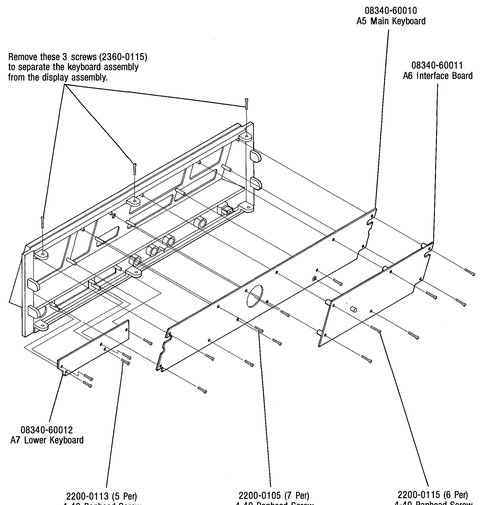


Figure 8H-5. A5, A6, A7 Disassembly

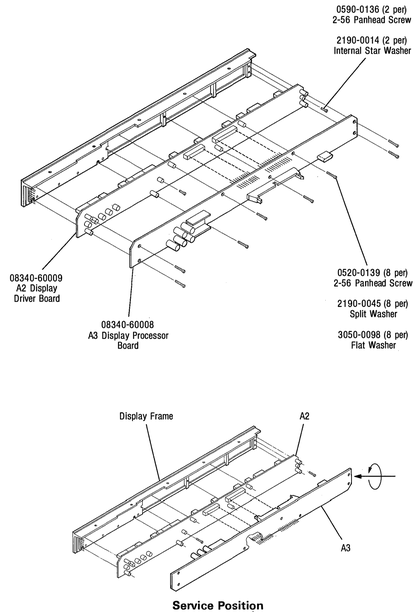


Figure 8H-6. A2, A3 Disassembly

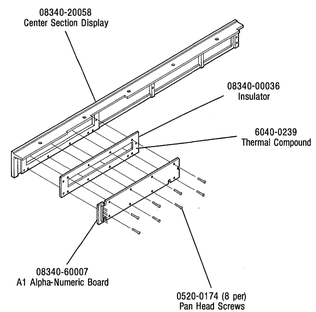


Figure 8H-7. A1 Disassembly

INSERT IN FRONT OF PAGE 8-573/8-574

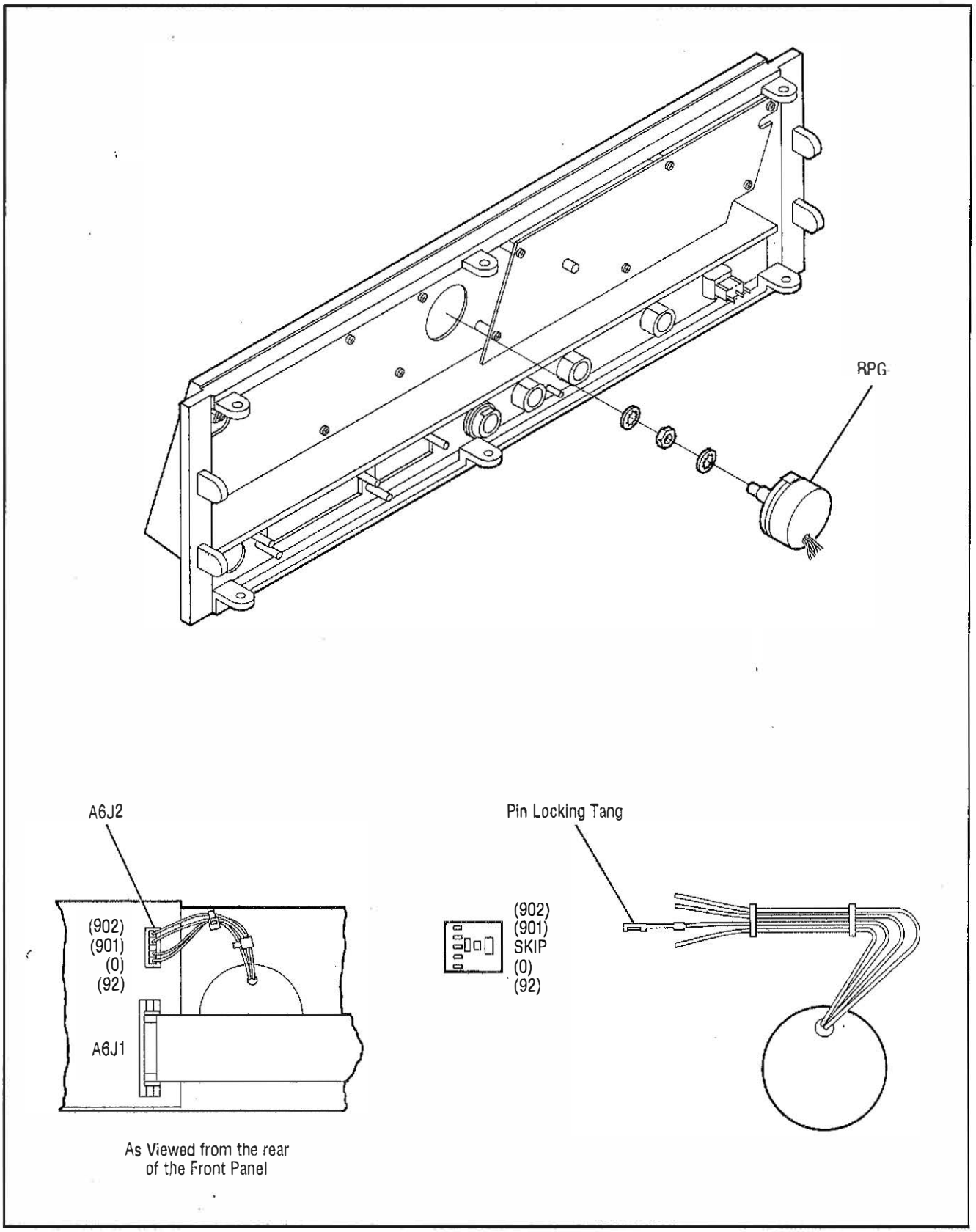


Figure 8H-8. RPG Disassembly

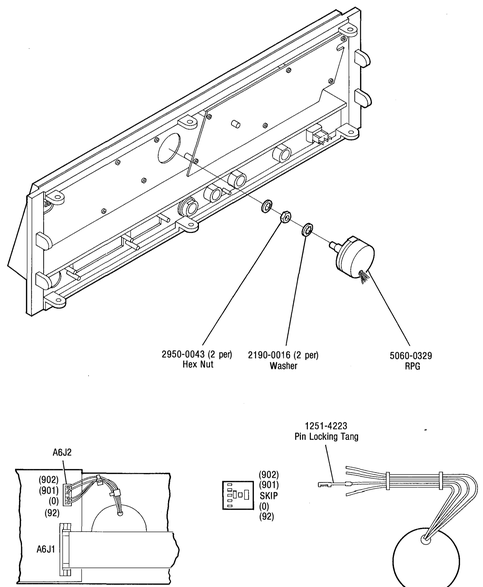
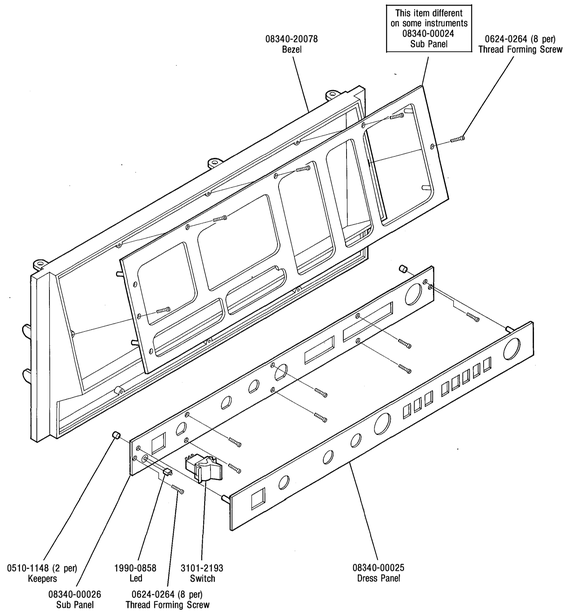
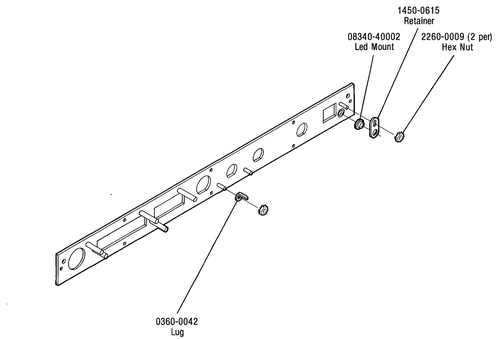
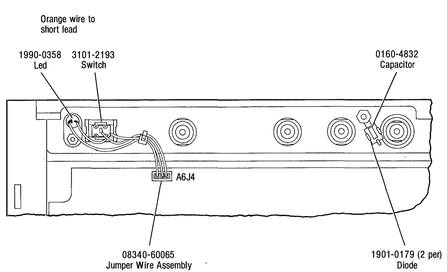


Figure 8H-8. RPG Disassembly







Service Position

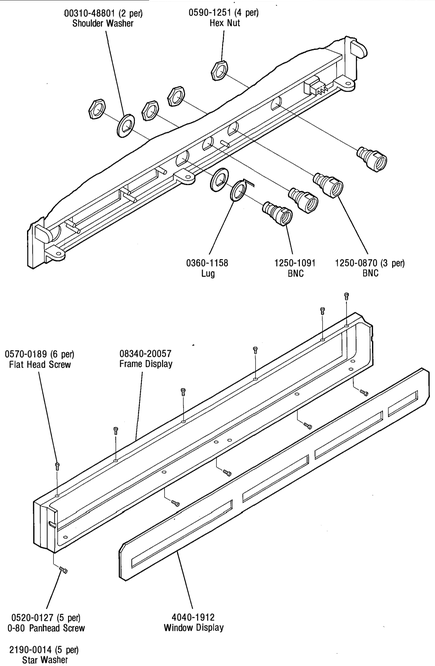


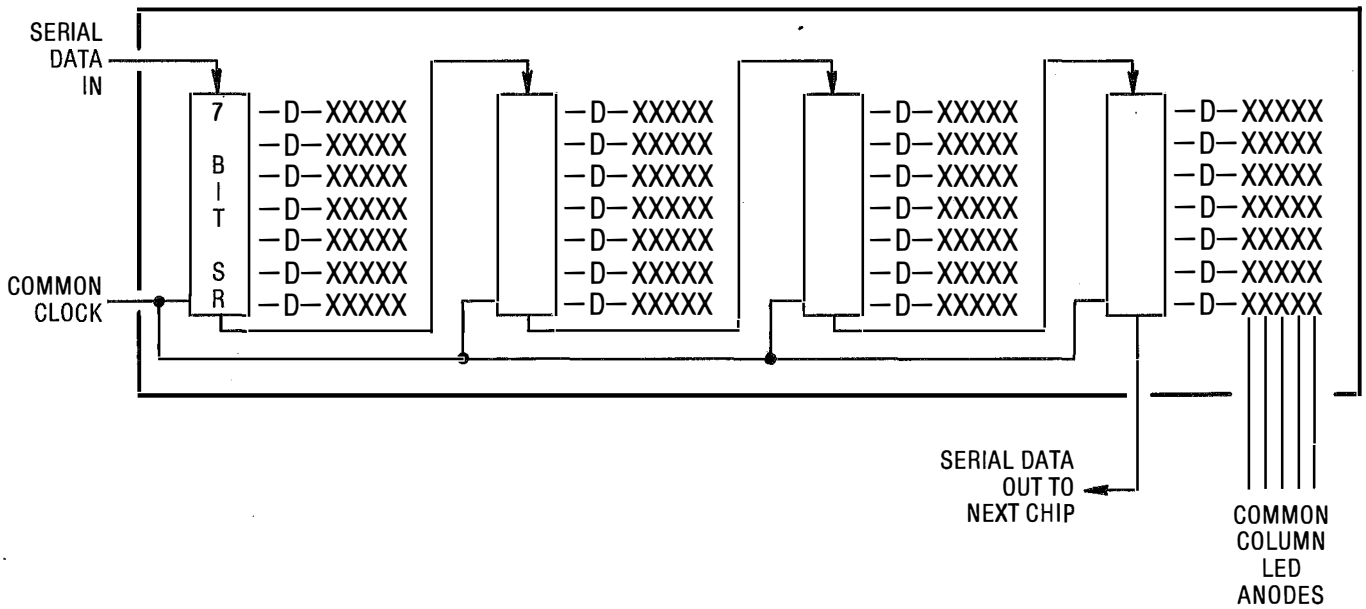
Figure 8H-9. Panels, Switch, and Connectors Dissassembly

A1 ALPHA DISPLAY, CIRCUIT DESCRIPTION

An integrated 5X7 dot matrix display is used in the 8340A for display of alphanumeric information. Seven, four-character chips are used for a total of 28 characters. The shift register (SR), drivers (D), and LEDs (X) are arranged as follows:

The 5 LEDs in each row are common to one driver. Each character has 5 columns (columns 1 through 5). The same column in each character is driven by a common column driver (i.e. column 1 in all 28 characters is driven by the same column driver).

The appropriate LEDs in one column of all 28 characters are turned on at one time for about 2.5 ms. The next column is selected and the appropriate LEDs in that column are turned on. The entire process is repeated at about 80 times per second.



When the processor is ready to display a line in the alpha display, the processor fetches the character out of RAM for the last character position of the display. Next, the processor determines which column of the character is being set up (for example, column 5). The processor looks up the bit pattern for the 7 LEDs in the column. The processor outputs these 7 bits, in parallel, to the shift register. The shift register outputs the 7 bits serially to the displays. The processor gets the next to the last character and repeats the above sequence until all 196 bits (7 rows times 28 characters) have been shifted into the displays. Since all 5 LEDs in each row are common to a row driver, if a bit for the particular row is a 1, the cathodes of the LEDs in that row will be pulled LOW. However, only one of the five LEDs is turned on by pulling the appropriate column line HIGH. The above sequence is repeated for each of the five columns and the whole process is repeated at a rate of approximately 80 times per second to ensure a flicker-free display.

The alpha display shift clock is the same alpha display clock generated and controlled on the Display Processor board.

The alpha displays dissipate a lot of power and as a result they must have a substantial heat sink. For this reason the display chips are soldered into the PC board and the PC board is screwed directly to the anodized aluminum bezel assembly. On the PC board, all of the pins to the chips have as much copper connected to them as possible so that the heat will be conducted into the copper on the PC board and then into the bezel. Heat sink compound should be used between the alpha display PC board and the bezel to ensure a low thermal resistance.

A1 ALPHA DISPLAY TROUBLESHOOTING

1. Remove the A1, A2 and A3 boards from the display casting and plug the A1 Board directly into the A2 Board. Take precautions to prevent the A1 Alpha Display from shorting out against the A2 Display Driver.

2. If the Alpha display appears to be working correctly after removing it from the casting, suspect that the anodized insulator has developed a short. If this is the case, clean the casting and the PC board and check for sharp protrusions or foreign particles. Install a new insulator using a non-silicone base thermal compound.

3. If part of the characters are working and some are not, either a signal trace is open or one of the integrated displays is bad. Probe CS1 through CS5, ALPHA CLK, and DATA IN right at the display chip that is not working. If the signals appear at its pins, replace the display. If DATA IN (pin 12) does not appear at the display in question, either this display or the previous display could be at fault.

A2 DISPLAY DRIVER, CIRCUIT DESCRIPTION

NUMERIC SEGMENT DRIVERS A

Each numeric digit is formed by various combinations of seven segments and a decimal point. The anodes of the same segment in each numeric digit are connected in parallel and go to a segment driver. The cathodes of all eight segments within a digit are connected in parallel and go to a digit driver. Therefore, there are eight segment drivers common to all digits plus one digit driver for each of the 31 digits. To display numbers in all display digits, the processor starts at the first digit by clearing the segment driver latch and by turning on the digit driver for the first digit. The display processor then determines from RAM what character should be displayed in this first digit and then sets the appropriate bits of the segment driver latch. Once these bits of the latch are set, the corresponding segment drivers supply current through the segment and out the digit driver. The processor leaves these drivers on for a few tens of milliseconds. At the end of this display time, the segment drivers are all turned off. The shift register/digit driver is immediately shifted to drive the second digit. None of the LED segments of the second digit turn on until the processor determines what character should be displayed and turns on the appropriate segment drivers. This second digit is then displayed for a few tens of milliseconds and so on through all 31 digits until the last digit is displayed and then the whole process is started over. This whole process is repeated about 80 times per second so the eye is not able to perceive the flicker.

The processor selects which numeric segments to turn on by setting the appropriate bits in an 8-bit addressable latch (U9). Processor I/O port P14 through P17 (A3U1 pins 31 through 34) control the address and D input to U9. The address bits (U9 pins 1, 2, and 3) are set to indicate the bit in the latch being changed and the D input (U9 pin 13) is set HIGH or LOW depending on whether you wish to turn on a segment or turn off a segment. The clock line (U9 pin 14) is connected to the LE (Latch Enable) clock signal from A3 block D. Since this clock is essentially the same as the processor LTE (Low Trigger Enable) line, each instruction cycle will transfer the information currently contained on the address and D inputs to the outputs of U9 (U9 pins 4 through 7 and pins 9 through 12).

Each output of U9 is connected through a 1 K ohm resistor to a segment current source and to a 2.2 K ohm resistor connected to the main +5.2V supply.

The segment current sources are formed by two transistors and a resistor (Q11, Q12, and R29 for example). When U9 pin 12 goes HIGH, the upper transistor (Q11) is turned on due to the base current supplied by the 2.2 K ohm resistor and conducts current

from the display supply out its emitter and through the resistor (R29). This current increases until the voltage drop across the resistor (R29) equals the VBE drop of the lower transistor. As soon as this current is reached, the lower transistor (Q12) begins to conduct and removes some of the base drive current to the upper transistor (Q11). This process reaches an equilibrium with the lower transistor (Q12) conducting just enough current to remove the excess base current supplied to the base of the upper transistor (Q11). This type of current source is used because it is fairly immune to the voltage variations of the display supply.

When U9 pin 12 goes LOW it conducts all of the current provided by the 2.2 K ohm resistor away from the base of Q11 thus turning off the current source.

Each of the eight segment current sources provides approximately 0.60/16.2 or 37 mA to its particular segment.

NUMERIC DISPLAYS B, C, AND D

The numeric displays consist of two 15 digit and one 5 digit monolithic seven-segment displays (A matched set is available to provide equal illumination). In the 8340A, only 13 of the 15 digits are used in each of the larger displays.

LED ANNUNCIATORS E

Each annunciator is connected in series with a current limiting resistor to +12 volts. The resistor values are selected to make the apparent brightness to the eye the same on all annunciators.

LEVEL SHIFTERS F

In order to meet the input voltage requirements of U4, U5 and U8 power shift registers, level shifters must be used to translate the TTL levels to that required by these ICs.

When the input to the clock level shifter (R7, R8, R9, VR4, and Q6) is not pulled LOW, current is supplied to the base of Q6 through R9 and VR4 and thus causes Q6 to turn on. When Q6 turns on, it pulls one end of R7 down to approximately -5 volts. Each clock input sources 1.8 to 3.5 mA therefore, the current through R7 will be between 5.4 and 10.5 mA making the voltage at the clock inputs (U4, U5 & U8 pin 9) between -3.6 and -2.25 volts. When the input to the clock level shifter is LOW, the base of Q6 is allowed to be pulled down to -5.2 volts thus turning Q6 off and allows the internal pullups of the IC to pull the input HIGH. When the input to one of the start level shifters (R1, R2, and VR1, or R3, R4, and VR2, or R5, R6, and VR3) is not pulled LOW, the start input (U4, U5, and U8 pin 8) will be at approximately +0.6 volts. When the input to one of the start level shifters is pulled low (1.0 volts), the start input will be at approximately -2.2 volts due to the 3.16 volt differential supplied by the zener diode (VR1, VR2, or VR3).

SHIFT REGISTER/NUMERIC DIGIT DRIVER G

The numeric digit drivers (U4, U5, and U8) are power shift registers whose outputs are capable of sinking 250 mA. When the start line (pin 8) is pulsed HIGH, all outputs of the shift register (pins 11 through 20 and 1 through 7) go HIGH. After the application of a start pulse, the first LOW going clock pulse applied to the clock line (pin 9) will cause output U8 (pin 11) to go LOW. Each successive pulse on the clock line (pin 9) shifts this LOW output to the next output line and the previous line goes HIGH. The LOW output shifts through each output line and finally is shifted out of the shift register at which time all outputs will again be HIGH. The outputs of these power shift registers (U4, U5, and U8) are each connected to all the segment cathodes of one digit thus when the output goes LOW it turns on all of the segments in that digit whose segment drivers are activated. The power shift registers have non-standard logic levels for the clock and start inputs. The clock input (pin 9) LOW level is -2.2 volts and has a pull up inside the IC so it can be driven from an open collector transistor. The start input (pin 8) has a HIGH level of +0.5 volts and a LOW level of -0.8 volts.

CONTROL DATA LATCH H

The control data latch (U3) is an open collector addressable D-latch. The address inputs (U3 pins 1, 2, and 3) and the D input (U3 pin 13) are connected to the display processor I/O port P10 through P13 (A3U1 pins 27 through 30). The clock line (U3 pin 14) is connected to the LE signal so each LE cycle the latch will be updated with the current information contained on the I/O port lines. Outputs 4, 5, and 7 (U3 pins 9, 10, and 12) go to the numeric display start pulse level translators. Outputs 0, 1, 2, 3, and 6 (U3 pins 4, 5, 6, 7, and 11) go to Alpha display column drivers 3, 2, 1, 4, and 5 respectively.

ALPHA COLUMN DRIVERS I

The alpha column drivers are formed by Q1 through Q5 and resistor packs U1 and U2. When it is time for the processor to turn on one of the alpha columns, the processor addresses one of the column control lines in the control data latch (U3) LOW which pulls down on the base of one of the column driver transistors (Q1 through Q5) through a 24 ohm resistor. This turns on the transistor which pulls the column line up to the Display Supply.

A2 DISPLAY DRIVER, BLOCK-BY-BLOCK TROUBLESHOOTING

Numeric Segment Drivers (A2 Block A)

ALL NUMERIC DISPLAYS ARE OFF

If all of the segments of all numeric displays are off, first troubleshoot the SHIFT REGISTER/NUMERIC DIGIT DRIVER (A2 Block **G**) and LEVEL SHIFTERS (A2 Block **F**). If no other fault is found, then possibly one of the control signals to A2U9 is faulty.

1. Press **[SHIFT] [FREE RUN]** to run the front panel display diagnostics. Set up the oscilloscope for 50 us/Div.

2. Probe CLR (A2U9 pin 15) with the oscilloscope. You should find LOW going TTL pulses which are 10 to 50 us wide. If this signal is LOW all the time then all numeric displays will remain OFF. If CLR is not correct, troubleshoot the DISPLAY PROCESSOR (A3 Block **D**) or replace A2U9 if U9's input is bad.

3. Probe LE (A2U9 pin 14) with the oscilloscope. Set the oscilloscope to 1 us/Div. You should find LOW going TTL pulses which are 0.36 us wide with a period of 1.36 us. If this signal does not appear, troubleshoot the DISPLAY PROCESSOR (A3 Block **D**).

4. Probe the remaining inputs to U9 (U9 pins 1, 2, 3, and 13). You should find TTL activity. If any of these lines do not have activity or have incorrect voltage levels, troubleshoot the DISPLAY PROCESSOR (A3 Block **D**).

ONE OR MORE NUMERIC DISPLAY SEGMENTS IS ALWAYS OR NEVER ON

If one or more of the numeric display's segments is always on or is never on, the problem most likely lies with the segment current source.

1. Probe the output of U9 which corresponds with the affected segment with the oscilloscope. Set the oscilloscope to 0.5 ms/Div. You should find various patterns of 0.3 ms wide, HIGH going pulses. These pulses will be limited in amplitude to about 3 to 3.5 volts.

2. If the signal at the output of A2U9 is approximately correct, and the segment is on all of the time, it is most likely that the transistor connected to the Display Supply is shorted or a trace from the current sources to the Numeric Displays is open or shorted.

3. If the signal at the output of A2U9 is approximately correct, and the segment is off all of the time, either the transistor connected to the Display Supply is open, the current limiting

transistor is shorted, or a trace from the current sources to the Numeric Displays is open or shorted.

Numeric Displays (A2 Blocks B Through D)

If you have determined that neither the Segment Drivers (A2 Block A) nor the Digit Drivers (A2 Block **G**) is at fault, replace the Numeric Display Set. This display set is matched for intensity category so be sure to either replace the entire set or else use the same intensity category.

LED Annunciators (A2 Block E)

See troubleshooting of **Annunciator Latch/Driver (A3 Block E).**

Level Shifters (A2 Block F)

1. Probe NUM CLK (A2TP3) with the oscilloscope. Set the oscilloscope to 1 us/Div. You should find 3 us wide, HIGH going, 3V pulses. If this signal is not present, troubleshoot the DISPLAY PROCESSOR (A3 Block **D**).

2. If the NUM CLK signal is higher than 3.5V, check the signal levels at the base of Q6. You should find 3 us wide pulses that are 0.6 to 0.8 volts high. If there are no pulses at all at Q6 base, VR4 is open and should be replaced. If the pulses at the base of Q6 are higher than 0.8V, the base of Q6 is open.

3. Probe CLK with the oscilloscope. You should find 3 uS wide, LOW going pulses that go between -3 volts and at least +1.8V. If CLK stays at -3 volts all the time, either Q6 is shorted or R7 is open. If CLK stays at a level near 5 volts all the time, Q6 is open.

4. If you have reason to believe that one of the STRT level shifter circuits is malfunctioning, probe the appropriate signal (LVL START, F1 START, or F2 START) at the cathode of VR1, VR2 or VR3. You should find 3 us wide, HIGH going pulses with levels from 0.7V to approximately 4 volts. If no signal appears, troubleshoot the CONTROL DATA LATCH (A2 Block **H**).

5. If one of these signals is greater than 4 volts, probe the associated test point (TP4, TP5, or TP7). You should find approximately +- 1.5 volt levels. If the signal at the test point stays at -1.5 volts all the time, it is likely that the zener diode is open. If this signal never goes negative, either the zener is shorted or is in backwards. It is also possible that an input to one of the Numeric Digit Drivers is shorted.

Shift Register/Numeric Digit Driver (A2 Block G)

1. Check for approximately 4.4 to 4.6 volts right at U4 or U5 pin

10 and U8 pin 10. If this voltage is not present, replace CR1 or CR2 as appropriate.

2. Probe the CLK signal at pin 9 of U4, U5, or U8 with the oscilloscope. You should find 3 us wide, LOW going pulses that go between -3 V and at least +1.8V. If these pulses are not present, troubleshoot the Level Shifters (A2 Block **D**).

3. Probe the STRT signal of the suspected driver at pin 8 of U4, U5, or U8 with the oscilloscope. You should find 3 us wide HIGH going pulses that go between approximately +-1.5V. If these pulses are not present, troubleshoot the Level Shifters (A2 Block **D**).

4. Probe the outputs of the Digit Drivers (U4, U5 or U6) with the oscilloscope. Set the oscilloscope to 0.1 ms/Div. Since the outputs of the drivers are open collector, connect a 1k ohm resistor between your probe and +5V with small clip leads. This should allow you to observe 400 us wide, LOW going pulses that go between +5V and approximately 0.5V. If this pulse does not appear or if the LOW level is above 0.8 volts, you should replace the driver.

Control Data Latch (A2 Block H)

1. Probe P10 thru P13 signals (A2U3 pins 1, 2, 3, and 13) with the oscilloscope. Set the oscilloscope 0.5 ms/Div. You should find TTL activity. If TTL activity is present, proceed with step 3.

2. Lift the appropriate pin of U3 to determine if the input to U3 is the cause of the problem. If the signal is correct after lifting the pin, replace U3. If the signal is still bad, troubleshoot the DISPLAY PROCESSOR (A3 Block **D**).

3. Probe LE (A2U3 pin 14) with the oscilloscope. Set the oscilloscope to 1 us/Div. You should find 0.4 us wide, LOW going pulses with a period of 1.4 us. If this signal is not present, follow the same procedure as in step 2.

4. Probe the three STRT lines and you should find 3 us wide, HIGH going pulses. If any of these signals are not present, replace U3.

5. Probe COL 1 through COL5 signals (A2U3 pins 4, 5, 6, 7, and 11) with the oscilloscope. Set the oscilloscope to 0.5 ms/Div. You should find signals which go between 0.5V and 4V. If any of these signals are not present, replace U3.

Alpha Column Drivers (A2 Block I)

1. Probe CS1 through CS5 at the collector of Q1 through Q5 with

the oscilloscope. Set the oscilloscope to 0.5 ms/Div. You should find approximately 1 ms wide, HIGH going pulses of varying amplitudes but at least 2V high. If these signals are present yet one or more alpha display columns are not lighting, check for opens to the A1 board or troubleshoot the A1 Alpha Display.

2. If CS1, CS2, CS3, CS4, or CS5 remain HIGH all the time, connect a 1k ohm resistor between your probe and ground using small clip leads and probe that signal again. If the signal now appears, it is likely that there is an open trace between the transistor and the alpha display chips.

3. If the signal remains HIGH after performing step 2, either the associated transistor is shorted or the input to this block is LOW all the time. Probe the appropriate COL 1 through COL5 signal at U3. If the signal appears at this point, it is likely that the drive transistor is shorted. If no signal appears at U3, troubleshoot the CONTROL DATA LATCH (A2 Block H).

4. If CS1, CS2, CS3, CS4, or CS5 remains LOW all of the time, probe the appropriate COL 1 through COL5 signal at U3. If a signal appears at the output of U3 but the output of the associated driver transistor (Q1 through Q5) remains LOW, a trace is open, one of the resistors in U2 is open, or the drive transistor is open. If no signal appears at U3, troubleshoot the Control Data Latch (A2 Block H).

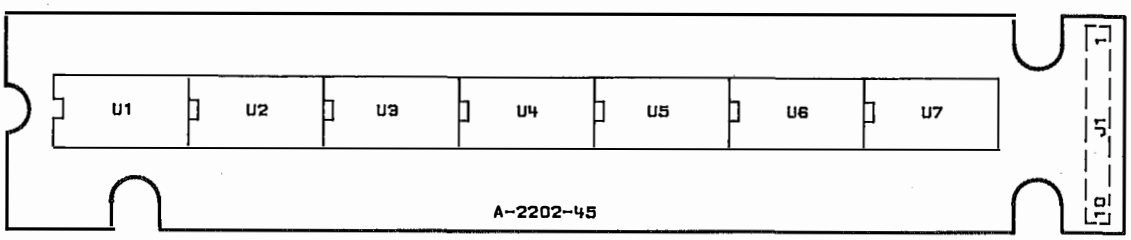


Figure 8H-10. A1 Alpha Display Component Location Diagram

A62J1 PIN I/O

Pin	Mnemonic	A62W1P1	A62W1P2	Levels
1	GND PLANE	PIN 1	PIN 1	0V
2	+12V	PIN 2	PIN 2	+12V
3	DB0	PIN 3	PIN 3	TTL
4	DB1	PIN 4	PIN 4	TTL
5	DB2	PIN 5	PIN 5	TTL
6	DB3	PIN 6	PIN 6	TTL
7	DB4	PIN 7	PIN 7	TTL
8	DB5	PIN 8	PIN 8	TTL
9	DB6	PIN 9	PIN 9	TTL
10	DB7	PIN 10	PIN 10	TTL
11	DB8	PIN 11	PIN 11	TTL
12	DB9	PIN 12	PIN 12	TTL
13	DB10	PIN 13	PIN 13	TTL
14	DB11	PIN 14	PIN 14	TTL
15	DB12	PIN 15	PIN 15	TTL
16	DB13	PIN 16	PIN 16	TTL
17	DB14	PIN 17	PIN 17	TTL
18	DB15	PIN 18	PIN 18	TTL
19	LIPS	PIN 19	PIN 19	TTL (LOW TRUE)
20	LSBY	NOT USED	PIN 20	0V TO +22V
21	GND PLANE	NOT USED	PIN 21	0V
22	HPUP	NOT USED	NOT USED	TTL (HIGH TRUE)
23	ADR0	PIN 23	PIN 23	TTL
24	ADR1	PIN 24	PIN 24	TTL
25	ADR2	PIN 25	PIN 25	TTL
26	ADR3	PIN 26	PIN 26	TTL
27	ADR4	PIN 27	PIN 27	TTL
28	LSTEPUP	NOT USED	PIN 28	TTL (LOW TRUE)
29	GND PLANE	PIN 29	PIN 29	0V
30	+22V	NOT USED	PIN 30	+22V
31	+5.2V	PIN 31	PIN 31	+5.2V
32	+5.2V	PIN 32	PIN 32	+5.2V
33	+5.2V	PIN 33	PIN 33	+5.2V
34	+5.2V	PIN 34	PIN 34	+5.2V
35	+5.2V	PIN 35	PIN 35	+5.2V
36	+5.2V	PIN 36	PIN 36	+5.2V
37	+5.2V	NOT USED	PIN 37	+5.2V
38	GND PLANE	NOT USED	PIN 38	0V
39	GND PLANE	PIN 39	PIN 39	0V
40	GND PLANE	NOT USED	PIN 40	0V
41	GND PLANE	NOT USED	PIN 41	0V
42	−5.2V	PIN 42	PIN 42	−5.2V
43	LSTP	NOT USED	NOT USED	TTL (LOW TRUE)
44	LSPLD	NOT USED	PIN 44	TTL
45	LSRQ	NOT USED	PIN 45	TTL (LOW TRUE)
46	GND PLANE	NOT USED	PIN 46	0V
47	SIOB	NOT USED	PIN 47	TTL (LOW TRUE)
48	GND PLANE	PIN 48	PIN 48	0V
49	ISOA	PIN 49	NOT USED	TTL (LOW TRUE)
50	GND PLANE	PIN 50	PIN 50	0V

Note: Refer to Front Panel Block Diagram and A62 Motherboard Wiring List for signal source and destination information.

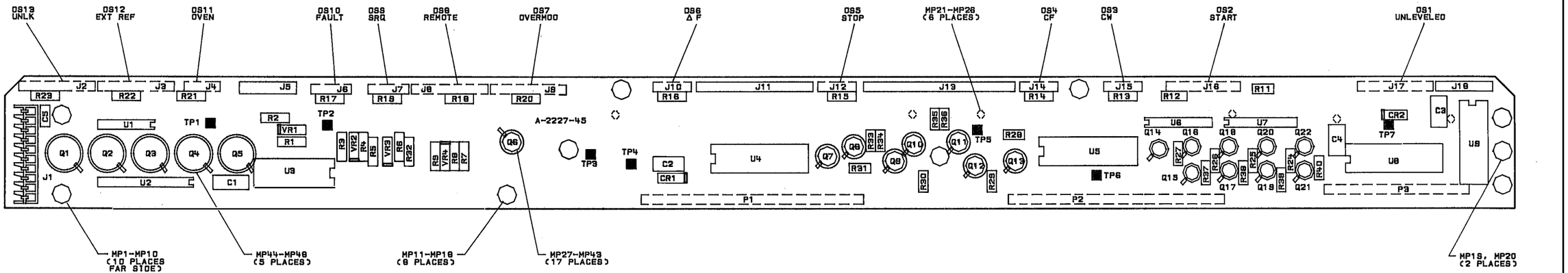


Figure 8H-11. A2 Display Driver, Component Location Diagram

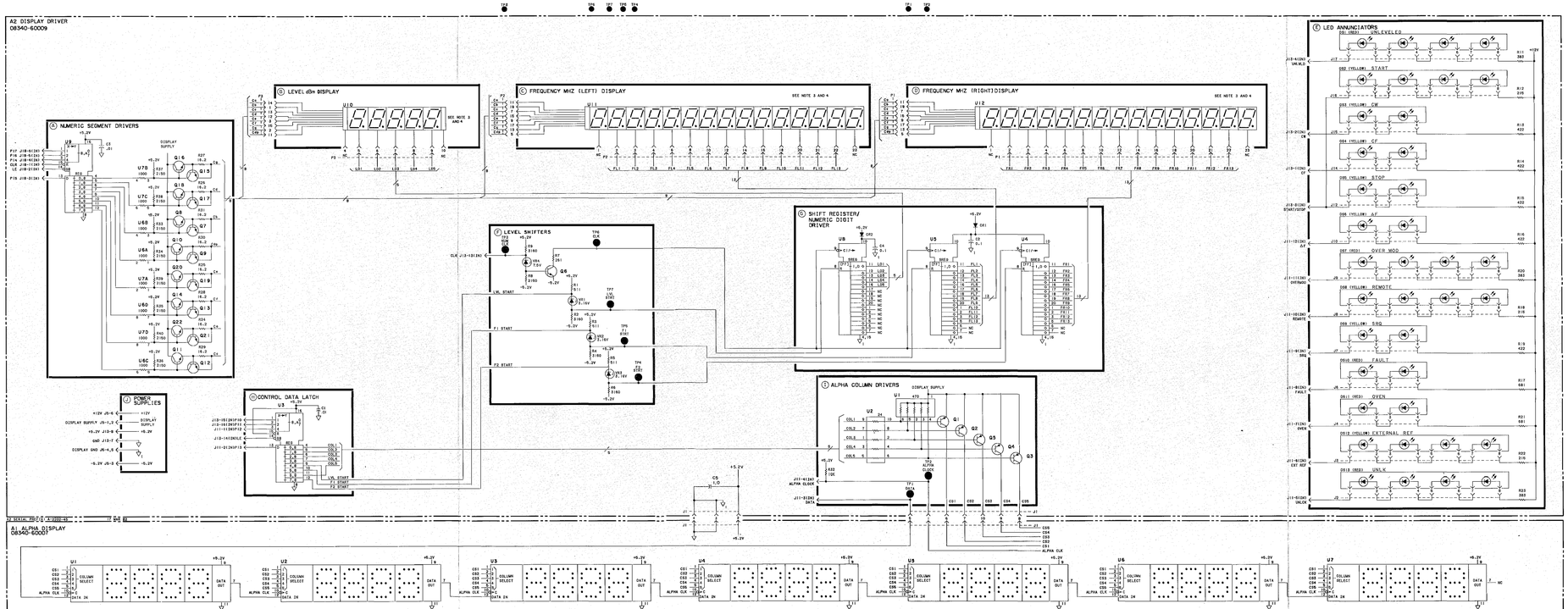


Figure 8H-12. A1 Alpha Display and A2 Display Driver, Schematic Diagram

A3 DISPLAY PROCESSOR, CIRCUIT DESCRIPTION

INSTRUMENT BUS INTERFACE B

The Instrument Bus Interface consists of an eight-bit D-latch (U6) and a 3 to 8 line decoder (U10).

The 3 to 8 line decoder (U10) decodes the address information from the instrument address bus and the SIOA signal and generates I/O strobe LEN 5 or LEN 7. LEN 5 (U10 pin 10) latches annunciator control bits (Block **E**) off the instrument data bus. LEN 7 (U10 pin 7) is the interrupt strobe to the display processor. LEN 7 is also the clock to the eight-bit D-latch (U6 pin 11) which latches the data being sent to the display via the instrument data bus.

The eight-bit D-latch (U6) serves to connect the two asynchronous buses together. The Q outputs of this latch are connected to the displays internal data/address bus. When the display processor is ready to accept the data stored in input latch U6, the read line of the processor (U1 pin 8) goes LOW enabling the D-latch (U6 pin 1). U6 then outputs onto the display data bus.

The Service Request Latch consists of two NAND gates connected as a set/reset latch. U3A has both of its inputs (U3 pins 1 and 2) HIGH so its output (U3 pin 3) will be LOW. U3B has one input (U3 pin 4) connected to the output of U3A (U3 pin 3) which is LOW. The other input (U3 pin 5) is connected to the processor read line (U1 pin 8 Block **D**) which is HIGH until it reads the data contained in the eight-bit data bus latch (U6). The output of U3B (U3 pin 6) is therefore HIGH which makes the circuit stable in this state until some input changes.

When the instrument processor sends an interrupt to the display, the interrupt line (U10 pin 7) goes LOW and then HIGH 400 nsec later. When this line goes LOW, U3 pin 1 goes LOW causing the output of U3A to go HIGH. This forces U3 pin 4 to go HIGH which causes the output of U3B (U3 pin 6) to go LOW. When this output goes LOW it forces the other input to U3A (U3 pin 2) LOW which makes the circuit stable in this state until some input changes. This output (U3 pin 6) is also connected to the interrupt line of the display processor (U1 pin 6). When this pin goes low, the processor starts an interrupt sequence.

During the interrupt service routine, the display processor takes the read line (U1 pin 8) LOW which is connected to an input to U3B (U3 pin 5) and to the eight-bit data bus latch (U6 pin 1). When this happens, the output of U3B (U3 pin 6) goes HIGH, forcing one input to U3A (U3 pin 2) HIGH. If the other input to U3A is HIGH (U3 pin 1 interrupt strobe) the output of U3A (U3 pin 3) will go LOW which presents a LOW at U3 pin 4 and makes the circuit stable in this state until some input changes and this completes the cycle.

DISPLAY PROCESSOR D

The display processor is an 8049 microcomputer. It contains 128 bytes of RAM and 2K bytes of ROM program memory. This ROM contains all of the microcoded program to control the display processor. This microcomputer contains an eight-bit down counter which uses a prescaled (divided by 32) address latch enable (ALE) signal for its input clock. I/O consists of two 8-bit parallel ports which can be either input or output, and an 8-bit bi-directional bus.

The display uses the 128 bytes of RAM for internal registers, storage for the present characters being displayed in the numeric and alpha displays and for a command-First In First Out register (FIFO).

The instrument processor communicates with the display processor via the lower 8-bits of the 16-bit bidirectional bus; however, the display processor cannot send data back to the instrument processor. The instrument processor outputs command or data information to the display interface latch. The clock to this latch also sets the display service request latch. The display processor immediately takes the information present in the interface latch and places it on the bottom of the FIFO. Commands and data contained on the FIFO are executed sequentially when the display processor has time that is not required to refresh the numeric and alpha displays. This method provides the minimum response time to interrupts from the instrument processor and at the same time always provides flicker free display refreshing.

The oscillator circuit consists of a 10.92 MHz crystal connected to the internal oscillator circuit of the processor (U1 pins 2 and 3). A crystal is used rather than an LC circuit due to variations in oscillator frequency from unit to unit when a LC circuit is used. Refer to manufactures data sheet for a more detailed discussion of the processor.

U3C provides a clock signal (LE) to the two control Addressable Latches on the display driver board (A2). This clock line is required to be HIGH when the reset to these Addressable Latches is LOW so LOW Reset is NANDed with the LTE clock to force the above condition to occur.

ANNUNCIATOR LATCH/DRIVER E

When the annunciator strobe (LEN 5) goes LOW and then HIGH (U5 and U7 pin 9), the information on the instrument data bus is latched into the annunciator data latches. The outputs of these latches drive the inputs of the annunciator drivers (U4 and U8). The annunciators are located on the A2 Display Driver Board. Each annunciator is connected in series with a current limiting resistor to +12 volts. The resistor values were selected to make the apparent brightness to the eye the same on all annunciators.

The HighVoltage drivers (U4 and U8) provide sufficient current sink capability and allow the use of the +12 volt supply for the annunciators.

PRESET CIRCUITRY A

The preset circuitry has two purposes. The first is to allow the instrument preset signal to clear the annunciator LEDs and to reset the display processor. The second is to allow either the instrument preset signal or the display processor to clear the numeric display segment driver data latch.

The LIPS signal comes into the display to a schmitt trigger buffer (U9B pin 5) is inverted twice and appears at U9A pin 3 with polarity unchanged. This buffered LIPS directly clears the annunciator latches (U5 and U7 pin 1 in Block **E**) and directly resets the display processor (U1 pin 4 in Block **D**). This Low-True signal is ORed (U9D pin 12 and 13) with a Low-True signal from I/O Port P25 of the display processor (U1 pin 36). The output of the above gate (U9D pin 11) is inverted (U9C pin 10) to produce the Low-True clear (U9C pin 8) which is sent to the NUMERIC SEGMENT DRIVERS (A2 Block **A**).

ALPHA DISPLAY SHIFT REGISTER G

The alpha displays require row information in serial form. This shift register (U2) has its parallel inputs (U2 pins 3, 4, 5, 6, 12, 13, and 14) connected to the display data/address bus. When the display processor does a write, the write line (U1 pin 10 in Block **D**) goes LOW and forces the parallel load line (U2 pin 1) LOW. At that time, the data on the data bus is loaded into the shift register (U2). This information is then shifted serially to the alphanumeric integrated displays (A1, U1 through U7).

The alpha display clock synchronizes the transfer of serial data from the alpha display shift register (U2) into the serial shift registers contained within the alpha display integrated circuits.

The main sequence synchronization clock (LTE) is ANDed (U3D pin 12 and 13) with I/O Port P27 (U1 pin 38) from the display processor to produce the alpha display clock signal (U3D pin 11). This signal goes to the shift register (U2 pin 2) and to the alphanumeric integrated displays (A1, U1 through U7) and allows the display processor to control the number of bits shifted into the Alpha Display. This method of generating a clock produces the fastest transfer of serial information to the Alpha Displays. It also allows the processor to do other things, once the shift clock has been turned on, until it is time to turn the clock off.

DSA CONNECTOR F

Start, Stop, Clock and Ground are arranged in the same order as on

the HP 5005A Signature Analyzer pod. The DSA function is enabled by shorting the ground and DSA Enable lines on the DSA connector (TP5 and TP6) together and forcing the LIPS line LOW (momentarily) by pressing instrument preset or momentarily shorting LIPS to ground on the display.

Two additional pins (TP7 and TP8) are connected to +5.2 volts and U1 pin 7 (processor's External Access EA). When EA is tied to +5.2V it forces the processor to do all instruction fetches from external memory. This function may be useful for troubleshooting address/data bus problems.

DISPLAY SUPPLY C

The peak current required by the displays can be as high as 2 amps. However, the average current required is much less. These current peaks or transients caused by strobing the Alpha and Numeric displays cause spurs on the 8340A RF output.

A constant current source connected to the instrument +5.2 volt supply is provided so that a constant load will be seen by the instrument supplies. The output of this current source is then connected to the LED current source circuits along with a large amount of energy storage (five 220 uF capacitors). The current source provides slightly more than the average amount of current required by the LEDs, and the capacitors provide the additional current required during peak demands.

Q1, Q2, and U11B form the display current source. Q1 and Q2 increase the current capability of the current source. Disregarding U11A for the moment, the emitter of Q1 will be forced to the same voltage as the positive input of U11B by virtue of the voltage feed back through R9. The positive input (U11B pin 5) is fixed at one diode drop below the supply (+5.2VF). R5 therefore, has a constant voltage drop across it and produces the constant current for the display supply. The average current demanded by the displays changes as more or less segments or characters are turned on. In order to keep the current source in regulation during both high and low average current demands, it is necessary to make the current source adjustable. This is accomplished by sensing the voltage at the energy storage capacitors through R11. As this voltage goes down, indicating that the average current is not sufficient, the voltage at U11A pin 1 goes up. This causes an increase in the voltage across R5 and therefore will increase the current to the display supply. The current source should not track the output voltage or respond to variations caused by strobing segments and columns. This would defeat the whole purpose of the current source. To eliminate this problem, U11A is connected as a slow integrator. It responds only to slow variations in the average voltage at the display supply. R12 and R13 set the quiescent operating point of the current source. R11, R3 and C20 set the gain and speed of the integrated voltage feedback loop.

When the current source has been supplying a large amount of current and suddenly the requirement goes down, the current source will try to continue supplying this large current. The voltage at the output will rise until it cannot go any higher and then the current source will go out of regulation. This causes a current transient on the main supply to the display. VR1 and R6 are used to sink this excess current until the integrating feedback has time to reduce the average output current.

POWER SUPPLIES H

The power supply filtering is straight forward except for the choke (L2) in the +5.2 volt supply line. The intention of this choke is to further filter out conducted transients on the 5 volt supply caused by the processor, TTL circuitry, and other display circuitry that could not be connected to the current regulated supply due to the voltage variations of that supply. Spurs related to the display processor running are reduced by approx 15 dB by adding this filter choke.

A3 DISPLAY PROCESSOR TROUBLESHOOTING

REQUIRED EQUIPMENT

* VOM
* Oscilloscope (100 MHz)
* 5005B Signature Analyzer (If DSA troubleshooting is used)
* Logic probe

PREPARATION

1. Measure the power supply voltages on the A3 Display Processor by connecting the VOM common lead to GROUND (TP10) and checking the -5.2V (TP11), +5.2V (TP13) and +12V (TP14) supplies for proper voltages.

2. If the supplies are correct, refer to Figure 8H-4 through 8H-7 and remove the front panel, separate the display assembly from the keyboard and reattach the keyboard to the frame.

3. Remove eight screws from the display assembly holding the A3 Display Processor in place. Turn the Display Processor over and reinsert the other end of P1 through P5 into the same sockets they came out of and install two screws to hold it in place.

4. The resulting position of the two display boards (shown in Figure 8H-7) is called the Service Position and allows most of the following troubleshooting to take place.

5. Place the display into the self-test mode by pressing **[SHIFT] [FREE RUN]**.

SYMPTOMATIC TROUBLESHOOTING

Display RAM Test Fails

1. Replace A3U1

Display Checksum Not Equal To "3A"

1. The display checksum is shown in the ENTRY DISPLAY during the front panel diagnostics. Press **[SHIFT] [FREE RUN]** and determine if the checksum is equal to 3A. If not, replace A3U1.

Numeric And ENTRY Displays Are Dim

1. Check Display Supply voltage (A3P5 pin 1,2) with an oscilloscope. This voltage should be 4.0V with 430 Hz 0.6V p-p ripple. If this voltage is low (< 3.2V), the displays are

likely to be dim and if this voltage is less than about 2.0V the displays will be blank. If this voltage is not correct, troubleshoot the Display Supply (A3 Block **C**).

Both Numeric And ENTRY Displays Are Blank

1. Check LRESET (A3TP12) and CLR (A3P1 pin 1). If either is LOW, troubleshoot PRESET CIRCUITRY (A3 Block **A**).

2. Check the Display Supply voltage (A3P5 pin 1 and 2) with an oscilloscope. This voltage should be 4.0V with 430 Hz 0.6V pk-pk ripple. If this voltage is low (< 3.2V), the displays are likely to be dim and if this voltage is less than about 2.0V the displays will be blank. If this voltage is not correct, troubleshoot the DISPLAY SUPPLY (A3 Block **C**).

3. If both LRESET and CLR are HIGH and the display supply voltage is 4.0V or greater then proceed to **All Numeric Displays Are Blank,** and **ENTRY DISPLAY Is Blank** troubleshooting procedures.

All Numeric Displays Are Blank

1. Connect the oscilloscope to CLK test point (A2TP6). Set it to 0.5 us/div and 1 V/div (0V = center screen). The waveform displayed should be LOW for 2.5 to 3.0 us with levels between +2V and approximately -2.5V. If this signal is not present, troubleshoot the NUM CLK in LEVEL SHIFTERS (A2 Block **F**).

2. Troubleshoot CONTROL DATA LATCH (A2 Block **H**).

3. Troubleshoot NUMERIC SEGMENT DRIVERS (A2 Block **A**).

Entry Display Is Blank

1. Connect oscilloscope to ALPHA CLK (A2TP2). Set the oscilloscope to 0.5 uS/div and lV/div (0V=Center screen). The waveform displayed should be TTL LOW-going pulses 0.3 uS wide with a period of 1.4 us. If this signal is not present, troubleshoot Alpha Display Clock Control in the ALPHA DISPLAY SHIFT REGISTER Block (A3 Block **G**).

2. Connect oscilloscope to DATA (A2TP1). Set the oscilloscope as above. The waveform display should indicated both HIGH and LOW signal levels approximately 1.4 us wide. If the DATA signal is always LOW, all LEDs in the ENTRY DISPLAY will be off. If this signal is not present, troubleshoot the ALPHA DISPLAY SHIFT REGISTER (A3 Block **G**).

3. Troubleshoot the CONTROL DATA LATCH (A2 Block **H**).

The Same Segment(s) Is Missing In Each Numeric Digit

1. Troubleshoot the NUMERIC SEGMENT DRIVERS (A2 Block **A**).

The Same Column Is Missing In Each ENTRY DISPLAY Character

1. Troubleshoot the ALPHA COLUMN DRIVERS (A2 Block **I**).
2. Troubleshoot the CONTROL DATA LATCH (A2 Block **H**).

One Entire Numeric Display Is Blank

1. Troubleshoot the appropriate STRT signal in the LEVEL SHIFTERS Block (A2 Block **F**).
2. Troubleshoot the appropriate SHIFT REGISTER/NUMERIC DIGIT DRIVER (A2 Block **G**).

The Display Goes Into Self Test When The 8340A Is Turned ON And Does Not Respond To Normal Instrument Functions

1. Troubleshoot the INSTRUMENT BUS INTERFACE (A3 Block **B**).

A3 DISPLAY PROCESSOR BLOCK-BY-BLOCK TROUBLESHOOTING

Preset Circuitry (A3 Block A)

1. Check LRESET (A3TP12) voltage. This should be a TTL HIGH. Now press **[INSTR PRESET]** on the front panel; LRESET should go LOW. If LRESET is correct, proceed to step 6.

2. Probe LIPS at A3U9B pin 5. LIPS should also be HIGH normally and should go LOW when you press **[INSTR PRESET]**. If LIPS is correct, proceed to step 4.

3. Check LIPS at the Instrument end of the ribbon cable and replace the ribbon cable if necessary.

4. Lift A3U9 pin 3 and retest LRESET right at pin 3.

5. If LRESET is still incorrect, replace A3U9. If LRESET is now correct, first suspect A3C21 is shorted. If this capacitor is not shorted look for evidence of a shorted trace associated with this signal. If no shorted trace exists then determine which of the following devices is holding LRESET down:

   A3U5 pin 1
   A3U7 pin 1
   A3U1 pin 4

6. Probe CLR at A3U9C pin 8 or A3P1-1. Set the oscilloscope to 0.2 ms/div and 1 V/Div. The CLR signal should be a continuous series of LOW pulses approximately 1 ms wide and 4 ms apart. Press **[INSTR PRESET]** and CLR should go LOW and remain LOW until the key is released. If both LRESET and CLR are correct, the Preset Circuitry is performing correctly. If CLR is not correct, proceed with step 7.

7. Disconnect the Display Processor board (A3) from the Display Driver board (A2) and repeat step 6. If CLR is now correct, suspect a shorted trace or a shorted input to A2U9 on the A2 Display Driver board.

8. If the CLR signal remains either HIGH or LOW, lift A2U9 pin 8 and check CLR right at the pin. If CLR is now correct, troubleshoot for a short to the CLR signal trace on the A3 Display Processor board.

9. Replace A3U9.

Instrument Bus Interface (A3 Block B)

ANNUNCIATORS ALL STAY ON AFTER **[INSTR PRESET]**

NOTE

If all the annunciators remain lit at power up (similar to holding [INSTR PRESET] in), the instrument processor may not be running. Check the negative power supplies.

1. If the annunciators all stay on after **[INSTR PRESET]**, the Load Strobe (LEN 5) from A3U10 may be bad. To check this, Direct I/O Addressing is used to manually generate the strobe. Press the following key sequence:

   [SHIFT] [GHz] [15] [Hz]
   [SHIFT] [MHz] [0] [Hz]
   [SHIFT] [kHz]

2. Probe LEN5 (A3U10 pin 10) with an oscilloscope while rotating the RPG. Set the oscilloscope to 0.2 us/div and 2 V/div. Rotating the RPG will cause a series of writes to the annunciator's address and there should be LOW going pulses approximately 300 ns wide displayed on the oscilloscope. A logic probe may also be used to detect pulses at this location. If the pulses are present, troubleshoot the Annunciator Latch/Driver (Block **E**).

3. Probe SIOA (A3U10 pin 4) while rotating the RPG. You should again find 300 to 400 ns wide, LOW going pulses. If SIOA is pulsing, proceed to step 5.

4. Probe SIOA on the Motherboard end of the ribbon cable. If SIOA is pulsing, replace the ribbon cable. If SIOA isn't pulsing, troubleshoot the A60 Processor.

5. Check each of the address bits (A0 thru A4 A3U10 pins 5, 2, 3, 6, and 1) for bus activity while the 8340A is sweeping. The lack of activity on any one of these address bits probably indicates that a wire is open in the front panel ribbon cable.

6. Lift A3U10 pin 10 and again check for pulses as in step 2. If pulses now appear at A3U10 pin 10 then check for shorts along LEN5 or troubleshoot the Annunciator Latch/Driver (A3 Block **E**). If after lifting pin 10 pulses still do not appear at pin 10 then replace A3U10.

FRONT PANEL ENTERS DISPLAY SELF TEST MODE AT POWER ON

1. If the Front Panel enters the display self test mode when power is turned on and the main instrument processor is

working, the display processor is probably not receiving interrupts. The interrupt strobe (LEN 7) from A3U10 may be bad. To check this, Direct I/O Addressing is used to manually generate the strobe. Press the following key sequence:

[SHIFT] [GHz] [15] [Hz]
[SHIFT] [MHz] [2] [Hz]
[SHIFT] [kHz]

2. Probe A3U10 pin 7 (LEN 7) with an oscilloscope while rotating the RPG. Set the oscilloscope to 0.2 us/div and 2V/div. Rotating the RPG will cause a series of writes to the display's address. There should be LOW going pulses approximately 300 ns wide displayed on the oscilloscope. A logic probe may also be used to detect pulses at this location. If the pulses are present, proceed to step 7.

3. Probe SIOA (A3U10 pin 4) while rotating the RPG. You should again find 300 to 400 ns wide, LOW going pulses. If SIOA is pulsing, proceed to step 5.

4. Probe SIOA on the Motherboard end of the ribbon cable. If SIOA is pulsing, replace the ribbon cable. If SIOA isn't pulsing, then troubleshoot the A60 Processor.

5. Check each of the address bits (A0 thru A4 A3U10 pins 5, 2, 3, 6, and 1) for bus activity while the 8340A is sweeping. The lack of activity on any one of these address bits probably indicates that a wire is open in the front panel ribbon cable.

6. Lift A3U10 pin 7 and again check for pulses at pin 7 as in step 2. If pulses now appear at A3U10 pin 7 then check for shorts along LEN7 or at the input of U3 or U6. If after lifting pin 7, pulses still do not appear then replace A3U10.

7. Probe LIRQ (A3U3 pin 6). You should expect LOW going pulses between 10 and 25 us wide to appear each time the display is addressed (LEN 7 pulsed). This time varies due to differences in the response time of the display processor to interrupts from the instrument processor. If pulses are present at LIRQ, the Service Request Latch is operating properly.

8. If LIRQ never goes LOW then check for LOW going pulses at A3U3 pin 4 each time the display is written to. If there are no pulses then replace A3U3.

9. Check the level of LREAD signal (A3U3 pin 5). LREAD should be HIGH normally and will go LOW for 700 ns each time the display processor accepts an interupt request.

10. If LREAD stays LOW, this will prevent LIRQ from going LOW. Inspect along the READ signal trace for evidence of a short.

If no short exists then lift A3U6 pin 1 to determine if its input is shorted to ground. If LREAD stays LOW after lifting this pin, then you must suspect that the processor A3U1 is bad and must be replaced.

DISPLAY REMAINS BLANK OR HAS GARBLED MESSAGES

If the display remains BLANK or has garbled messages and numbers in the displays, one or more of the data bits may not be getting to the display processor. To check this you may use Digital Signature Analysis (DSA) or you may do the following manual verification:

1. Set up the 8340A to write to the Display using Direct I/O Addressing. Press

   [SHIFT] [GHz] [15] [Hz]
   [SHIFT] [MHz] [2] [Hz].

2. Turn off the display updating by pressing **[SHIFT] [CONT].**

3. Turn the 8340A POWER switch to the STANDBY position.

4. Connect LRESET (A3TP12) to GROUND (A3TP10).

5. Connect EA (A3TP8) to +12V (A3TP14).

6. Connect READ (A3TP9) to GROUND (A3TP6).

7. Turn the 8340A POWER switch to the ON position.

8. Press the following keys to write a "0" to the Display Interface Latch: **[SHIFT] [kHz] [0] [Hz].**

9. Check each output of the interface latch (A3U6 pins 2, 5, 6, 9, 12, 15, 16, and 19) for being LOW.

10. Press the following keys to write all "1s" to the Display Interface Latch: **[255] [Hz].**

11. Check each output for a HIGH level.

12. If any of the outputs are not HIGH or LOW when they should be, check the ribbon cable for opens or replace A3U6.

Display Supply [A3 Block C]

If the +5.2V power supply is correct yet the Display Supply is not, then you must troubleshoot the Display Supply as follows:

DISPLAY SUPPLY VOLTAGE < 3V

If the Display Supply voltage is below approximately 3 volts, neither the numeric displays nor the entry display will light up with the proper intensity. If the Display Supply is below approximately 2V, all of the LEDs will be off.

1. Measure the output of U11B (pin 7). Under normal conditions, this voltage should be approximately 3.3 volts. If this output (U11B pin 7) is approximately 0.1 to 0.2 volts, it is likely that either Q1 or Q2 is open. Check Vbe on Q1 and then Q2 to help determine which is at fault. If this output (U11B pin 7) is near 5 volts, CR12 may be shorted or U11 is bad.

2. Measure the voltage at U11B pin 5. This voltage should be approximately 4.3 volts (one diode drop below the supply). If this voltage is greater than 4.3V, either CR1 is shorted, R8 is open, or the input to the U11A (pin 5) is damaged.

3. If all of the above is correct, check U11A. If Q1 is saturated or shorted, U11A's output voltage is limited to approximately +5.5V when the Display supply is between 0V to 3.7V. If a voltage outside this range appears, suspect U11A or the associated resistors. If C20 is shorted it will cause the Display supply voltage to be too low.

4. Measure the voltage at U11A pin 3. It should be approximately 4V. If it is not, measure the voltage between U11A pin 2 and pin 3. If the voltage between U11A pins 2 to 3 is not 0V, either R11 is shorted or else U11 is bad. If this voltage is 0V, suspect that either R12 or R13 is bad or is an incorrect value causing the operating point of the current source to be incorrect.

DISPLAY SUPPLY VOLTAGE > 4.2V

If the Display supply average voltage is above approximately 4.2V, the current source is not regulating. If the display supply voltage is above about 4.4V, it is likely that VR1 is open in addition to other problems. Either condition will cause excessive current fluctuations on the +5.2V supply which will be conducted and radiated to sensitive circuits inside the 8340A. This will result in unwanted spurious signals on the output at 80 Hz, 400 Hz, 2.5 kHz and 5 kHz away from the output frequency.

1. Check the collector to emitter voltage of A3Q1. If this voltage is less than about 0.15V, Q1 is likely shorted and should be replaced.

2. Check the collector to emitter voltage of A3Q2. This voltage should be approximately 3.6V. If Vce is less than about 0.08V, Q2 is likely shorted. If Vce is 0.1V to 3.5V, Q2 is being over-driven by U11B. Lift one end of R11 to break the feedback from the Display Supply.

3. Determine if U11A is operating correctly by measuring the voltage at U11A pin 3 and at U11A pin 1. These two voltages should both be very close to being the same and should be approximately 3.9V to 4.0V. If the voltage at U11A pin 3 is not near 4.0V, either R12, R13, or U11 is bad and should be replaced. If the voltage at pin 3 is about 4.0V but the output (pin 1) is not, either a trace is shorted or U11A is bad.

4. If the output of U11A is correct, measure the voltage at U11B pin 5. This voltage should be about 4.2 to 4.3 volts. If this voltage is near ground, CR1 is likely open which will cause the display supply to be saturated.

3. If all measurements up to this point are correct yet the Display supply is still saturated, replace U11.

Display Processor Section (A3 Block D)

If you have reason to suspect that the Display Processor is at fault, start by determining if all of the inputs to the processor are correct.

1. Measure the following points and verify that the corresponding voltages are present.

   A3U1 pin 40 - +5 volts

   LRESET (A3U1 pin 4) - HIGH

   LIRQ (A3U1 pin 5) - HIGH

   EA (A3U1 pin 7) - LOW

   A3U1 pins 5 and 25 - HIGH

2. Probe LTE (A3U1 pin 11) with an oscilloscope. Set the oscilloscope to 1 us/Div. This signal should have a period of approximately 1.4 us and should be LOW for 1 us. If LTE is present, proceed to step 7.

3. Probe the two sides of the crystal (Y1) with the oscilloscope set to 50 ns/Div. You should find a 10.92 MHz, 4V signal on both sides. If the signal is present, proceed to step 6.

4. Check both C1 and C2 to see if either is shorted and replace if necessary. If either C1 or C2 are replaced, repeat step 2.

5. If C1 and C2 are not shorted, replace Y1 and repeat step 2.

6. If LTE is still not present, verify that the trace for LTE is not shorted. If LTE is not shorted, U1 should be replaced.

7. Probe LE (A3U3C pin 8) with the oscilloscope set to 1 us/div. You should find an inverted version of LTE. Press **[INSTR PRESET]** and LE should go HIGH.

If all other signals are correct, the remaining outputs from the processor are best checked using DSA as described in the **DISPLAY ASSEMBLY DSA TROUBLESHOOTING.** However, you can use the internal DSA routine (documented below) to exercise all of the processor outputs in a predictable manner and look at the outputs with a scope.

NOTE

If any of the following signals are not present or are not the correct amplitude (minimum of 4V except for CLK), you should troubleshoot the block that the signal is connected to or replace A3U1 as appropriate.

1. Connect DSA EN (A3TP5) to GND (A3TP4).

2. Turn the POWER switch to STANDBY and then ON again to start DSA mode.

3. Set the oscilloscope to 1 us/Div and trigger off of the appropriate edge of the signal.

4. Probe D0 through D7 (U1 pins 12 through 19). You should find LOW going TTL Level pulses which are 1 to 2 us wide.

5. Probe P10 through P17 (U1 pins 27 through 34). You should find HIGH going TTL Pulses which are 3 to 4 us wide.

6. Probe P25 and P27 (U1 pins 36 and 38). You should find HIGH going TTL pulses which are 3 to 5 us wide.

7. Probe CLK (U1 pin 37). You should find HIGH (1.6V) going pulses which are 3 to 4 us wide. This signal is clamped to 1.6V by the LEVEL SHIFTERS on the A2 Board.

8. Probe START (U1 pin 35) with the oscilloscope. Set the oscilloscope to 10 ms/Div. You should find a signal that is HIGH for approximately 12 ms and LOW for approximately 21 ms.

Annunciator Latch/Driver (A3 Block E)

NOTE

If all of the annunciators stay on after instrument preset yet the rest of the display and the keyboard are correct, first trouble-

shoot the PRESET CIRCUITRY (Block A) and then the INSTRUMENT BUS INTERFACE (Block B).

NOTE

The Annunciator Latch/Driver can be partially troubleshot using DSA as explained in DISPLAY ASSEMBLY DSA TROUBLESHOOTING.

ONE OR MORE ANNUNCIATORS ERRONEOUSLY ON OR OFF

1. If one or more annunciators are ON or OFF when they should not be, verify that the appropriate outputs of A3U5 & U7 are LOW if the associated annunciator is on, and HIGH if the annunciator is OFF. If the output of U5 and U7 are correct, proceed to step 3.

2. Determine if the output of U5 or U7 is bad or if the input to U4 or U8 is shorted. This can be accomplished by lifting the output pin of U5 or U7 and repeating step 1.

3. Verify that the associated output of U4 or U8 is in the correct state (see **NOTE** below). The output of U4 or U8 should be approximately 0.2V if the annunciator is ON, and 6.5 to 9V if the annunciator is off. If the outputs of U4 and U8 are correct, the Annunciator Latch/Driver is operating correctly.

NOTE

Since the outputs of U4 and U8 are open collector outputs, an open trace, open series resistor, or open annunciator will allow the output of U4 or U8 to stay LOW all the time. If you suspect one of the above faults, you should attach a 1K ohm pullup resistor between your probe and the +5 V supply. The levels will then be 0.1 or 5 V if the driver is working correctly.

ONE OR MORE ANNUNCIATORS ARE ERRONEOUSLY OFF

1. If all of the annunciators are off, check the +12V supply on the A2 Display Driver board.

2. If one or several annunciators are off when they should be on and you have already determined that Annunciator Latch/Driver (Block **E**) is operating correctly, check for +12V right at the annunciator on the A2 Display Driver Board.

3. If +12V does not appear at the annunciator, look for an open trace along the top edge of the A2 board. If +12V is present, replace the annunciator.

DSA Connector (A3 Block F)

The function and use of the DSA (Digital Signature Analysis) Connector is explained in **DISPLAY ASSEMBLY DSA TROUBLESHOOTING.**

Alpha Display Shift Register (A3 Block G)

1. If the Entry display is either BLANK or ALL dots are ON, it is possible that this circuitry is malfunctioning. Press **[SHIFT] [FREE RUN]** to run the front panel display diagnostics. Set an oscilloscope up to display TTL levels at 2 us/Div.

2. Probe the display's clock signal (ALPHA CLOCK) at P4-4 with the oscilloscope. You should find a series of seven 0.3 to 0.4 us wide, LOW going pulses. If these pulses are present, proceed to step 5.

3. Probe U3D pin 11 for the pulses described in step 2. If there is still no signal at U3D pin 11 then check LTE (U3D pin 13) for a continuous series of HIGH going pulses 0.36 us wide and a period of 1.36 us. If no signal appears then troubleshoot DISPLAY PROCESSOR (A3 Block **D**).

4. If LTE appears correctly at U3D pin 13 then probe CLK CTL (U3D pin 12). You should find approximately 10 us wide, HIGH going pulses which are used to gate on the clock pulses to the alpha displays. If no signal appears then troubleshoot the DISPLAY PROCESSOR (A3 Block **D**). If both LTE and CLK CTL are correct, replace U3.

5. Probe A3U2 pin 1 with the oscilloscope. You should find approximately 0.8 us wide, LOW going TTL pulses. If there are no pulses then you should troubleshoot the DISPLAY PROCESSOR (A3 Block **D**).

6. Probe DATA (A3U2 pin 9) with the oscilloscope. You should find TTL activity in bursts of seven which correspond in time with the seven clock pulses at P4-4. If this activity is present, then the Alpha Display Shift Register is working.

7. If the activity described in step 6 is not present, lift U2 pin 9 and recheck for activity. If no activity exists after lifting pin 9, replace U2. If activity resumes, check this signal line for shorts on any of the A1, A2 or A3 assemblies. If no shorts exist, troubleshoot the A1 Alpha Display.

A3 DISPLAY PROCESSOR DSA TROUBLESHOOTING

Overview of DSA Options

OPTION 1

The display processor can be forced to repetitively count through its entire address space. A signature analyzer can then be used to determine if the correct signatures appear on D0 through D7, A8 through A10, and +5VF.

OPTION 2

The DSA routine contained in the display processor's memory can be used by enabling the DSA mode and using a signature analyzer to determine if the correct signatures appear on D0 through D7, A8 through A10, the Parallel I/O Ports and many other signal lines. This routine is not able to check the annunciator latches or drivers, the instrument bus interface latches, or any of the signals on the display driver board which have non-TTL levels.

OPTION 3

The main instrument DSA routine can be used to stimulate the annunciator latches, the address decoder and the instrument bus interface latch. A signature analyzer may then be used to determine if the correct signatures appear on these lines.

Freerun DSA (Option 1)

The Freerun DSA mode is selected by connecting EA (A3TP8) to +5.2VF (A3TP7). This forces the processor to do all instruction fetches from external memory. Since there is no external memory and D0 through D7 are pulled up, the front panel processor will fetch FF Hex instruction op codes which does not alter the program counter. After executing this instruction the processor will increment its program counter and do an instruction fetch from the next location and will therefore repetitively count through its entire memory space.

1. Connect EA (A3TP8) to +5.2V (A3TP7) to enable the Freerun DSA mode. Connect the signature analyzer as follows:

   START and **STOP** connected to A10 (A3U1 pin 23), trigger on falling edge.

   CLOCK connected to LE (A3U3 pin 8), trigger on leading edge.

2. Probe the signals listed in the table below with the signature analyzer and verify that the signatures correspond to those given.

Mneumonic	J1 pin #	Signature
D0	11	H62U
D1	10	C21A
D2	9	HA07
D3	8	H0AA
D4	7	P030
D5	6	4442
D6	5	4U2A
D7	4	0772
A8	1	9635
A9	2	1734
A10	3	8P54
+5.2VF	17	7A70

DSA Using The Routine Contained In Display Memory (Option 2)

1. Connect DSA EN (A3TP5) to GND (A3TP6) to enable the internal DSA routine. Connect the signature analyzer as follows:

   START connected to A3TP1, trigger on falling edge.

   STOP connected to A3TP2, trigger on leading edge.

   CLOCK connected to A3TP3, trigger on rising edge.

   GRND connected to A3TP4.

   The +5.2V Signature under these conditions should be H9U2. This indicates that all processor instructions are being executed correctly, the ROM checksum is correct and that the internal RAM is good.

2. Set the **START** polarity to trigger on the leading edge.

3. Set the **STOP** polarity to trigger on the falling edge.

4. Probe the signals listed in the table below with the signature analyzer and verify that the signatures correspond to those given.

Mneumonic	Location	Signature
D0	A3U1 pin 12	CPAC
D1	A3U1 pin 13	20U1
D2	A3U1 pin 14	5P21
D3	A3U1 pin 15	8F24
D4	A3U1 pin 16	FP86
D5	A3U1 pin 17	023P
D6	A3U1 pin 18	185F
D7	A3U1 pin 19	H576
P10	A3U1 pin 27	C606
P11	A3U1 pin 28	06F6
P12	A3U1 pin 29	5868
P13	A3U1 pin 30	39C4
P14	A3U1 pin 31	H2A6
P15	A3U1 pin 32	5FC3
P16	A3U1 pin 33	3U26
P17	A3U1 pin 34	PP24
A8	A3U1 pin 21	4218
A9	A3U1 pin 22	162P
A10	A3U1 pin 23	131U
START	A3U1 pin 35	F81C
P25	A3U1 pin 36	CH4A
NUM CLK	A3U1 pin 37	20PA
CLK CTL	A3U1 pin 38	0H8P
ALPHA CLOCK	A3U3D pin 11	F81C
	A3U9D pin 11	7551
CLR	A3U9C pin 8	CH4A
DATA	A3U2 pin 9	F033
LVL START	A2U3 pin 9	36PH
F1 START	A2U3 pin 10	324H
F2 START	A2U3 pin 12	5746

DSA Using The Instrument's DSA Routine (Option 3)

The 8340A's main processor has incorporated a general purpose DSA routine which exercises all of the I/O addresses. This can be enabled by connecting LSTS test point on the processor to ground.

1. Connect LSTS (A60TP13) to ground. Connect the signature analyzer as follows:

   START connected to HSTM (T1) on the A61 Memory board, trigger on the rising edge

   STOP connected to LSOB (T2) on the A61 Memory board, trigger on the rising edge

   CLOCK connected to LIOSB (A60TP4), trigger on the rising edge

   GRND connected to GND test point on the A61 Memory board.

When the instrument is turned on, the instrument will continually send out signatures to each output address. The information contained on the data bus is latched into the eight bit latch contained on the display processor board when its I/O strobe is addressed. In order to get this latched information onto the internal display data bus, the display processor must be forced to 3-state all of its data/address bus drivers and control line drivers. When this is accomplished, the output enable of the input latch (A3U6 pin 1) can be pulled low which will cause the outputs of A3U6 to drive the internal data/address bus with the bit pattern stored there by the instrument processor. The above can be accomplished by making the following connections on the display processor:

2. Connect LRESET (A3TP12) to GND (A3TP5).

3. Connect EA (A3TP8) to +12VF (A3TP14).

4. Connect LREAD (A3TP9) to GND (A3TP5).

5. Probe the signals listed in the table below with the signature analyzer and verify the signatures correspond to those given.

Mneumonic	Location	Signature
DB0	J2-3	H186
DB1	J2-4	CFPH
DB2	J2-5	H077
DB3	J2-6	0942
DB4	J2-7	CC29
DB5	J2-8	63CP
DB6	J2-9	F77H
DB7	J2-10	2757
ADR0	J2-23	AUCU
ADR1	J2-24	U154
ADR2	J2-25	012F
ADR3	J2-26	8U24
ADR4	J2-27	7UUF
SIOA	J2-49	1714
D0	A3U6 pin 12	5056
D1	A3U6 pin 15	A239
D2	A3U6 pin 9	46P7
D3	A3U6 pin 6	8U5C
D4	A3U6 pin 16	1F22
D5	A3U6 pin 5	73C7
D6	A3U6 pin 19	P76U
D7	A3U6 pin 2	FF4C
LEN 5	A3U10 pin 10	2563
LEN 7	A3U10 pin 7	52CA

6. In order to check the latched information in the annunciator latches (U5 and U7) the three jumpers installed in steps 2, 3, and 4 must be removed. Switch the instrument to STANDBY when removing these jumpers or be sure to remove the jumper between +12V and EA first.

7. Probe the signals listed in the table below with the signature analyzer. Verify that the signatures correspond to those given.

Mneumonic	Location	Signature
CF	A3U5 pin 2	A18U
DELTA F	A3U5 pin 5	9A09
START/STOP	A3U5 pin 7	PH05
CW	A3U5 pin 10	031F
UNLVLD	A3U5 pin 12	HU2P
FAULT	A3U5 pin 15	508P
OVERMOD	A3U7 pin 10	H05A
OVEN	A3U7 pin 12	A0C4
EXT REF	A3U7 pin 15	4169
UNLK	A3U7 pin 2	15HH
SRQ	A3U7 pin 5	U2AH
REMOTE	A3U7 pin 7	3F4F

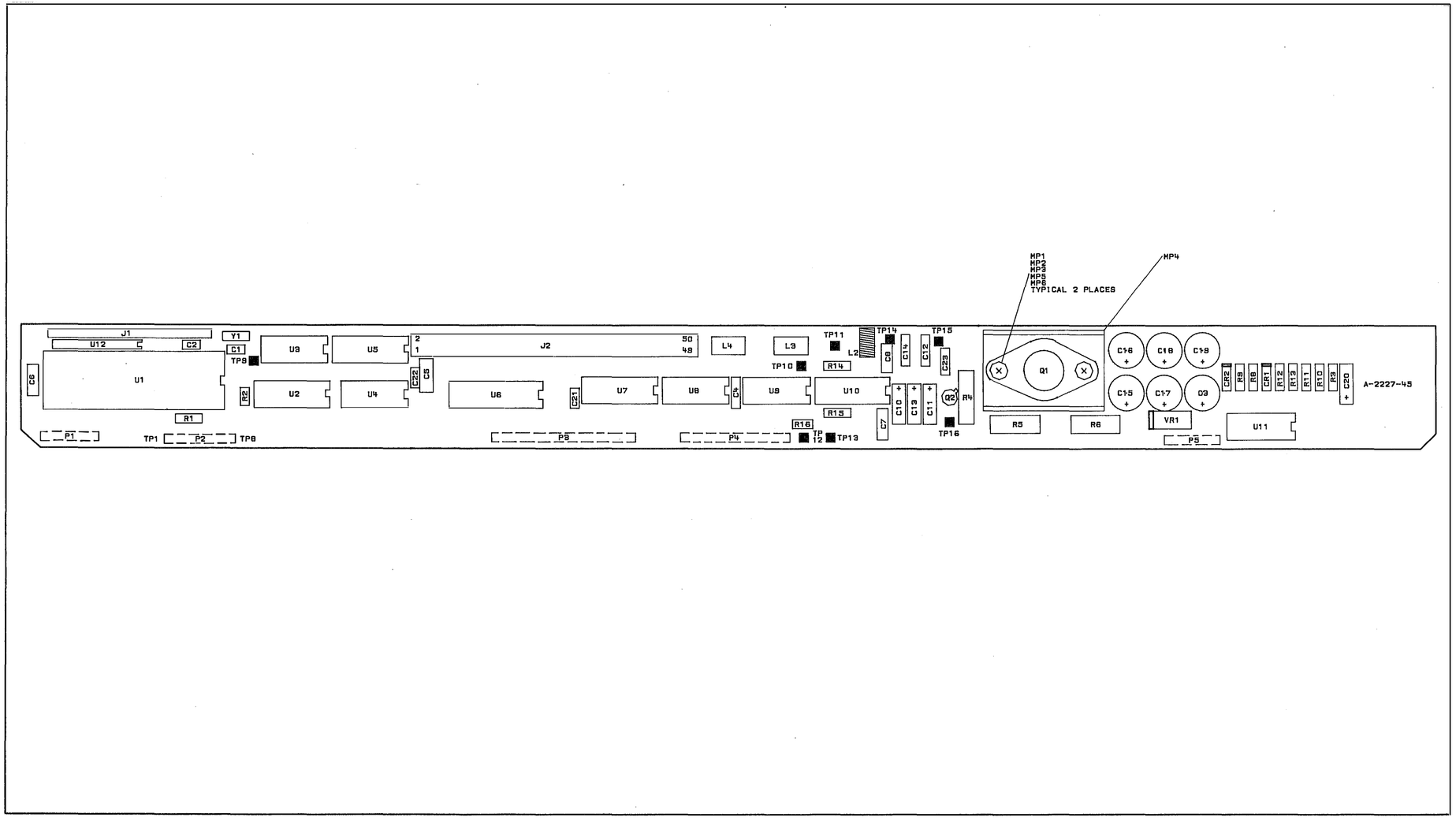


Figure 8H-13. A3 Display Processor, Component Location Diagram

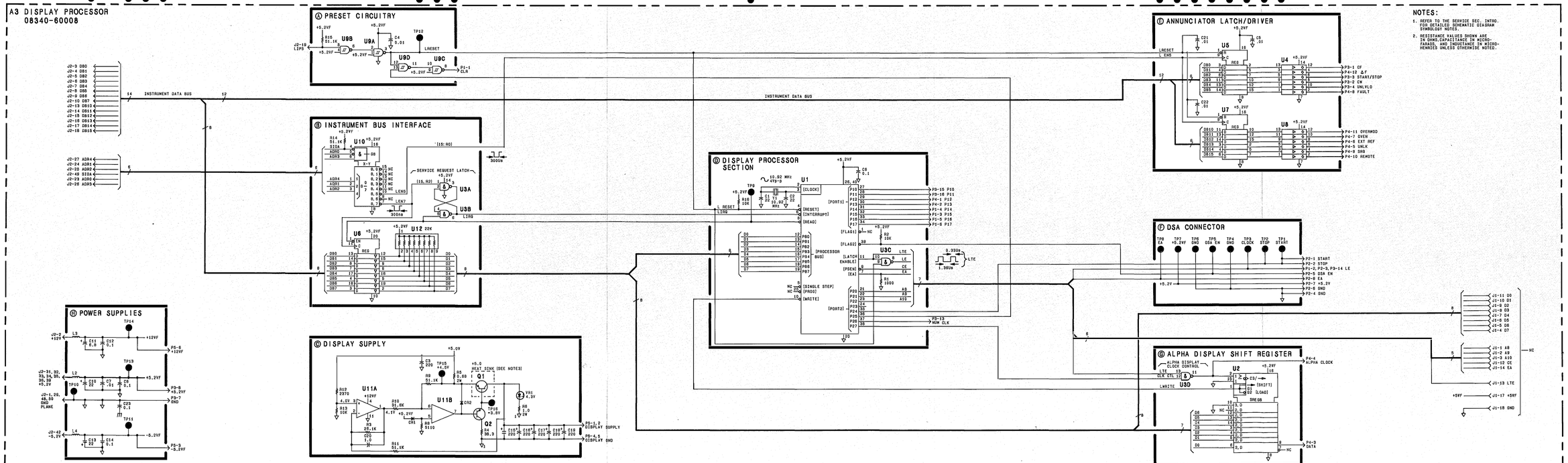


Figure 8H-14. A3 Display Processor, Schematic Diagram

A5 KEYBOARD AND A7 LOWER KEYBOARD, CIRCUIT DESCRIPTION

The keyboard section includes the A5 Keyboard Assembly and the A7 Lower Keyboard Assembly. Since both assemblies operate in the same manner, they will be covered together in the circuit descriptions below.

MAIN KEYBOARD B AND LOWER KEYBOARD B

The two keyboards contain 58 keys which have a multi-finger contact structure. Each key shorts one column line and one row line to digital ground.

There is not a general pattern followed for the encoding of the rows and columns, however, it may be necessary to determine what row and column each key translates to during troubleshooting.

ANNUNCIATORS A

The annunciator LED's are driven from latches on the A6 board.

A5 KEYBOARD AND A7 LOWER KEYBOARD TROUBLESHOOTING

ANNUNCIATORS (A5 AND A7 BLOCK A)

1. If one of the front panel LEDs stays on all the time, troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**).

2. If one of the front panel LEDs never comes on, even when **[INSTR PRESET]** is pressed, the cause is most likely a bad LED. To determine if the output of the latch is correct, probe the appropriate output of A6U6, A6U7, A6U16, or A6U17 and press **[INSTR PRESET]**. The voltage at this output should be approximately 0.4V if the latch is working correctly. If the voltage is correct, replace the appropriate LED. If the voltage is incorrect, troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**).

MAIN KEYBOARD (A5 BLOCK B) AND LOWER KEYBOARD (A7 BLOCK B)

1. Determine the ROW number and the COLUMN number of the key which is not working correctly. Probe the appropriate ROW and then the appropriate COLUMN at A6U1 or A6U10. Each signal should go LOW (0V) when the key is pressed.

2. If the row or column signal stays HIGH all of the time, even when the associated key is pressed, check for an open connector between the A5 or A7 keyboard and the A6 controller board. If no open trace or connector is found, replace the key pushbutton.

3. If the row or column signal stays LOW all of the time, even when the associated key is not pressed, measure the resistance of this signal line to ground. If the resistance is 1 ohm or less, either the signal trace must be shorted to ground or the key pushbutton is broken and is shorting the trace to ground. If the resistance is greater than 1 ohm, the associated input to A6U1 or A6U10 is probably shorted. Replace either U1 or U10 as appropriate.

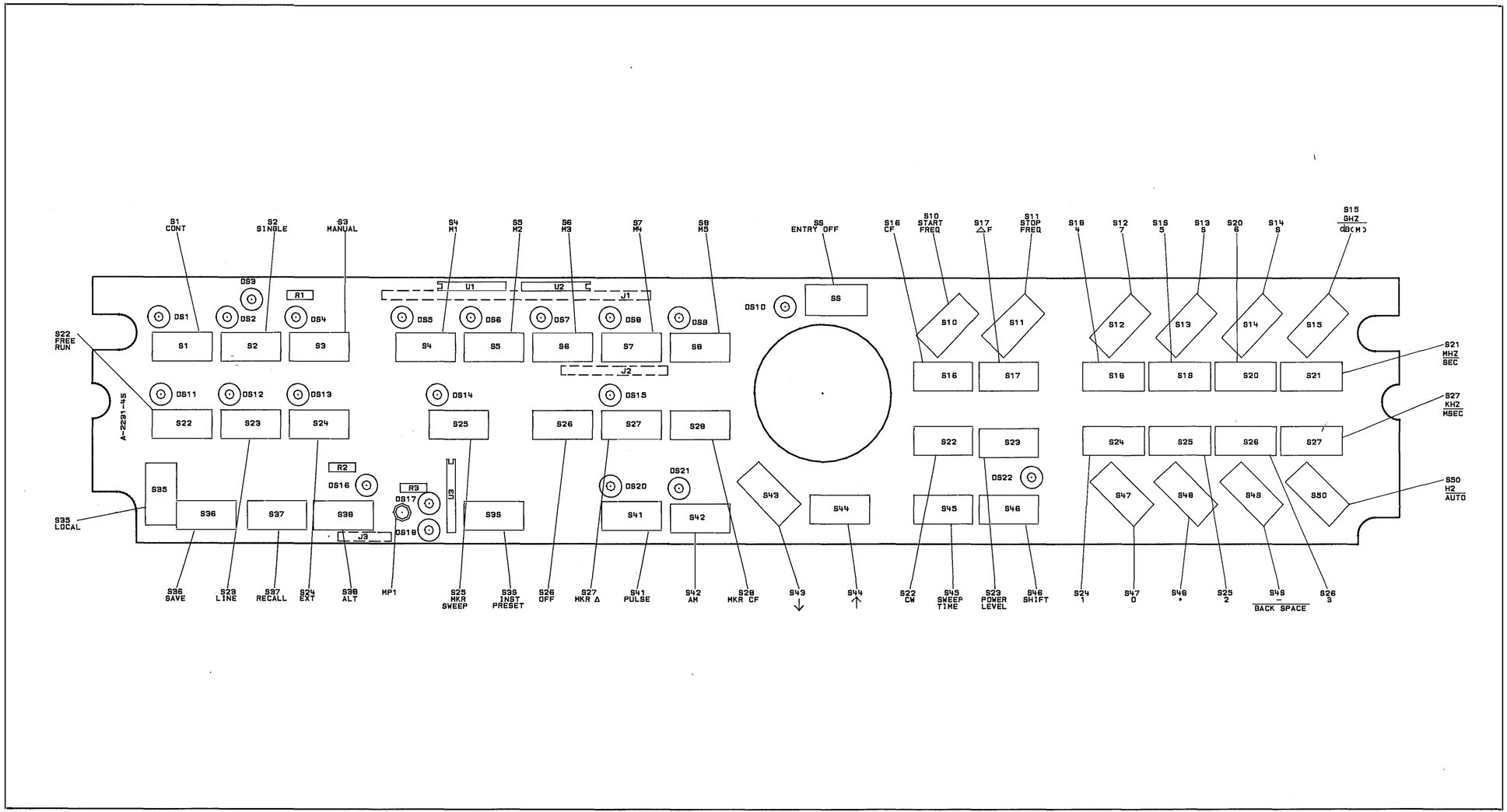


Figure 8H-15. A5 Keyboard, Component Location Diagram

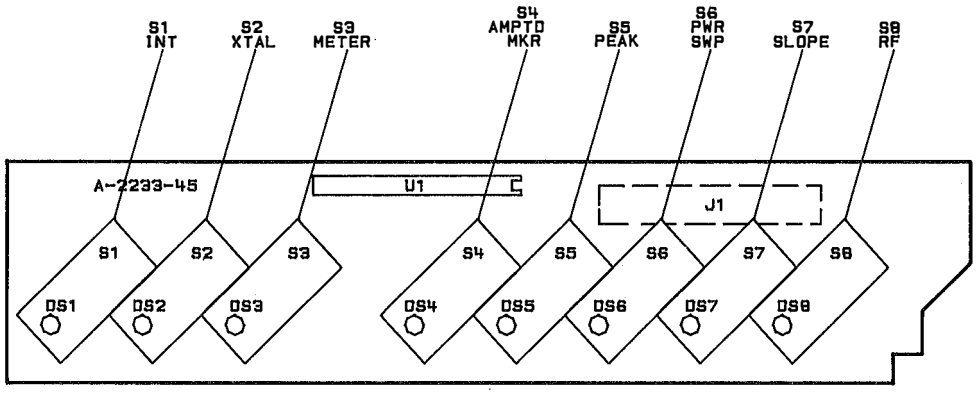
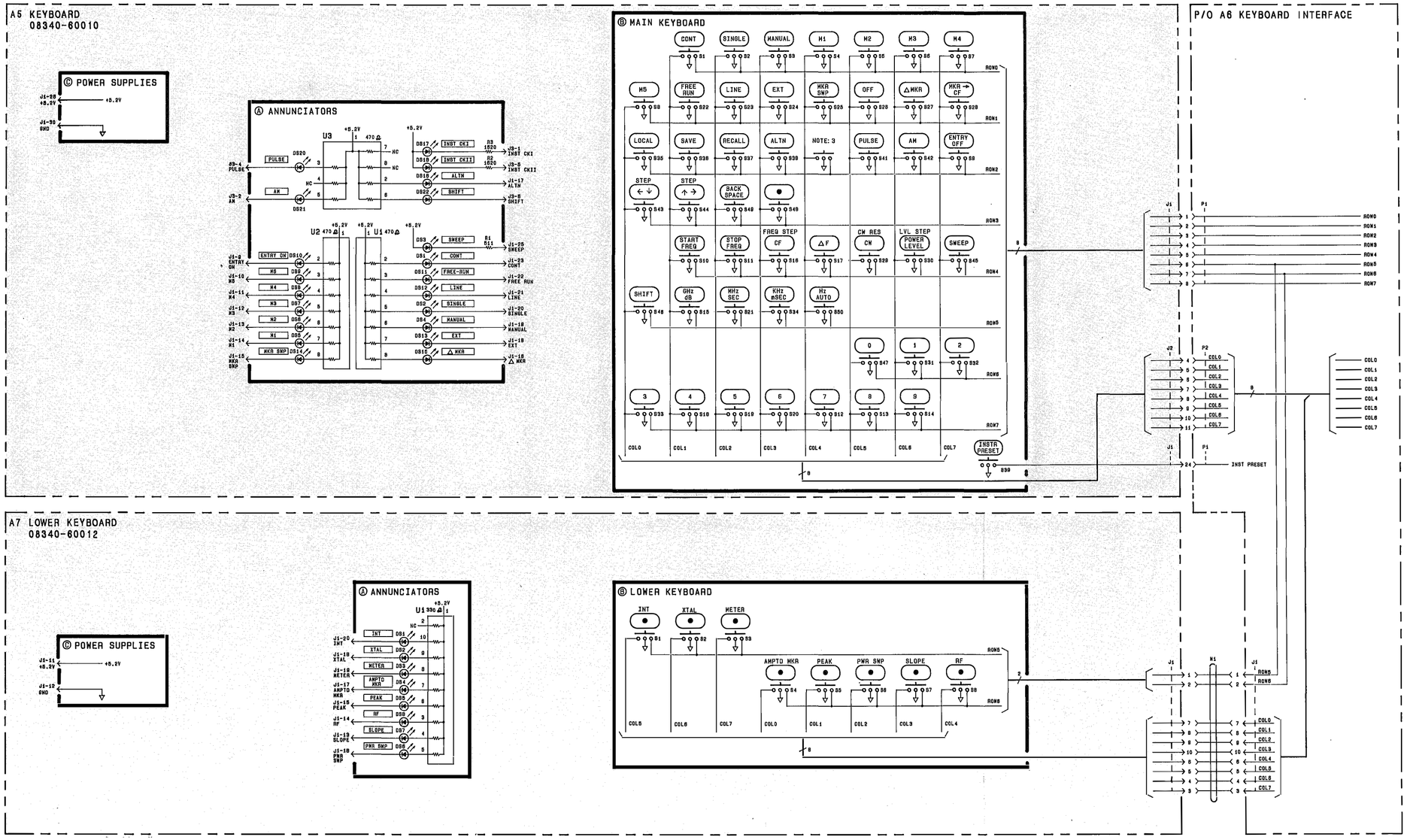


Figure 8H-16. A7 Lower Keyboard, Component Location Diagram



NOTES:

1. REFER TO THE SERVICE SEC. INTRO. SCHEMATIC DIAGRAM NOTES.
2. RESISTANCE VALUES ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. RESERVED FOR FUTURE USE.

Figure 8H-17. A5 Keyboard and A7 Lower Keyboard, Schematic Diagram

A6 KEYBOARD INTERFACE, CIRCUIT DESCRIPTION

KEYBOARD ENCODER/DATA BUFFER A

Two, eight-line to three-line priority encoders (U1 & U10) are used to encode the row and column information. When a key is pressed one row line and one column line is grounded by the key. The row and column is encoded and is presented in Low-True binary form at the outputs (U1 and U10 pins 9, 7, and 6). This information is immediately available at the inputs of U11, the inverting output buffer which converts the above six bits to High-True signals.

Table for Keyboard Encoder U10 & U1

Column or Row selected Low	Output of U10 or U1 PIN 9	7	6
0	1	1	1
1	0	1	1
2	1	0	1
3	0	0	1
4	1	1	0
5	0	1	0
6	1	0	0
7	0	0	0

If more than one key is pressed, the priority encoder only encodes the lowest column and row number.

The encoders can be disabled by a latched control bit. The main instrument processor outputs a HIGH on DB7 (A6U6 pin 3, Block **E**). The processor then outputs address 6, R1: (see U15 pin 10, Block **F**), which latches DB7 to U6 pin 2. This latched bit is sent to U1 pin 5, disabling U1. U1 pin 14 is then HIGH, disabling U10. This control line is used to lockout the keyboard.

If the decoders are not disabled, pressing any key generates a service request (LOW KEY DOWN to Block **C**, HI KEY DN SRQ to Block **I**, and LSRQ to the instrument processor). The processor then outputs address 6, R3: (Block **F**) and reads the encoded key information from U11 (Block **A**).

KEY DOWN TIMER C

The Low-True keydown signal fires a non-retriggerable one-shot (U20 pin 9) which is set for approximately 20 msec pulses. The Q-bar output (U20 pin 12) goes LOW for 20 msec and on its rising edge it clocks a D flip-flop (U19 pin 11) whose D input (U19 pin 12) is connected to the Low-True keydown signal. If a key is still down at this moment, the D flip-flop is reset indicating that a valid keydown has been detected.

When a valid keydown is detected, the Q-bar output (U19 pin 8) goes high and this is the HI KEY DOWN SRQ.

SRQ BUFFER I

The HI KEY DN SRQ signal is NORed (U3 pin 3) with the Hi-True RPG SRQ (U3 pin 2) signal to generate LSRQ (U3 pin 1) to the instrument processor.

The keydown SRQ signal is also present at U11 pin 2 which contains the encoded key information. This bit, when read by the processor during an SRQ service routine, indicates that it was a keydown that generated the service request. U11 inverts this signal so the processor sees a Low-True signal.

Once the instrument processor has read the encoded information, the processor generates a strobe (U15 pin 9 I/O 6,R2: in Block **F**) which sets the SRQ flip-flop (U19 pin 10) indicating that key information has been read by the processor and prepares the key down circuitry for the next keydown signal.

A keyboard lockout signal (U6 pin 2 in Block **E**) is inverted (U8 pin 5 to 6 Block **C**) and if it is LOW it resets the keydown one shot and prevents this one-shot from ever firing.

REPEAT FUNCTION CIRCUITS D

The repeat key function consists of two timing circuits. The first is a 500 msec (U9A) timer which is triggered by the Q output of the keydown flip-flop (U19 pin 9, Block **C**) when a valid keydown has been detected. After 500 msec the rising edge of the Q-bar output of this one-shot (U9 pin 4) clocks a D flip-flop (U4 pin 11). The D input (U4 pin 12) is connected to the Low-True KEY DOWN line from the encoders (U10 pin 14 in Block **A**). If a key is still down 500 msec after a valid key has been detected this flip-flop U4B will be reset activating the repeat function. The Q-bar output of this flip-flop (U4 pin 8) goes high which releases the reset of the second timer (U5 pin 4) and allows it to generate high going pulses at a 5 Hz rate.

The second timer (U5) is a 555 timer. The timing components (R1, R2, CR1, and C8) ensure that high going pulses with a very low duty cycle are generated. The high going output (U5 pin 3) of this timer goes through an inverter (U14 pin 3 to 1) and becomes LOW REPEAT to the RESET of the keydown SRQ flip-flop (U19 pin 13) which has the same effect as pressing the key again. The duration of the reset pulse to this flip-flop (U19B) must be shorter than the fastest time that the main processor can get around to servicing the keydown interrupt or else another keydown SRQ cycle will be immediately started.

KEY UP TIMER (DEBOUNCE) B

The key released timing function prevents key bounce from causing multiple keydown interrupts to the instrument processor. This is accomplished by disabling the keydown circuitry as soon as a valid keydown has been been detected and not re-enabling it until all keys have been up continuously for 50 msec.

As soon as a key is depressed, the REPEAT DISABLE signal (U14B pin 4) goes HIGH when the KEYBOARD LOCKOUT signal (U14B pin 6) is LOW. This REPEAT DISABLE signal is inverted twice (U8 pin 3-4,9-8) and appears at the input of a NOR gate (U14D pin 12). The other input to this NOR gate (U14D pin 11) is connected to the Q output of the keyup one-shot (U9B pin 5) which will go HIGH for 50 msec after the positive transition of the LOW KEY DOWN signal (U9B pin 10). The output of the above NOR gate (U14C pin 13) goes LOW and is inverted (U14C pin 9). The output of the inverter (U14C pin 10) causes the reset line of a D flip-flop (U4A pin 1) to go HIGH which enables this flip-flop. The keydown SRQ line is connected to the clock line (U4A pin 3) so as soon as a valid keydown has been detected, the flip-flop will be set. The Q-bar output (U4A pin 6) goes directly to the enable of the key down one-shot (U20 pin 10 in Block C) which prevents detecting any further key closures until this enable goes HIGH.

When the key is released the Low-True keydown line goes HIGH, firing one-shot U9B (pin 10) for 50 msec which continues to disable the keydown circuitry until it has timed out.

The 0.01 uF cap connected to the output of U8B pin 4 was added to prevent a possible race condition. The input to U14D pin 12 must remain HIGH until the one-shot output going to U14D pin 11 is HIGH and stable. Since the one-shot is fired by the same signal that goes into U14D pin 12, some means of delay had to be implemented. Both digital and analog delay is used to prevent a parametric change from causing a race condition.

At the end of 100 msec, the one-shot output (U9B pin 5) goes LOW which causes the keydown disable flip-flop to be cleared (U4A pin 1) which in turn re-enables the keydown flip-flop (U20B pin 10 in Block C).

RPG COUNTERS DATA BUFFERS G

The rotary pulse generator (RPG) RP1 generates two pulses which are 90 degrees out of phase with each other when the knob is rotated.

Two four bit up/down counters (U13 and U18) count up or down depending on the direction in which the RPG is turned. The two signals from the RPG (which are 90 degrees out of phase) are connected to the up/down input (U13 and U18 pin 1) and to the

clock input (U13 and U18 pin 2). If the clock line goes HIGH while the up/down line is still LOW, the counters count down. On the other hand if the RPG is turned in the opposite direction, the up/down line will be HIGH when the clock line goes HIGH and the counters will count up. When the counter counts down below 0, the output is set to all ones and counted down from there.

The outputs of the up/down counters (U13 and U18 pins 13 through 16) are always present at the inputs to the noninverting bus driver from which the instrument processor reads present count.

The up/down counters are cleared by the processor (U13 and U18 pin 8) after the information is read which readies them for the next count period.

A 0.01 uF capacitor is connected to the clock line and the up/down line (C13 and C14) from the RPG (U8 pins 11 and 13) to prevent static discharges from clocking the up/down counters.

RPG COUNT WINDOW TIMER H

The clock line that goes to the up/down counters from the RPG is connected to the clock of a 70 msec one-shot (U20A pin 2). The very first pulse on the RPG clock line fires the one-shot. At the end of 70 msec, the one-shot output (U20A pin 4) clocks a D flip-flop (U19A pin 3). If the RPG is enabled, the D input to this flip-flop (U19A pin 2) will be LOW and the Q-bar output (U19A pin 6) will go HIGH causing the LSRQ (Block **I**) line to go LOW, indicating a service request to the processor. The Q-bar output (U19A pin 6) also goes to the input of the inverting bus buffer (U11 pin 17 in Block **A**). The output of U11 is read by the processor during the service request routine. A LOW on this line indicates the RPG which needs service.

The RPG SRQ line also goes to the disable count input of the up/down counters (U13 and U18 pin 7 Block **G**) which disables any further counting until the processor has serviced the RPG service request.

After the instrument processor has read the information from the up/down counters, a reset strobe is generated (U15 pin 9, Block **F**) by the processor which sets the RPG SRQ flip-flop and clears the up/down counters and prepares the entire circuit for another cycle.

ANNUNCIATOR LATCHES E

Four 8-bit D-latches (U6, U7, U16, and U17) store LED & control information. 29 bits control all of the various LEDs on the front panel. One bit is an instrument preset lockout (U16 pin 2) which is ANDed with the input from the hardware instrument preset signal. One bit is the lockout for the rest of the keyboard (U6

pin 2) which prevents any keyboard entries. The last bit (U17 pin 9) is unused.

The same bit that turns on the enabled LED also enables the RPG (U19 pin 2 Block **H**). U19 pin 2 is the D input.

The green SWEEP LED is driven by an inverter which is controlled by a NAND gate. This NAND gate forces the LED to be ON when LIPS (Instrument Preset signal) is LOW.

ADDRESS DECODER F

U15 is used to decode four strobes from the five Address lines and the I/O strobe (SIOB). LEN 4 and LEN 4 (U15 pin 11 and 10) are used to clock the LED and control input D-latches (U6, U7, U16, and U17 Block **E**). LEN 6 (U15 pin 9) resets the Key down and RPG service request circuitry. LEN 7 (U15 pin 7) is a read strobe and enables the coded key information, the RPG count information, and the two bits which indicate which circuit requested service onto the bus to be read by the processor.

POWER SWITCH AND STANDBY LED

During STANDBY operation, the POWER switch grounds the LSBY line which activates the fan relay and signals the power supplies to turn off.

The STANDBY LED is connected to the +22 volt supply through a current limiting resistor. The POWER switch grounds the cathode of this LED during standby thus turning on the LED.

A6 KEYBOARD INTERFACE TROUBLESHOOTING

REQUIRED EQUIPMENT

* VOM
* Oscilloscope (100 MHz)
* 5005B Signature Analyzer (If DSA Troubleshooting is used)
* Logic Probe

PREPARATION

1. Refer to Figure 8H-4 and remove the Front Panel Assembly from the instrument.
2. Disconnect the display from the keyboard and reattach the display to the frame.
3. Lay the keyboard down in front of the instrument to allow access to the Keyboard Interface.

SYMPTOMATIC TROUBLESHOOTING

One Or More LED'S Do Not Light When [INSTR PRESET] Is Pressed

1. Troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**) and the Annunciators (A5 and A7 Block **A**).

None Of The Annunciators Light When [INSTR PRESET] Is Pressed

1. Troubleshoot the INSTR PRESET BUFFER (A6 Block **J**).
2. Troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**)

All Of The Annunciators Except SWP Remain On After Power Up or After [INSTR PRESET]

1.Troubleshoot the ADDRESS DECODER (A6 Block **F**).

2. Troubleshoot the INSTR PRESET BUFFER (A6 Block **J**).

Check LED I Or II Remain On After [INSTR PRESET]

1. The instrument processor self test has failed. Refer to the A60 Processor troubleshooting.

Pressing A Key Gives No Response (Display Does Not Change And The Instrument State Does Not Change)

1. Probe KEYBOARD LOCKOUT at A6U6 pin 2 (Block **E**). This signal

should be LOW. If KEYBOARD LOCKOUT (U6 pin 2) is HIGH, troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**).

2. Probe LOW KEY DOWN at U10 pin 14. Press any key and this signal should go LOW. If LOW KEY DOWN does not go LOW, troubleshoot the KEYBOARD ENCODER/DATA BUFFER (A6 Block **A**).

3. Probe HI KEY DN SRQ (A6 TP 3) with an oscilloscope. Set the oscilloscope to 5 ms/Div. This signal should normally be LOW and, when you press a key, go HIGH for a period of time that is equal to the response time of the instrument processor to a SRQ. This will vary between 100 us and 25 ms. If HI KEY DN SRQ is correct, troubleshoot the SRQ BUFFER (A6 Block **I**). If HI KEY DN SRQ is not correct, troubleshoot the KEY DOWN TIMER (A6 Block **C**).

When A Key Is Held Down, The Key Is Not AutomaticallY Repeated

1. Probe REPEAT RESET (U4A pin 5 Block **B**). This signal should go HIGH and stay HIGH as long as a key is depressed. If REPEAT RESET functions correctly, troubleshoot REPEAT FUNCTIONS CIRCUIT (A6 Block **D**). If REPEAT RESET does not function correctly then troubleshoot the KEY UP TIMER (DEBOUNCE) (A6 Block **B**).

Pressing A Key Sometimes Produces Several Of The Same Characters In The Display

1. Probe LOW KEY DISABLE (A6 U20B pin 10, Block **C**). This signal should go LOW and remain LOW until after the key is released. If LOW KEY DISABLE appears to be functioning correctly, troubleshoot the KEY DOWN TIMER (A6 Block **C**). If LOW KEY DISABLE is HIGH all the time, troubleshoot the KEY UP TIMER (A6 Block **B**).

Sometimes Keystrokes Are Missed By The Instrument

1. Troubleshoot the KEY DOWN TIMER (A6 Block **C**).

The 8340A Only Responds To Keystrokes And/Or The RPG When It Is In A Swept Mode And Ignores Them When Not In A Swept Mode

1. Troubleshoot the SRQ BUFFER (A6 Block **I**).

Turning The RPG When There Is An Active Function Produces No Response

1. Press a function key and verify that the ENTRY ON LED lights. If this LED does not light, troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**).

2. If the ENTRY ON LED is lit, probe CLK (A6TP1) with an

oscilloscope. Set the oscilloscope to 5 ms/Div. You should see LOW going pulses as you rotate the RPG and the pulse width should vary with the speed of rotation. If CLK is not correct, troubleshoot the RPG and RPG COUNTERS/DATA BUFFERS (A6 Block **G**).

3. Probe HI RPG SRQ (A6TP8). You should find HIGH going pulses which vary in width depending on the response time of the instrument processor to a SRQ. These pulses should be between 100 us and 25 ms. If HI RPG SRQ is correct, troubleshoot the SRQ BUFFER (A6 Block **I**) and the RPG COUNTERS/DATA BUFFERS (A6 Block **G**). If HI RPG SRQ is not correct, troubleshoot the RPG COUNT WINDOW TIMER (A6 Block **H**).

Turning The RPG Produces A Change Only In One Direction

1. Troubleshoot the RPG and RPG COUNTERS/DATA BUFFER (A6 Block **G**).

Turning The RPG Causes Either Very Small Or Very Large Changes In The Active Function In The ENTRY DISPLAY

1. Troubleshoot the RPG COUNT WINDOW TIMER (A6 Block **H**).

The Instrument Will Not Do An Instrument Preset When The [INSTR PRESET] Key Is Pressed

1. Troubleshoot the INSTR PRESET BUFFER (A6 Block **J**).

A6 KEYBOARD INTERFACE BLOCK-BY-BLOCK TROUBLESHOOTING

KEYBOARD ENCODER/DATA BUFFER (A6 BLOCK A)

U1, U10, And U11 Troubleshooting

1. Probe KEYBOARD LOCKOUT (U1 pin 5). This signal should be LOW unless the 8340A is in REMOTE mode. If KEYBOARD LOCKOUT is HIGH, troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**).

2. Probe LOW KEY DOWN (U10 pin 14). This signal should be HIGH and go LOW when any key is pressed. If this signal is correct, proceed to step 6.

3. If LOW KEY DOWN stays HIGH even when a key is pressed, check the enable into U10 (U10 pin 5). This signal should also be HIGH and go LOW when any key is pressed. If the enable signal to U10 pin 5 in correct, proceed to step 5.

NOTE

If COL 1 or ROW 3 is found to be functioning incorrectly in steps 4 or 5, L STEPUP may be the cause. Perform the troubleshooting for L STEPUP prior to troubleshooting the Keyboard.

4. If the signal to U10 pin 5 functions incorrectly, either U1 is bad or the appropriate input to U1 is not being pulled LOW by the key row. Probe the appropriate key row input to U1. This signal should be HIGH and go LOW each time the associated key is pressed. If the key row functions correctly, replace U1. If the key row does not function correctly, troubleshoot the Keyboard (A5 and A7 Block **B**).

5. If U10 pin 5 functions correctly, either U10 is bad or the appropriate input to U10 is not being pulled LOW by the key column. Probe the appropriate key column input to U10. This signal should be HIGH and go LOW each time the associated key is pressed. If the key column functions correctly, replace U10. If the key column does not function correctly, troubleshoot the Keyboard (A5 and A7 Block **B**).

6. If all the rest of the circuitry on the A6 board is functioning correctly yet a key stroke or RPG number is not communicated to the instrument, it is possible that the buffer (U11) is not functioning correctly. Probe LEN 7 at U11 pin 1 or 19 with an oscilloscope. Set the oscilloscope to 0.1 us/Div. You should find 300 to 400 ns wide, LOW going pulses each time you press a key or repetitive pulses if you hold a key down. If the pulses are not present, troubleshoot the ADDRESS DECODER (Block **F**).

7. Use LEN 7 to trigger the oscilloscope and probe the outputs of

U11 to see if the output is in the correct state during the output enable pulse. When you probe pin 3, you should find it LOW if a key was pressed. When you probe pin 18, you should find it LOW if the RPG was rotated. The remaining outputs (pins 5, 7, 9, 12, 14, and 16) should be HIGH or LOW depending on the key code of the key being depressed (see the circuit description and schematic).

8. If one or more of the outputs are not correct, probe the corresponding input. Since U11 is an inverting buffer you should find the inverted version of the signals described in step 7. If the levels are correct at the input, replace U11. If the signals are not correct, troubleshoot the device from which the signal came.

LSTEPUP Troubleshooting

1. Probe LSTEPUP at the cathode of CR2 or CR3. LSTEPUP should be HIGH and only go LOW when pin 22 on the rear panel 8410 Interface connector is grounded. If this signal is HIGH and stays HIGH when the input is shorted to ground, check the front panel ribbon cable and rear panel cable assy for an open wire. If LSTEPUP is LOW all the time, proceed to step 3.

2. With the diodes installed, check the voltage at the anode of each diode both with LSTEPUP open and with LSTEPUP shorted to ground. The anodes should be at approximately 5V when LSTEPUP is open and at approximately 0.4V when LSTEPUP is shorted to ground. If the voltage at either anode is 0.2V or less when LSTEPUP is grounded, that diode is likely shorted and should be replaced. If the voltage at either anode remains at 5 V when LSTEPUP is grounded, that diode is open and should be replaced.

3. If LSTEPUP stays LOW all the time, lift the cathodes of the two diodes (CR2 and CR3) out of the PC Board and check the signal LSTEPUP with an ohmmeter to determine if a short to ground exists. If LSTEPUP is not shorted to ground, check CR2 and CR3 for being open as described in step 2.

4. Check COL 1 (U10 pin 3) and ROW 3 (U1 pin 1) for a HIGH when no key is pressed. If either signal is LOW, determine whether the COL or ROW line is shorted or the encoder (U1 or U10) input is shorted.

KEY UP TIMER (A6 BLOCK B)

1. Probe KEYBOARD LOCKOUT. This signal should be LOW unless the 8340A is in REMOTE mode. If this signal is not correct, troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**).

2. Probe LOW KEY DOWN with an oscilloscope. Set the oscilloscope to 100 ms/Div. This signal should go LOW each time a key is

pressed and remain LOW until the key is released. If this signal is not correct, troubleshoot the KEYBOARD ENCODER/DATA BUFFER (A6 Block **A**).

3. Connect the trigger of the oscilloscope to LOW KEY DOWN (A6TP6) and trigger on the rising edge. Set the oscilloscope to 10 ms/Div and probe the output of the key up timer (A6TP7). You should find a HIGH going pulse 45 to 55 ms wide each time a key is RELEASED. If this pulse is not present, replace U9B. If the duration of this pulse is not correct, check or replace R7 or C24.

4. Probe LOW KEY DISABLE (A6TP13). This signal should go LOW when HI KEY DN SRQ goes HIGH and should remain LOW for 45 to 55 ms after LOW KEY DOWN goes HIGH. If LOW KEY DISABLE is correct, proceed to step 10.

5. Probe U4A pin 1. This signal should go HIGH when a key is pressed and should remain HIGH for 45 to 55 ms after the key is released. If the signal at U4A pin 1 is not correct, proceed to step 8.

6. Probe HI KEY DN SRQ (A6TP3) with the oscilloscope. Set the oscilloscope to trigger on the LOW going edge of LOW KEY DOWN (A6TP6). You should find a 100 us to 20 ms wide, HIGH going pulse that occurs 15 to 25 ms after the LOW going edge of LOW KEY DOWN. If HI KEY DN SRQ is not correct, troubleshoot the KEY DOWN TIMER (A6 Block **C**).

7. If HI KEY DN SRQ is correct, check U4A pins 2 and 4 to make sure they are pulled HIGH by R11. If these inputs are also correct, replace U4A.

8. Probe A6TP4 (U14D pin 12) with the oscilloscope. Set the oscilloscope to 100 ns/Div and trigger on the HIGH going edge of LOW KEY DOWN. You should find that this signal remains HIGH for a minimum of 100 ns after a key is released. If this signal is LOW all the time, either U8 or U14 is bad.

9. If the signal at A6TP4 is HIGH all the time, probe REPEAT DISABLE (U14B pin 4). REPEAT DISABLE should be an inverted version of LOW KEY DOWN. If REPEAT DISABLE is not correct, replace U14. If REPEAT DISABLE is correct, either U8 is bad or C23 is shorted.

10. If LOW KEY DISABLE is correct, probe REPEAT RESET (U4A pin 5). This signal should go HIGH when HI KEY DN SRQ goes HIGH and remain HIGH for 45 to 55 ms after LOW KEY DOWN goes HIGH.

11. If REPEAT RESET is not correct, either the output of U4A is bad or the input to U9A pin 3 is bad. Lift U4A pin 5, recheck for the correct signal at U4A pin 5, and replace the

appropriate part.

KEY DOWN TIMER (A6 BLOCK C)

1. Probe KEYBOARD LOCKOUT (U8C pin 5). This signal should be LOW unless the 8340A is in REMOTE mode. If this signal is not correct, troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**).

2. Probe the output of U8C pin 6. This signal should be an inverted version of KEYBOARD LOCKOUT. If this signal is not correct, replace U8.

3. Probe LOW KEY DISABLE (U20 pin 10). This signal should go LOW when HI KEY DN SRQ goes HIGH and should remain LOW for 45 to 55 ms after LOW KEY DOWN goes HIGH. If this signal is not correct, troubleshoot the KEY UP TIMER (A6 Block **B**).

4. Probe LOW KEY DOWN with an oscilloscope. Set the oscilloscope to 100 ms/Div. This signal should go LOW each time a key is pressed and remain LOW until the key is released. If this signal is not correct, troubleshoot the KEYBOARD ENCODER/DATA BUFFER (A6 Block **A**).

5. Connect the trigger of the oscilloscope to LOW KEY DOWN (A6 TP6) and trigger on the falling edge. Set the oscilloscope to 10 ms/Div and probe the output of the Key Down Timer (A6TP14). You should find a 15 to 25 ms wide, LOW going pulse each time a key is pressed. If this pulse is not present, replace U20B. If the duration of this pulse is not correct, check or replace R5 or C17.

6. Probe HI KEY DN SRQ with the oscilloscope. Each time a key is pressed, you should find a 100 us to 20 ms wide, HIGH going pulse which starts at the same time as the output of the Key Down Timer (TP14) goes HIGH. If HI KEY DN SRQ is correct, proceed to step 10.

7. Probe LOW REPEAT (A6TP12). This signal should remain HIGH unless a key is held down for longer than approximately on half second. If LOW REPEAT is not correct, troubleshoot the REPEAT FUNCTION CIRCUITS (A6 Block **D**).

8. Probe LEN 6 (U19B pin 10) with an oscilloscope. Set the oscilloscope to 0.2 us/Div. You should find a LOW going, 300 to 400 ns wide pulse each time a key is pressed. (This signal may be difficult to find unless a storage scope is used. Refer to ADDRESS DECODER Troubleshooting (A6 Block **F**) for further information.) If LEN 6 is not correct, troubleshoot the ADDRESS DECODER (A6 Block **F**).

9. If LEN 6 is correct, either the output of U19B (pin 8) is bad or one of the three destinations of HI KEY DN SRQ is bad.

Determine which part is bad (U11 Block **A**, U4 Block **B**, U19 Block **C**, or U3 Block **I**) and replace the defective part.

10. If HI KEY DN SRQ is correct, probe LOW DEBOUNCED KEY DOWN (U19B pin 9) with the oscilloscope. You should find LOW going, 15 to 25 ms wide pulses starting when the signal at TP14 goes HIGH.

11. If LOW DEBOUNCED KEY DOWN is not correct, either the output of U19B is bad or U9A pin 1 (Block **D**) input is bad. Lift U19 pin 9, recheck for the correct signal at U19 pin 9, and replace the appropriate part.

REPEAT FUNCTION CIRCUITS (A6 BLOCK D)

1. Probe REPEAT RESET (U9A pin 3) with the oscilloscope. Set the oscilloscope 20 ms/Div and trigger off the LOW going edge of LOW KEY DOWN (A6TP6). REPEAT RESET should go HIGH 15 to 25 ms after LOW KEY DOWN goes LOW and should remain HIGH for 45 to 55 ms after LOW KEY DOWN (TP6) goes HIGH. If this is not correct, troubleshoot the Key Up Timer (A6 Block **C**).

2. Probe LOW DEBOUNCED KEY DOWN (U9 pin 1) with the oscilloscope (same settings as step 1). This signal should go LOW 15 to 25 ms after LOW KEY DOWN goes LOW and remain LOW 100 us to 20 ms (depends on how fast the main processor services the HI KEY DN SRQ). If this signal is not correct, troubleshoot the Key Down Timer (A6 Block **C**).

3. Probe REPEAT DISABLE (U4 pin 10) with the oscilloscope (same settings as step 1). This signal should go HIGH when any key is pressed and go LOW as soon as the key is released. If this signal is not correct, troubleshoot the Key Up Timer (A6 Block **B**).

4. Probe U9A pin 4 (A6TP9) with the oscilloscope. Set the oscilloscope to 100 ms/Div and trigger on the HIGH going edge of HI KEY DN SRQ (A6TP3). Press any key and hold it down. This signal should go LOW for approximately 400 ms and then go HIGH for approximately 100 ms. If this signal is not present, replace U9. If the duration of this signal is not correct, check or replace R3 or C7.

5. Probe TP5 (U4 pin 8) with the oscilloscope (same settings as step 4). Press any key and hold it down. TP5 should be LOW and remain LOW for approximately 400 ms. It should then go HIGH and remain HIGH until the key is released. If the signal at TP5 is correct, proceed to step 7.

6. Lift U4B pin 8 and check for the signal described in step 5 right at the pin. If this signal is now correct, check for shorts along the trace or replace U5 if there are no shorts.

If the signal is not correct, replace U4.

7. Probe U5 pin 3 with the oscilloscope. Set the oscilloscope to 50 ms/Div and select rising edge triggering. When you press and hold a key you should find a HIGH going pulse every 100 ms. If this signal appears correct, proceed to step 10.

8. If the signal at U5 pin 3 goes HIGH (when U5 Pin 4 goes HIGH) and remains HIGH until the key is released, C8 is shorted. If the signal is a square wave, CR1 is most likely open.

9. If U5 pin 3 stays either HIGH or LOW, lift U5 pin 3 and recheck the signal right at the pin. If the signal is now correct, check for shorts or replace U14 if no shorts exist. If the signal is still bad, replace U5.

10. Adjust the oscilloscope to 20 us/Div. Verify that these HIGH going pulses are approximately 20 us wide. If these 20 us wide, HIGH going pulses are spaced very close together (< 100 ms), it is very likely that CR1 is shorted.

11. If the signal at U5 pin 3 is correct, probe LOW REPEAT (A6 TP12) with the oscilloscope. Set the oscilloscope to 50 ms/Div and triggering on the LOW going edge of this signal. You should find the inverted version of the signal at U5 pin 3.

12. If LOW REPEAT is not correct, lift U14A pin 1 and recheck the signal right at the pin. If the signal is now correct, check for shorts or replace U19 if no shorts exist. If the signal is still bad, replace U14.

ANNUNCIATOR LATCHES (A6 BLOCK E)

1. Probe ANNUNCIATOR RESET at U6 pin 1. This signal should be HIGH all the time and should go LOW when **[INSTR PRESET]** is pressed. If ANNUNCIATOR RESET is not correct, troubleshoot the INSTR PRESET BUFFER (A6 Block **J**).

2. Probe LEN 5 at U6 pin 11 with the oscilloscope. Set the oscilloscope to 200 ns/Div and trigger on the LOW going edge of this pulse. You should find a LOW going, 300 to 400 ns wide pulse each time you press a key which has a LED associated with it. If this signal is not present, troubleshoot the ADDRESS DECODER (A6 Block **F**).

3. Probe LEN 4 at U16 pin 11 with the oscilloscope. Set the oscilloscope to 200 ns/Div and trigger on the LOW going edge of this pulse. You should find a LOW going, 300 to 400 ns wide pulse each time you press a key which has a LED associated with it. If this signal is not present, troubleshoot the ADDRESS DECODER (A6 Block **F**).

One Or More Of The Front Panel LEDs Never Light

1. Perform steps 1, 2, and 3 at the beginning of the ANNUNCIATOR LATCHES troubleshooting.

2. Check the voltage at the appropriate output of the ANNUNCIATOR LATCHES (U6, U7, U16, or U17). When **[INSTR PRESET]** is pressed the voltage at all of these outputs should be LOW (approximately 0.4V). If the appropriate output is LOW yet the LED is OFF, replace the LED.

3. If the output checked in step 2 does not go LOW, lift the output pin and recheck the voltage right at the pin with **[INSTR PRESET]** pressed. If the signal is now correct, check for shorts either on the A6 board or on the A5 or A7 keyboards. If the signal is still bad, replace the appropriate latch.

One Or More Outputs From The Annunciator Latches Is Not Correct

1. Perform steps 1, 2, and 3 at the beginning of the ANNUNCIATOR LATCHES troubleshooting.

2. If one or more of the outputs from the ANNUNCIATOR LATCHES (U6, U7, U16, and U17) is not correct, enable the INSTRUMENT DSA by connecting the LSTS test point (TP13 on the A60 Processor board) to ground.

3. Verify that suspected latch output is not working. Set the oscilloscope to 100 us/Div and probe the output. If the output is working, you should find TTL activity (< 0.4V for LOW and > 3.5V for HIGH).

4. Probe the appropriate data bus input for this section of the latch with the oscilloscope. Set the oscilloscope to 10 us/Div and triggering on the LOW going edge of this signal. You should find a series of low going pulses, 2 to 4 us wide. The LOW level should be very near 0V an the HIGH level should be very near +5V. If the signal is correct, proceed to step 6.

5. Check this same data bus line at the Motherboard end of the front panel ribbon cable. If the signal appears at the Motherboard correctly, repair or replace the ribbon cable. If no signal appears at the Motherboard, refer to the A60 Processor troubleshooting.

6. Lift the appropriate output pin of the latch and check the signal right at the pin as described in step 4. If the signal is still not correct, replace the latch.

7. If the signal is correct with the pin lifted, check along the signal trace for shorts. In the case of the control signals, troubleshoot the following:

RPG COUNT WINDOW TIMER (A6 Block **H**) if the ENTRY ON signal (U6 pin 19) is bad.

KEY UP TIMER (A6 Block **B**), KEYBOARD ENCODER/DATA BUFFER (A6 Block **A**) or KEY DOWN TIMER (A6 Block **C**) if the KEYBOARD LOCKOUT signal (U6 pin 2) is bad.

INSTR PRESET BUFFER (A6 Block **J**) if INSTR PRESET LOCKOUT signal (Ul6 pin 2) is bad.

Front Panel SWEEP LED Not Operating Correctly

1. With the 8340A sweeping, probe LSPLD (U2D pin 13) with the oscilloscope. Set the oscilloscope to approximately the same ms/Div as the sweep time of the 8340A. You should find both HIGH and LOW TTL levels with the LOW level corresponding to the times when the sweep LED should be ON. If LSPLD is correct, proceed to step 4.

2. Measure LSPLD at the Motherboard end of the ribbon cable. If LSPLD is present at the Motherboard, the ribbon cable is likely open and should be replaced.

3. If no signal appears at the Motherboard then disconnect the 50 pin ribbon Cable from the A6 Keyboard Interface and recheck for this signal. If there still is no signal at the Motherboard, troubleshoot this signal on the A58 Sweep Generator. If the signal is present, check for shorts along this signal path on the A6 board and replace U2 if no shorts are found.

4. Probe U2D pin 11. You should find an inverted version of LSPLD. If the signal does not appear at pin 11, check for shorts and then replace U2 if there are no shorts.

5. Check the signal at U2 pin 8. It should be the same as LSPLD. If the signal at U2 pin 8 is correct yet the SWEEP LED is not flashing, replace the green SWEEP LED. If the signal at U2 pin 8 is not correct, check for shorts along the signal path of the A5 Keyboard as well as the A6 board and then replace U2 if no shorts are found.

ADDRESS DECODER (A6 BLOCK F)

1. Measure the voltage between the ground pin (U15 pin 8) and chassis ground. If the measured voltage is not 0V, repair or replace the front panel ribbon cable.

2. Place the 8340A into the DSA mode by grounding the LSTS test point on the A60 Processor board. Probe A0 thru A4 and SIOB (U15 pins 1 through 6) with the oscilloscope. Set the oscilloscope to 2 us/Div and triggering on the LOW going edge. You should find bus activity (both HIGH and LOW levels) on every line. If the signals are present, proceed to step 5.

3. Measure the signal(s) that is not present at the Motherboard end of the ribbon cable. If the signal is present at the Motherboard, the ribbon cable is most likely open and should be replaced.

4. If no signal appears at the Motherboard, disconnect the 50 pin ribbon cable from the A6 Keyboard Interface and recheck for the signal. If there still is no signal at the Motherboard,

troubleshoot the signal on the A60 Processor board. If the signal is present, check for shorts along the signal path on the A6 board and replace U15 if no shorts are found.

5. If all of the inputs to U15 are correct, probe LEN 4 through LEN7 (U15 pins 7, 9, 10, and 11) with the oscilloscope. Set the oscilloscope to 200 ns/Div. You should find 200 to 400 ns wide, LOW going pulses. If LEN 4 through LEN 7 are correct, the ADDRESS DECODER is operating properly.

6. If any of these signals is not correct, lift the appropriate pin of U15 and check the signal right at the pin. If the signal is now correct, troubleshoot the blocks which are connected to the signal. If the signal is still not correct, replace U15.

RPG COUNTERS/DATA BUFFERS (A6 BLOCK G)

1. Probe CLK (A6TP1) with the oscilloscope. Set the oscilloscope to 10 ms/Div. You should find a repetitive TTL signal when you rotate the RPG. If the signal is present, proceed to step 3.

2. Remove the 902 (white/black/red) wire from the RPG connector and check CLK right at the wire. If the signal is not present, replace the RPG. If the signal is present, check C25 for being shorted. If C25 is not shorted, replace U8.

3. Probe the output of the U8E (pin 10). The inverted version of CLK should be present. If the signal is correct, proceed to step 5.

4. If the signal is not present at U8E pin 10 output, either U8 is bad or one of the inputs driven by this signal is preventing the signal from changing. Lift U8 pin 10 and check the signal right at this pin. If the signal still is not correct, replace U8. If the signal is correct, inspect for shorts along this signal trace. If no shorts exist, determine which of the destinations is the problem.

5. Probe UP/DOWN (A6TP2) with the oscilloscope. Set the oscilloscope to 10 ms/div. You should find a repetitive TTL signal when the RPG is rotated. If the signal is present, proceed to step 7.

6. Remove the 901 (white/black/brown) wire from the RPG connector and check the signal right at the wire. If the signal still is not present, replace the RPG. If the signal is present, check if C26 is shorted. Replace U8 if C26 is not shorted.

7. Probe the output of U8E (pin 12). The inverted version of UP/DOWN should be present. If the signal is correct, proceed to step 9.

8. If the signal is not present at U8E pin 12, either U8 is bad or one of the inputs driven by this signal is preventing the signal from changing. Lift U8 pin 12 and check the signal right at this pin. If the signal still is not correct, replace U8. If the signal is correct, inspect for shorts along this signal trace. If no shorts exist, determine which of the destinations is the problem.

9. Probe LEN6 at U13 or U18 pin 8 and LEN7 at U12 pin 1 or 19 with the oscilloscope. Set the oscilloscope to 200 ns/Div and trigger on the LOW going edge. You should find 200 to 400 ns wide, LOW going pulses each time the RPG is rotated. If these pulses are not present, troubleshoot the ADDRESS DECODER (A6 Block **F**).

10. Probe HI RPG SRQ at U13 or U18 pin 7 with the oscilloscope. Set the oscilloscope to 20 ms/division. HI RPG SRQ should be LOW and goes HIGH for 100 us to 20 ms each time the RPG is rotated. If this signal is not correct, troubleshoot the RPG COUNT WINDOW TIMER (A6 Block **H**).

11. Probe the outputs of U13 and U18 (pins 13 through 16 and pin 19) with the oscilloscope. Set the oscilloscope to 20 ms/Div and trigger on the HIGH going edge. Each time you rotate the RPG (very slowly counter clockwise) you should find a series of pulses on these pins. If pulses do not appear at an output, either U13 or U18 is bad or the input to the bus buffer (U12) is bad.

12. Probe each output of U12 (pins 3, 5, 7, 9, 12, 14, 16, and 18) with the oscilloscope. Set the oscilloscope to 200 ns/Div and trigger on the LOW going edge of LEN7 (U12 pin 1 or 19). Rotate the RPG slowly in both directions and verify that both HIGH and LOW levels are present at each output of U12 during the first 200 to 400 ns after the trigger. If one or more of the outputs does not exhibit both HIGH an LOW states during this time window yet the corresponding input to U12 does, U12 is bad.

13. If all of these outputs are correct but you still suspect that the main processor is not getting the data, verify that these signals are getting through the front panel ribbon cable by probing right at the Motherboard with the oscilloscope. Set the oscilloscope the same as in step 12. Note that if one of these data lines is open, several of the LEDs on the front panel will also be incorrect.

RPG COUNT WINDOW TIMER (A6 BLOCK H)

1. Probe LEN6 at U13 or U18 pin 8 (Block **G**) and LEN7 at U12 pin 1 or 19 (Block **G**) with the oscilloscope. Set the oscilloscope to 200 ns/Div and trigger on the LOW going edge. You should find

200 to 400 ns wide, LOW going pulses each time the RPG is rotated. If these pulses are not present, troubleshoot the ADDRESS DECODER (A6 Block **F**).

2. Probe ENTRY ON at U19A pin 2. This signal should be LOW if an active function is displayed in the entry display. Press **[START FREQ]** and this signal should go LOW. If this signal does not go LOW, troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**).

3. Probe CLK (U20 pin 2) with the oscilloscope. Set the oscilloscope to 10 ms/Div. You should find a repetitive TTL signal when the RPG is rotated. If CLK is not correct, troubleshoot the RPG COUNTERS/DATA BUFFER (A6 Block **G**).

4. Connect the trigger of the oscilloscope to CLK (A6TP1) and trigger on the falling edge. Probe the output of the RPG COUNT WINDOW TIMER (A6TP15) with the oscilloscope. You should find a LOW going pulse 65 to 75 ms wide each time the RPG is rotated. If this pulse is not present, replace U20. If the duration of this pulse is not correct, check or replace R6 or C22.

5. Probe HI RPG SRQ with the oscilloscope. Each time the RPG is rotated you should find a 100 us to 20 ms wide, HIGH going pulse which goes HIGH at the same time as the output of the RPG COUNT WINDOW TIMER (TP15) goes HIGH.

6. If HI RPG SRQ is not correct, lift U19 pin 6 and recheck the signal. Press **[INSTR PRESET]** and the signal should go LOW. Rotate the RPG and verify that HI RPG SRQ pulses HIGH (if the 8340A is sweeping) or goes HIGH and stays HIGH (if the 8340A is not sweeping). If the signal is correct at U19 pin 6, either there is a short along this trace or one of the inputs connected to HI RPG SRQ is bad and is preventing it from changing levels. If the signal at U19 pin 6 is not correct, replace U19.

SRQ BUFFER (A6 BLOCK I)

1. Probe LSRQ (U3A pin 1) with the oscilloscope. Set the oscilloscope 100 us/Div and trigger on the LOW going edge. Press **[CW]** on the 8340A and rotate the RPG. You should find a 100 us wide, LOW going pulse each time the RPG is rotated. If this signal is correct, proceed to step 4.

2. Probe HI RPG SRQ (TP8) with the oscilloscope. Set the oscilloscope to trigger on the HIGH going edge. Each time the RPG is rotated, you should find a 100 us wide, HIGH going pulse. If this signal is correct, replace U3.

3. If HI RPG SRQ is not correct, lift U3A pin 2 and recheck HI RPG SRQ at TP8. Rotate the RPG and verify that this signal goes HIGH and stays HIGH. Press ENTRY OFF and verify that HI RPG SRQ

returns LOW when you rotate the RPG. If HI RPG SRQ is now correct, replace U3. If the signal is still bad at TP8, troubleshoot the RPG COUNT WINDOW TIMER (A6 Block **H**).

4. Press any key and you should find a 100 us wide, LOW going pulse on LSRQ when the key is pressed.

5. If LSRQ is not correct, probe HI KEY DN SRQ (TP3) with the oscilloscope. Set the oscilloscope to trigger on the HIGH going edge. Each time a key is pressed, you should find a 100 us wide HIGH going pulse. If HI KEY DN SRQ is correct, replace U3.

6. If HI KEY DN SRQ is not correct, lift U3A pin 3 and recheck HI KEY DN SRQ at TP3. Press any key and verify that this signal goes HIGH and stays HIGH. Press **[INSTR PRESET]** and verify that HI KEY DN SRQ returns LOW. If the signal is correct, replace U3. If the signal is incorrect, troubleshoot the KEY DOWN TIMER (A6 Block **C**).

INSTR PRESET BUFFER (A6 BLOCK J)

1. Probe INSTR PR LOCKOUT (U3D pin 12). This signal should be LOW unless the instrument is in REMOTE mode. If this signal is HIGH, troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**).

2. Probe INSTR PRESET (U3D pin 11). This signal should be HIGH and go LOW when the **[INSTR PRESET]** key is pressed. If this signal is correct, proceed to step 6.

3. If INSTR PRESET stays HIGH all the time, check for an open circuit on both the A5 and the A6 boards. You can manually ground this signal at A6P1 pin 24 to verify that the signal at U3D pin 11 goes LOW at the same time. This will cut the problem in half.

4. If INSTR PRESET stays LOW all the time, lift one side of C1 and recheck the level of INSTR PRESET. If this corrects the problem, replace C1.

5. If INSTR PRESET still stays LOW, detach the A6 board from the A5 keyboard. If INSTR PRESET is now correct, remove the INSTR PRESET key switch from the A5 keyboard and check for shorts. If no shorts exist, replace the key switch.

6. If INSTR PRESET is correct, probe U3D pin 13. The signal at this pin should be LOW and should go HIGH when INSTR PRESET goes LOW. If the signal is not correct, check for shorts along the trace and then replace U3 if no shorts exist.

7. Probe LIPS (U3C pin 10). LIPS should be HIGH and go LOW when **[INSTR PRESET]** is pressed. If LIPS is correct, proceed to step 10.

8. If LIPS is LOW all the time, disconnect the front panel ribbon cable from the A6 Keyboard Interface board and probe LIPS on the Motherboard. If LIPS is still LOW, troubleshoot the A52 Positive Regulator board or the A61 Memory board.

9. If LIPS is correct, reconnect the A6 board and lift U3C pin 10. If LIPS is correct after lifting U3C pin 10, replace U3. If LIPS is not correct, check for shorts along the signal trace and then replace U8 if no shorts are exist.

10. Probe U8A pin 2. The signal on this pin should be LOW and go HIGH when **[INSTR PRESET]** is pressed. If the signal is correct, proceed to step 12.

11. Lift U8 pin 2 and recheck the signal at the pin. If the signal is correct, check for shorts along the signal trace and replace U2 if no shorts exist. If the signal is still not correct, replace U8.

12. If the signal at U8 pin 2 is correct, probe ANNUNCIATOR RESET at U2 pin 3. This signal should be HIGH and go LOW when **[INSTR PRESET]** is pressed. If ANNUNCIATOR RESET is not correct, lift U2 pin 3 and recheck right at the pin. If this signal is bad right at the pin, replace U2. If this signal is good with the pin lifted, check for shorts along the signal trace and if no shorts exist, troubleshoot the ANNUNCIATOR LATCHES (A6 Block **E**) to determine which latch input is bad.

A6 KEYBOARD INTERFACE DSA TROUBLESHOOTING

A limited amount of DSA is available on the Keyboard Interface. All of the latched LED Bits and Control Bits as well as the Strobes can be tested for correct operation by using the following main instrument DSA routine and a Signature Analyzer.

1. Ground the LSTS test point on the A60 Processor board and then turn the instrument to STANDBY and then ON. Connect Signature Analyzer as follows:

   START connected to T1 on the A61 Memory board, trigger on the rising edge.

   STOP connected to T2 on the A61 Memory board, trigger on the rising edge.

   CLOCK connected to LIOSB (A60TP4), trigger on the rising edge.

   GRND connected to chassis ground or ground pin.

2. Probe the signals listed in the table below and verify that the signatures match those given.

Mnemonic	Location	Signature
DB0	A6J3-3	H186
DB1	A6J3-4	CFPH
DB2	A6J3-5	H077
DB3	A6J3-6	0942
DB4	A6J3-7	CC29
DB5	A6J3-8	63CP
DB6	A6J3-9	F77H
DB7	A6J3-10	2757
DB8	A6J3-11	P702
DB9	A6J3-12	67A8
DB10	A6J3-13	FU51
DB11	A6J3-14	9PA2
DB12	A6J3-15	3H44
DB13	A6J3-16	37FH
DB14	A6J3-17	CF15
DB15	A6J3-18	H186
ADR0	A6J3-23	AUCU
ADR1	A6J3-24	U154
ADR2	A6J3-25	012F
ADR3	A6J3-26	8U24
ADR4	A6J3-27	7UUF

SIOB	A6J3-47	3704
LEN 4	A6U15 pin 11	P769
LEN 5	A6U15 pin 10	U034
LEN 6	A6U15 pin 9	FAFP
MKR SWP	A6U6 pin 12	8H01
M1	A6U6 pin 9	2156
M2	A6U6 pin 15	79U9
M3	A6U6 pin 6	F8A6
M4	A6U6 pin 16	AA19
M5	A6U6 pin 5	H973
ENTRY ON	A6U6 pin 19	AP4U
KEYBOARD LOCKOUT	A6U6 pin 2	7C63
ALTN	A6U7 pin 19	FH92
EXT	A6 U7 pin 2	A070
SINGLE	A6U7 pin 16	5F49
MAN	A6U7 pin 5	C892
FREE	A6U7 pin 15	7124
LINE	A6U7 pin 6	F5C5
CONT	A6U7 pin 12	C03U
DELTA MRKR	A6U7 pin 9	5C2A
PEAK	A6U16 pin 12	CC23
XTAL	A6U16 pin 9	0UFP
AMPTD MRKR	A6U16 pin 15	6614
PWR SWP	A6U16 pin 6	C5A1
INT	A6U16 pin 16	12FC
RF	A6U16 pin 5	10PH
EXT	A6U16 pin 19	H7A5
INST PR LOCKOUT	A6U16 pin 2	20CH
AM	A6U17 pin 19	38U3
SLOPE	A6U17 pin 2	086U
PULSE	A6U17 pin 16	P6A0
INST CK I	A6U17 pin 5	FH41
INST CK II	A6U17 pin 15	9A82
FM	A6U17 pin 6	CAU3
SHIFT	A6U17 pin 12	0F6P
	A6U17 pin 9	6155

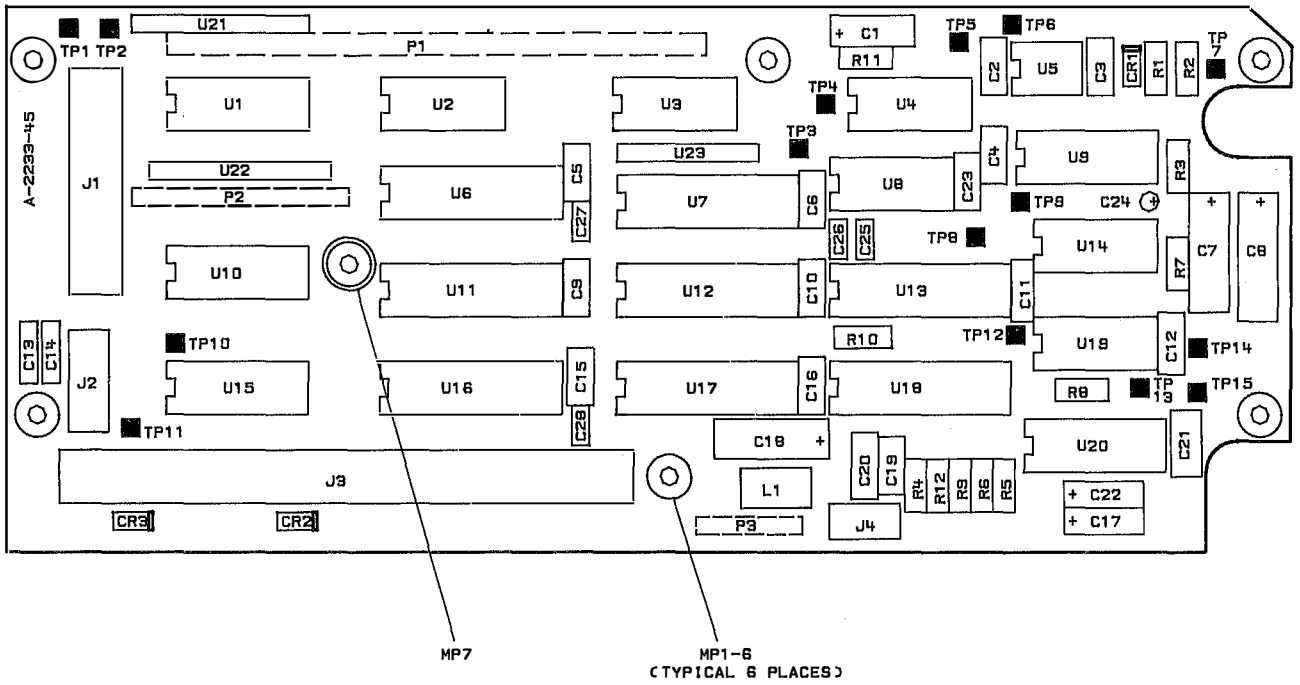


Figure 8H-18. A6 Keyboard Interface, Component Location Diagram

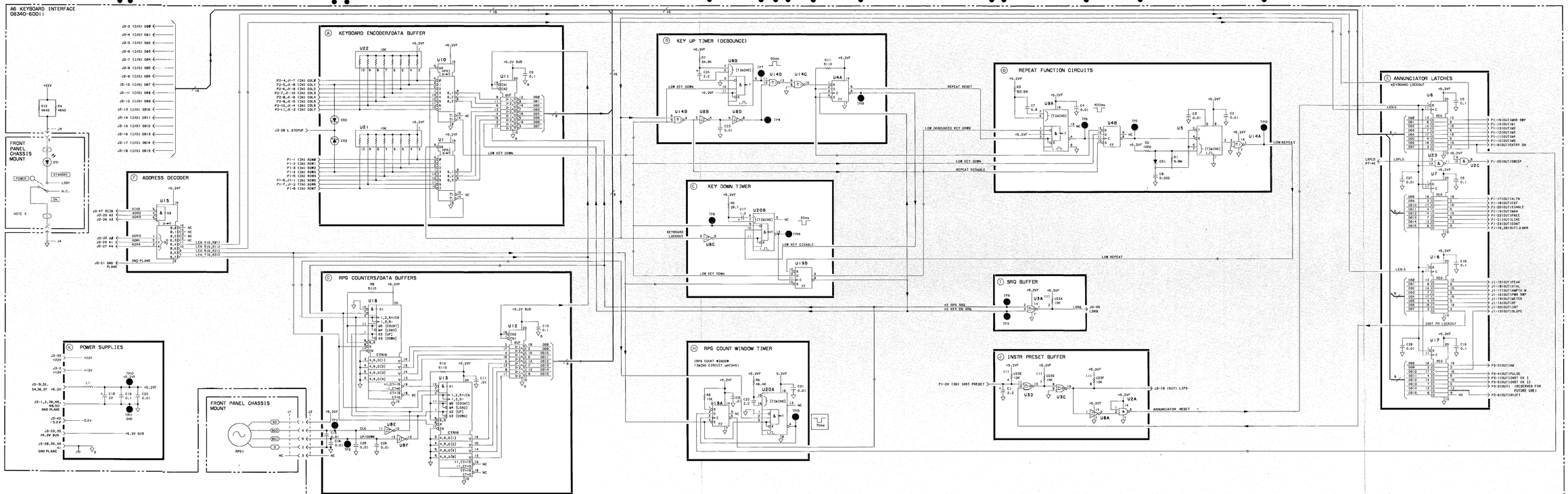


Figure 8H-19. A6 Keyboard Interface Schematic Diagram

REAR PANEL
THEORY OF OPERATION

INTRODUCTION

This Rear-Panel description provides information on the connectors and components located on the HP 8340A Rear Panel. Figure 8H-25, Rear Panel Features, located near the end of this section, shows the components mounted on the Rear Panel.

DESCRIPTION

The assemblies and components mounted on the 8340A Rear Panel perform many different functions which may be divided into the following groups:

- HP-IB - Provides a digital interface by which the 8340A can communicate with other HP-IB-equipped instruments or controllers.

- SWEEP-RELATED INTERFACE LINES - These are signals such as MUTE, PEN LIFT, NEG BLANK, Z-AXIS BLANK/MKRS, EXT TRIGGER INPUT, and STOP SWP IN/OUT. These signals allow the 8340A to interface with external devices such as X-Y recorders or network analyzers. The external device can then determine what state the 8340A sweep is in (sweep in progress, retrace, sweep stopped for band switch, etc). External devices may stop the 8340A sweep with the **STOP SWP IN/OUT**. When the 8340A is in External Trigger mode, the **EXT TRIGGER INPUT** allows an external device to initiate sweeps.

- FREQUENCY STANDARD - The **INT** and **EXT** connectors, in conjuction with the **FREQUENCY STANDARD** switch, allows selection of either the internal or the external frequency standard. The standard is used as a master timebase for the 8340A.

- RF OUTPUTS - All instruments are equipped with **AUX OUTPUT**. Option 004 and 005 instruments have the **RF OUTPUT** connector mounted on the Rear Panel.

- DEDICATED INTERFACE CONNECTORS - Provide interfacing with the HP 8410B/C and the HP 8755C Network Analyzers.

- FAN - Provides instrument cooling.

- LINE MODULE - Holds main line fuse and the line voltage selector cam. This module also suppresses line transients.

BLOCK DIAGRAM

Figure 8H-20, Rear Panel Block Diagram, shows all Rear Panel connectors, the source or destination of the associated signals, and any other assemblies these signals go through.

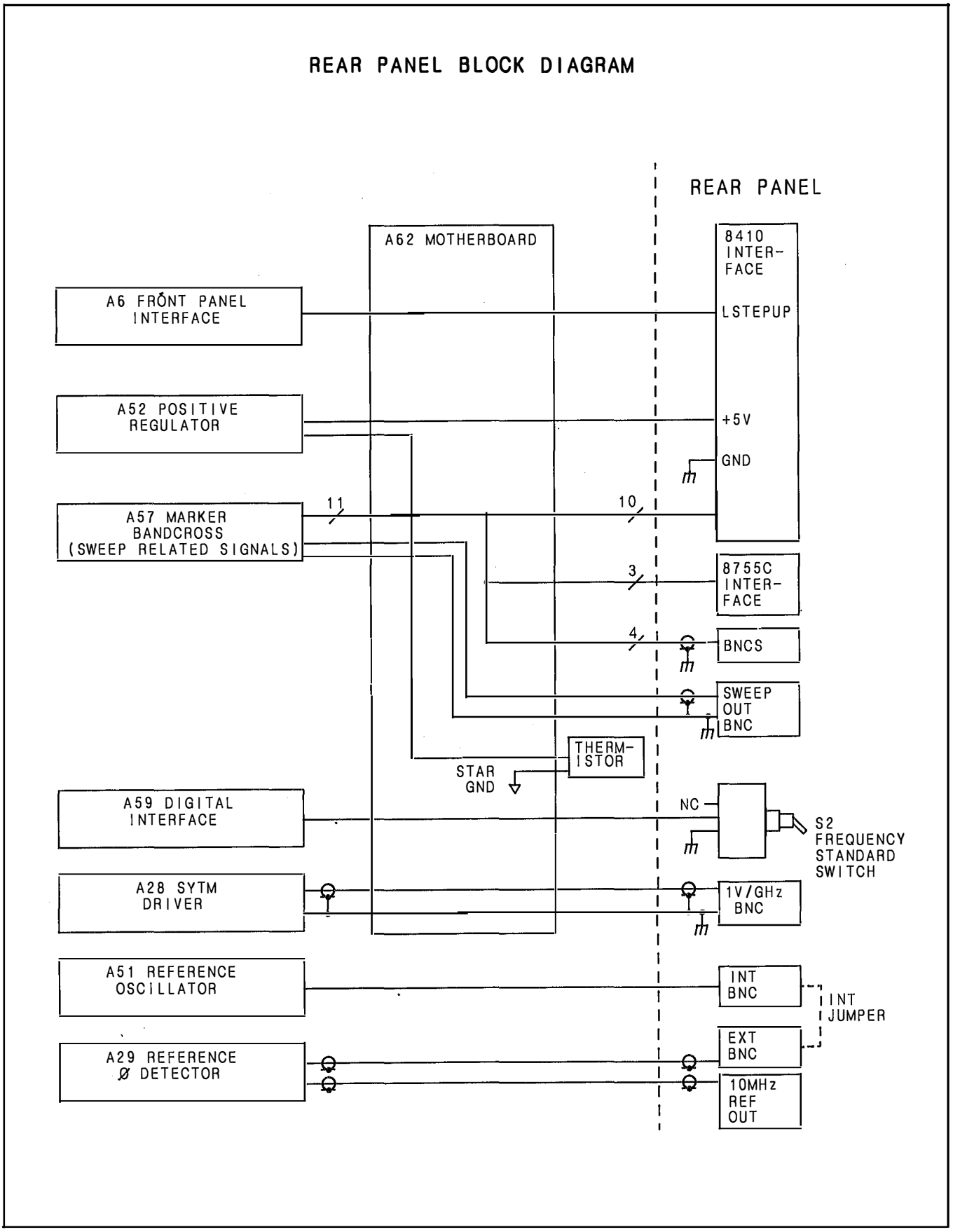


Figure 8H-20. Rear Panel Block Diagram (1 of 2)

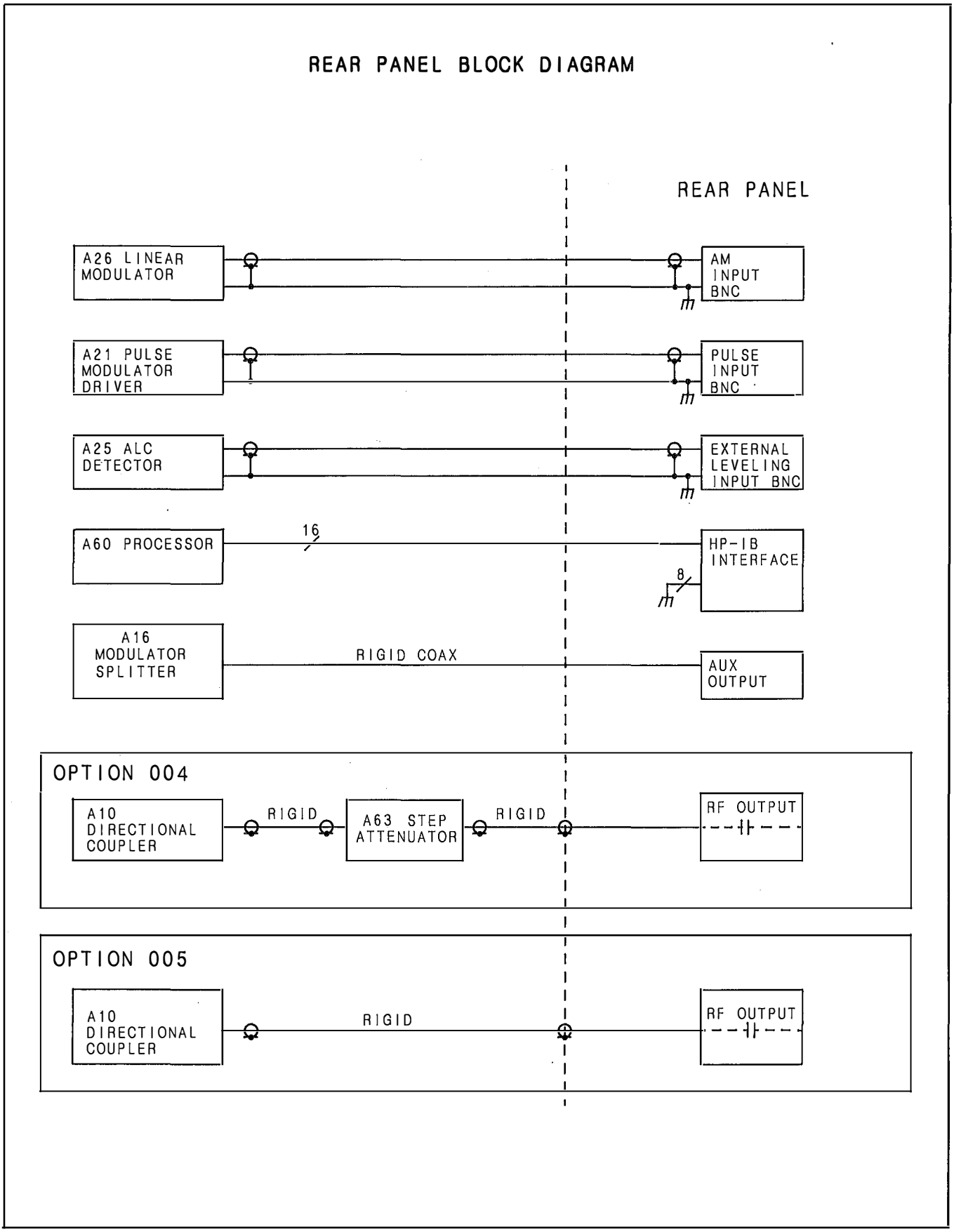


Figure 8H-20. Rear Panel Block Diagram (2 of 2)

REAR PANEL
TROUBLESHOOTING TO ASSEMBLY LEVEL

REAR PANEL CONNECTORS

Refer to Figure 8H-26 to determine the source/destination assembly that generates or receives the signal in question, and which assembly(ies) and/or cable(s) it propagates through. Refer to the **"REAR PANEL INDIVIDUAL ASSEMBLIES"** descriptions for a functional description of each Rear Panel connector.

FAN

Fan troubleshooting information is provided in the **"POWER SUPPLY - FAN"** functional group.

LINE MODULE

Line module troubleshooting information is provided in the **"POWER SUPPLIES -FAN"** functional group.

MECHANICAL ASSEMBLIES

Refer to Section VI, parts list.

REAR PANEL
INDIVIDUAL ASSEMBLIES

LINE MODULE

Description

The line module performs several functions. The main line fuse protects the instrument from line voltage surges, incorrect line voltage, or internal damage due to a short in the line module, transformer, motherboard, or a rectifier board. The line module also suppresses power line transients. The line voltage selector cam allows the user to easily configure the 8340A for operation at different line voltages. The selected voltage is visible through a small window (see Figure 8J-1 in the **"POWER SUPPLIES - FAN"** functional group).

Line Module Troubleshooting

Refer to **"LINE MODULE TROUBLESHOOTING"** in the **"POWER SUPPLIES - FAN TROUBLESHOOTING TO ASSEMBLY LEVEL"** section for troubleshooting information.

LINE MODULE REPLACEMENT

Refer to Figure 8J-5. Transformer - Line Module - Fan Replacement in the **"POWER SUPPLIES - FAN"** functional group for replacement procedures.

RF CONNECTORS

AUX OUTPUT 2.3 - 7 GHz J19

This is a type-N female connector that nominally provides a -3 dBm RF output from the HP 8340A's fundamental YIG oscillator. Impedance of this connector is nominally 50 Ohms.

RF OUTPUT J20

This precision APC-3.5 male connector replaces the standard Front Panel RF output connector in Option 004 and Option 005 instruments. Option 004 has a Rear Panel RF output with attenuator, and Option 005 has a Rear Panel RF output without the attenuator. The specifications for each option are listed in Table 1-1 (Section I of this manual). Output impedance is nominally 50 Ohms. The RF OUTPUT connector has a capacitor built into it. This capacitor is in series with the RF OUTPUT and protects the instrument from DC potentials. The maximum dc voltage that may be applied to the RF connector is 50 Vdc.

Considerable care must be used when working with APC-3.5 connectors. Do not deform the connector by excessive tightening force, and do not allow the connector to become corroded, scratched, or dirty. If cleaning is necessary, use a firm, lint free brush only. Do not use any cleaning solvents since they can chemically damage the plastic bead that supports the center conductor. If this connector is mechanically degraded, high frequency losses will occur.

REAR PANEL BNC CONNECTORS

1V/GHz (19V MAX) J6

This BNC connector has an output voltage that is proportional to the RF output frequency, with a ratio of 1 volt per GHz frequency. The maximum specified output voltage is 19V. Above 19 GHz this output levels off at approximately 20V. Accuracy is 1V/GHz ±1% ±2mV with a load impedance > 4 kohms. (Note: This output is current limited. Loads less than 4 kohms will cause the circuit to current limit at high frequency. An output voltage ratio of 0.5 volts/GHz can be achieved by clipping two jumpers on the A28 SYTM board (see the RF Section functional group). This allows a proportional output for the entire 10 MHz to 26.5 GHz frequency span of the HP 8340A.

SWEEP OUTPUT J7

The output voltage range for this connector is 0 to +10 Vdc. When the HP 8340A is sweeping, the **SWEEP OUTPUT** is 0 Vdc at the beginning of the sweep and +10 Vdc at the end of the sweep, regardless of sweep width. In CW mode, the **SWEEP OUTPUT** is always at 0 volts. In MANUAL mode, the **SWEEP OUTPUT** ranges from 0 Vdc at the 10 MHz minimum frequency, to 10 Vdc at the 26.5 GHz maximum frequency, with proportional voltages at the frequencies between these points.

10 MHz REF OUTPUT J8

This output provides a 10 MHz signal at approximately 0 dBm, derived from the internal frequency standard of the HP 8340A. This can be the master time base reference output for a network of instruments.

INT J9/EXT J10 (SWITCH & BNC CONNECTORS)

These items allow the user to select either the internal (INT) 10 MHz crystal oscillator frequency standard, or an external (EXT) frequency standard to be used as the master timebase for the HP 8340A. To select the internal standard, place the switch in the **INT** position and connect a jumper cable between the **INT** and **EXT** BNC connectors (the **INT** BNC is now outputting 10 MHz at approximately +3 dBm). To use an external standard, disconnect the jumper, change the switch to **EXT**, and connect the external source to the **EXT** BNC connector. The external source must be either 5 MHz ±50 Hz, or 10 MHz ±100 Hz, and provide 1 to +10 dBm into the 50 Ohm BNC connector. When the switch is in the **EXT** position, the internal standard is turned off and the amber **EXT**

REF annunciator lights above the Front Panel **ENTRY DISPLAY.**

EXTERNAL TRIGGER INPUT J11

This input triggers the start of a sweep. Trigger signal must be >2 volts (10V maximum), and wider that 0.5 microseconds. Nominal input impedance is 2 KOhms.

MUTE OUTPUT J12

This output provides an active LOW, TTL signal which causes external X-Y recorders or instruments to pause while the HP 8340A crosses a frequency band switchpoint. The X-Y recorder Operating Guide, located at the end of Section III, explains the interaction of recorders with the HP 8340A.

PENLIFT OUTPUT J13

OPERATION WITH X-Y RECORDERS

PENLIFT disables an X-Y recorder's ability to lower its pen during sweep retrace. If **[SHIFT] [LINE]** is pressed on the Front Panel, PENLIFT will also disable the pen during forward sweep band switchpoints. Because of X-Y recorder limitations PENLIFT will always disable the X-Y recorder's pen at sweep times under 5 seconds.

PENLIFT enables pen operation by providing a current path to ground for the X-Y recorder's pen solenoid. The voltage at the PENLIFT output in this state will be approximately 0 Vdc. Circuit impedance in this state is approximately 0.5 Ohms (Q3 on).

PENLIFT disables pen operation by not providing a current path to ground for the X-Y recorder's pen solenoid. The voltage on the PENLIFT output will be equal to the X-Y recorder's pen solenoid supply voltage. Circuit impedance in this state is very high (Q3 open). A 56.2 volt zener diode protects the PENLIFT circuit from excessively high X-Y recorder solenoid voltages. A57CR10 protects the circuit from negative voltages on the input.

OPERATION WITH TTL LOADS

The PENLIFT output will be at TTL levels if connected to TTL devices.

NEG BLANKING J14

This output provides a negative rectangular pulse (approximately -5 volts into 2 KOhms) during sweep retrace and forward sweep band switchpoints.

Z-AXIS BLANK/MKRS J15

This output supplies a positive rectangular pulse (approximately +5 volts into 2 KOhms) during sweep retrace and forward sweep band switchpoints. This output also supplies a -5 volt pulse when the RF output is coincident with a marker frequency.

STOP SWP IN/OUT J16

When this line is grounded, forward sweeping is stopped. The sweep will resume when this input is released from ground. If this input is grounded during retrace, the retrace will continue but the next sweep will not begin until **STOP SWP IN/OUT** is released from ground. This line is also an output, a TTL LOW indicates that the sweep has been stopped by the 8340A.

NOTE

For troubleshooting information, refer to Figure 8H-26, Rear Panel Assembly, Schematic Diagram located at the end of this section. More information concerning the operational parameters of these BNC signals may be found in Section III of this manual.

8410 INTERFACE J18

The HP 8340A Synthesized Sweeper interfaces with the HP 8410B/C Network Analyzer by means of the Source Control Cable (HP Part Number 08410-60146 CD9). This interface permits multi-octave operation of the 8410B/C with the 8340A. This connector has pins that duplicate several Rear Panel functions, including **EXT TRIGGER INPUT**, **MUTE OUTPUT**, **PENLIFT OUTPUT**, **NEG BLANK**, and **Z-AXIS BLANK/MKRS**. There is also a pin input (LSTEPUP) for a switch closure to execute the **UP** key function, which is used to increment the active Front Panel control function. Figure 8H-21 contains a visual representation of the 8410 Interface Cable.

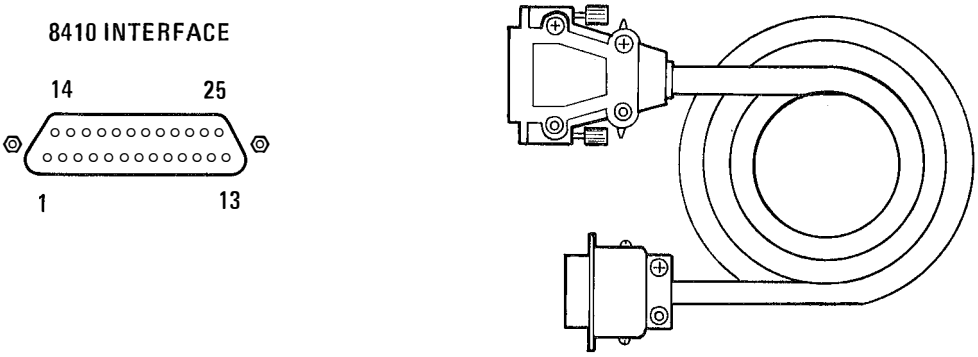
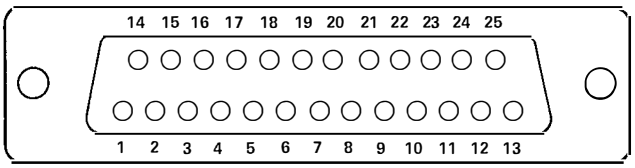


Figure 8H-21. 8410 Interface and Cable

The pin configuration of the 8410B/C INTERFACE and descriptions of all related signals are located in Figure 8H-22.

8410C INTERFACE CONNECTOR J18
(As seen from rear panel)



J18 Pin	Mnemonic	Levels	Input/Output	Signal Source/ Destination	A62J31 Pin	J18W46 Wire Color Code
1						
2	Z-AXIS BLANK	+5V, −5V*	OUTPUT	A57P1-99	2, 16	2
3						
4	LALTSEL	TTL (LOW TRUE)	OUTPUT	A57P1-59	10, 24	0
5	LSSP (LSTOP SWEEP)	TTL (LOW TRUE)	I/O	A57P1-107	5, 19	5
6	+5.2V			A52P1-17, 18, 41, 42	3	3
7						
8						
9	$\overline{\text{MUTE}}$	TTL (LOW TRUE)	INPUT	A57P1-61	8, 22	4
10	EXT TRIG	EXT SOURCE INPUT LEVEL	INPUT	A57P1-106	4, 18	6
11	PEN LIFT	SEE TEXT	OUTPUT	A57P1-108	6, 20	8
12						
13						
14	NEG BLANK	0V, −5V*	OUTPUT	A57P1-41	1, 15	1
15						
16	LRETRACE	TTL (LOW TRUE)	OUTPUT	A57P1-58	11, 25	9 - 0
17	LALTEN	TTL (LOW TRUE)	OUTPUT	A57P1-60	9, 23	9
18						
19	GND			STOP SWEEP BNC GND LUG		9 - 0 - 7
20						
21						
22	LSTEPUP	TTL (LOW TRUE)	INPUT	A62J1-28	14	9 - 0 - 8
23						
24	8410 TRIG	TTL (LOW TRUE)	OUTPUT	A57P1-62	7	7
25						

*See text

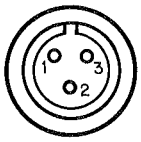
Figure 8H-22. 8410 INTERFACE Connector J18

8755C ALT SWP INTERFACE J17

The HP 8340A can sequence alternate sweeps in the HP 8755C Scalar Network Analyzer with Interface Cable 8120-3174 CD8. Figure 8H-23 shows the pin configuration and complete description of the 8755C ALT SWP INTERFACE signals.

ALTERNATE SWEEP INTERFACE CONNECTOR J17

8755C
ALT SWP
INTERFACE



(viewed from rear of instrument)

Pin	Mnemonic	Description	Level	Wire Color Code	A62J31 Pin	Source
1	LALTEN	LOW to Externally Enable ALT SWP Mode in HP 8755C	TTL OUTPUT	9 - 1 - 5	23	A57P1-60
2	LALTSEL	Channel Select (HIGH =Channel 1, LOW =Channel 2)	TTL OUTPUT	9 - 1- 6	24	A57P1-59
3	LRETRACE	LOW During Retrace	TTL OUTPUT	9 - 1 - 7	25	A57P1-58

Figure 8H-23. HP 8755C ALT SWP INTERFACE J17

HP-IB INTERFACE CONNECTOR J21

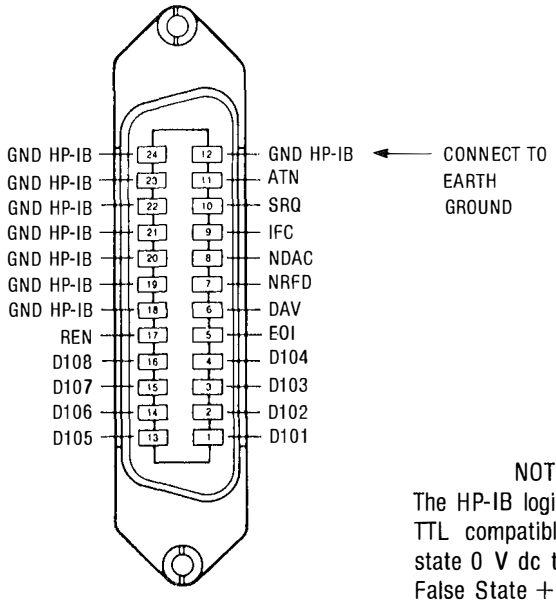
The HP-IB interface allows the HP 8340A to communicate with another instrument or device on the HP-IB bus.

The 8340A's HP-IB may be checked for proper operation by performing the **"HP-IB OPERATION VERIFICATION PROCEDURE"**, located in the **"MANUAL PERFORMANCE TEST PROCEDURES"**, Section IV.

Refer to Figure 8H-24, HP-IB Connector, for further information.

For more information concerning HP-IB operation, refer to the remote programming information in Section III.

HP-IB troubleshooting information may be found in the **"CONTROLLER"** functional group in this manual.

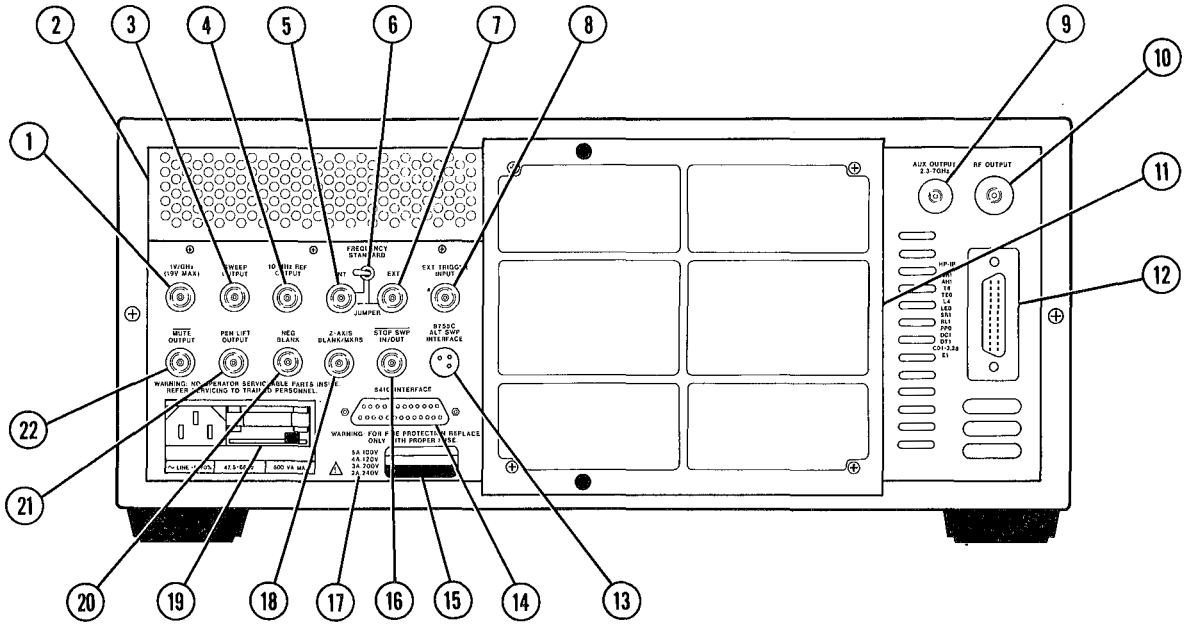


NOTE
The HP-IB logic levels are TTL compatible, ie., true state 0 V dc to 0.4 V dc, False State +2.5 V dc to +5 V dc.

MNEMONICS TABLE

Mnemonic	Description
ATN	LOW = Attention control line
DAV	LOW = Data Valid control line
DIO1 through 8	LOW = Data Input/Output lines
EOI	LOW = End Or Identify control line
IFC	LOW = Interface Clear control line
NDAC	LOW = Data Not Accepted control line
NRFD	LOW = Not Ready For Data control line
REN	LOW = Remote Enable control line
SRQ	LOW = Service Request control line

Figure 8H-24. HP-IB Connector J21



1. 1V/GHz J6
2. HEAT SINK (P/O A62 Motherboard)
3. SWEEP OUTPUT J7
4. 10MHz REF OUTPUT J8
5. FREQUENCY STANDARD INT J9
6. FREQUENCY STANDARD SWITCH
7. FREQUENCY STANDARD EXT J10
8. EXT TRIGGER INPUT J7 – J11
9. AUX OUTPUT 2.3 – 7 GHz J19
10. RF OUTPUT J20 (Option 004 and 005 only)
11. FAN (B1)
12. HP-IB J21
13. 8755C ALT SWP INTERFACE J17
14. 8410 INTERFACE J18
15. SERIAL TAG
16. $\overline{\text{STOP SWP}}$ IN/OUT J16
17. FUSE RATING GUIDE
18. Z-AXIS BLANK/MKRS J15
19. LINE MODULE
20. NEG BLANKING J14
21. PEN LIFT OUTPUT J13
22. $\overline{\text{MUTE}}$ OUTPUT J12

Figure 8H-25. Rear Panel Features

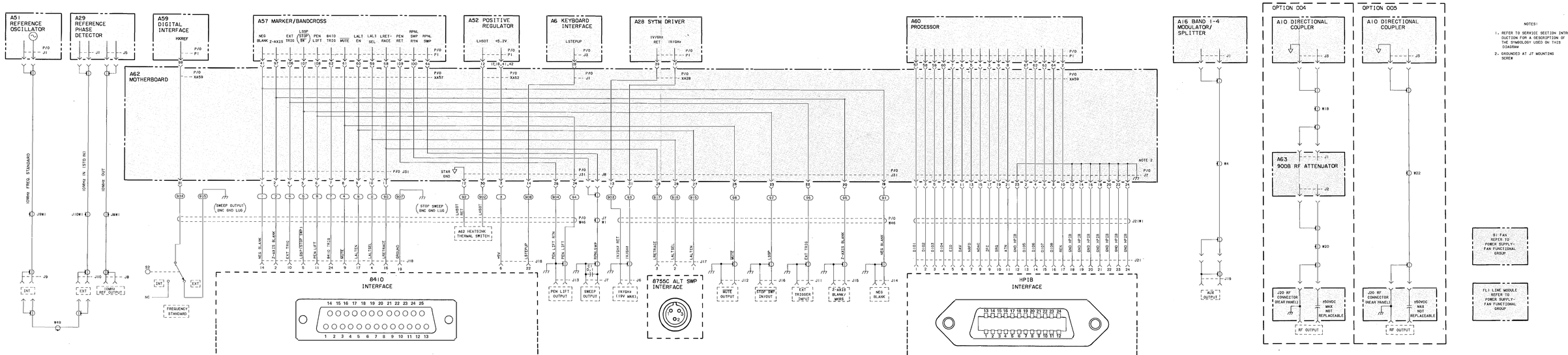
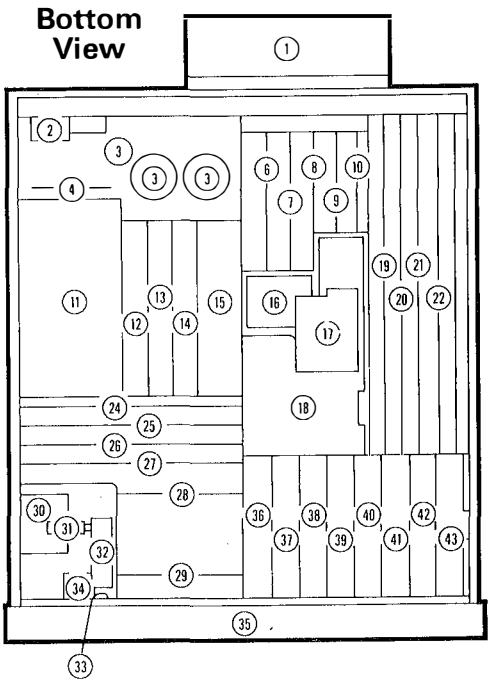
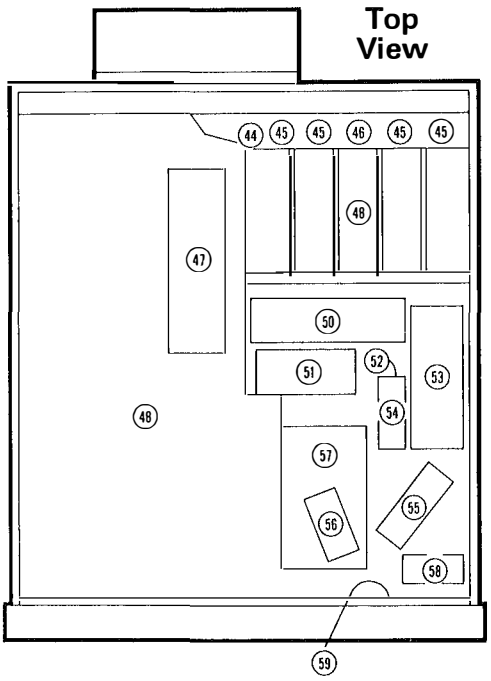


Figure 8H-26. Rear Panel Assembly, Schematic Diagram

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 3					Volume 4		
			Ref.-M/N Loops	20-30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	33					●			
A2	Display Driver	33					●			
A3	Display Processor	33					●			
A4	Not Assigned	-								
A5	Keyboard	35					●			
A6	Keyboard Interface	35					●			
A7	Lower Keyboard	35					●			
A8	3.7 GHz Oscillator	57						●		
A9	Band 0 Pulse Modulator	56						●		
A10	Directional Coupler	32						●		
A11	Band 1-4 Detector	31						●		
A12	Band 0 Splitter/Detector	34						●		
A13	SYTM (Switched YIG Tuned Multiplier)	30						●		
A14	Band 1-4 Power Amplifier	53						●		
A15	Band 0 Low Pass Filter	52						●		
A16	Band 1-4 Modulator/Splitter	51						●		
A17	Band 0 Mixer	54						●		
A18	Band 0 Power Amplifier	55						●		
		60						●		
A19	Capacitor Assembly	48								●
A20	RF Section Filter	50						●		
A21	Pulse Modulator Driver	29						●		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						●		
A25	ALC Detector	27						●		
A26	Linear Modulator	26						●		
A27	Level Control	25						●		
A28	SYTM Driver	24						●		
A29	Reference Phase Detector	12	●							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	●							
A31	M/N Phase Detector	14	●							
A32	M/N VCO (Voltage Controlled Osc.)	15	●							
A33	M/N Output	15	●							
A34	Reference-M/N Motherboard	5	●							
A35	Rectifier	4								●
A36	PLL1 VCO (Voltage Controlled Osc.)	36		●						
A37	PLL1 Divider	37		●						
A38	PLL1 IF	38		●						
A39	PLL3 Upconverter	39		●						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		●						
A41	PLL2 Phase Detector	41		●						
A42	PLL2 Divider	42		●						
A43	PLL2 Discriminator	43		●						
A44	YIG Oscillator (YO)	18			●					
A45	Directional Coupler	18			●					
A46	7 GHz Low Pass Filter	18			●					
A47	Sense Resistor Assembly (YO circuit)	47			●					
	(SYTM circuit)	47						●		
A48	YO Loop Sampler	18			●					
A49	YO Loop Phase/Detector	18			●					
A50	YO Loop Interconnect	17			●					
A51	Reference Oscillator	16	●							
A52	Positive Regulator	6								●
A53	Negative Regulator	7								●
A54	YO Pretune/Delay Compensation	8			●					
A55	YO Driver	9			●					
A56	--15V Regulator	10								●
A57	Marker/Bandcross	19					●			
A58	Sweep Generator	20			●					
A59	Digital Interface	21					●			
A60	Processor	22					●			
A61	Not Assigned	23					●			
A62	Motherboard	49				●				
A63	90 dB RF Attenuator	59						●		
AT1	Peripheral Mode Isolator	58						●		
AT2	15 dB Attenuator	18			●					
B1	Fan Assembly	1								●
A62C1-3	Power Supply Filter Capacitors	3								●
FL1	AC Line Module	2								●
A62Q1-4	Power Supply Regulating Transistors	45								●
A62S1	Power Supply Thermal Switch	44								●
T1	Power Supply Transformer	11								●
A62U1	Power Supply Regulator	46								●

RF SECTION (POWER LEVEL CONTROL) I

RF SECTION
INTRODUCTION

This section provides descriptions and block diagrams for the RF and microcircuit sections. Descriptions for ALC Loop assemblies, SYTM-Related assemblies, and pulse modulation-related assemblies are also supplied.

LIST OF ASSEMBLIES COVERED

The following assemblies are described in this functional group. Some assemblies (microcircuits) are not field repairable. These are described only with a drawing of the assembly and a schematic drawing, Figure 8I-42, RF Section Schematic Diagram.

- A8 3.7 GHz Oscillator
- A9 Band 0 Pulse Modulator
- A10 Directional Coupler
- A11 Band 1-4 Detector
- A12 Band 0 Splitter/Detector
- A13 SYTM (Switched YIG-Tuned Multiplier)
- A14 Band 1-4 Power Amplifier
- A15 Band 0 Low Pass Filter
- A16 Band 1-4 Modulator/Splitter
- A17 Band 0 Mixer
- A18 Band 0 Power Amplifier
- A20 RF Section Filter
- A63 RF Attenuator/J5 RF OUTPUT Connector
- AT1 Peripheral Mode Isolator
- A21 Pulse Modulator Driver
- A24 Attenuator Driver/SRD Bias
- A25 ALC Detector
- A26 Linear Modulator
- A27 Level Control
- A28 SYTM Driver/A47 Sense Resistor Assembly (SYTM Circuit)

RF SECTION
THEORY OF OPERATION

INTRODUCTION:

This section provides an overall description of the RF Section as well as a brief description of the following:

- Microcircuit Assemblies
- ALC Loop Assemblies
- SYTM-Related Assemblies
- Pulse Modulation-Related Assemblies

This section also contains a Simplified Block Diagram and an RF Section Schematic Diagram for the A8 - A18, A20, A63 and AT1 assemblies.

RF SECTION, OVERALL DESCRIPTION

The RF Section contains the microcircuits and printed circuit boards that produce, amplify, and control the RF output. A brief discussion about the function of the microcircuits will be covered first, followed by the Automatic Leveling Loop and Pulse Modulation operation. The last three paragraphs will cover the Switched YIG Tuned Multiplier (SYTM) and its associated assemblies. Figure 8I-1 contains an RF functional group simplified functional block diagram.

RF power generated by the YIG Oscillator in the YO Loop is delivered to the Mod/Splitter in the RF Section. The Mod/Splitter couples off a portion of this signal to provide an auxilary output at the rear panel of the 8340A. The RF is split again to provide RF to the Band 1-4 Power Amplifier and swept LO to the Band 0 Mixer.

Band 0 (.01-2.3 GHz) is produced by mixing a high power swept LO signal with a fixed RF signal. This RF signal is generated by the 3.7 GHz oscillator and passes through a linear modulator, the pulse modulator, and low pass filter before reaching the mixer. The output frequency of the mixer is the difference between the LO and the RF frequencies [F(IF)=F(LO)-F(RF)]. So by sweeping the LO from 3.71 to 6.0 GHz the IF sweeps from 0.01 to 2.3 GHz. The IF is amplified by the Band 0 Power Amplifier and enters the Band 0 Splitter/Detector where a small portion of the signal is split off and detected for leveling. The leveled RF then enters the SYTM. The SYTM provides a straight through path for the RF from the Band 0 Splitter/Detector when Band 0 is activated. After the SYTM the signal passes through the Directional Coupler, which performs no funcion in Band 0, and the Step Attenuator before reaching the instrument output connector.

Bands 1 through 4 (2.3-26.5 GHz) are obtained by feeding the RF output from the Mod/Splitter through the Band 1-4 Power Amp. The SYTM generates harmonics from the high level output of the Power Amp to produce Bands 2-4. The SYTM contains a bandpass filter that is tuned to the desired RF output frequency. As a result the SYTM passes the desired RF output frequency and rejects the unwanted harmonic related signals. The Directional Coupler couples off part of the RF output from the SYTM to the Band 1-4 Detector for leveling in Bands 1-4. The Step Attenuator is used in all bands when low power output levels are needed.

Leveling is accomplished through the automatic level control circuit (ALC). The ALC uses feedback to hold the RF output constant throughout the entire frequency range of the 8340A. When internally leveled and operating in Bands 1-4, voltage from the

Band 1-4 Detector is fed through a log amplifier and summed with a correction level that closely approximates the variations of the RF attenuator and RF cables. The corrected detector level is then fed through the sample/hold and is routed on to the Linear Modulator Driver Board. Here the corrected detector voltage is summed with the reference voltage at the input of the integrator. If the corrected detector voltage is not equal to the reference voltage the integrator output voltage will change. The integrator output drives an exponential driver that feeds current to the linear modulator in the Mod/Splitter. This changes the RF output level, and hence the detected voltage from the Band 1-4 Detector. The integrator voltage will continue to change until the corrected detector voltage cancels the reference voltage. Leveling in Band 0 uses the same ALC by switching in the Band 0 Splitter/Detector in place of the Band 1-4 detector. The modulator drive is also switched to the A9 Band 1-4 Modulator in the 3.7 GHz oscillator.

Pulse modulation in the 8340A requires special drive circuitry and modulators to achieve narrow pulse widths. The pulse modulator for Bands 1-4 is located in the Mod/Splitter and the pulse modulator for Band 0 is located just after the 3.7 GHz oscillator. The pulse modulator drive circuitry coordinates the ALC operation with the pulse signal. When the pulse input is driven low to turn off the RF the ALC is signaled to sample and hold the current RF level. During the time the pulse input is held low the output is attenuated by more than 80 dB. When the pulse input is returned to its normal high level the ALC releases the hold circuits and the instrument returns to the RF level it had before the RF was turned off.

The SYTM contains a step recovery diode (SRD) which generates the harmonics for Bands 2-4. The ability of the SRD to generate harmonics is effected by power level, frequency and DC bias. For maximum conversion efficiency the SRD bias is varied with power level and frequency. In Band 1 (2.3-7.0 GHz) the SRD is biased on to allow the fundamental to pass through. The SYTM also contains a YIG-tuned bandpass filter that can be tuned over Bands 1-4 (2.3 to 26.5 GHz frequency range) by changing the magnetic field. The passband of the filter must track closely the YO frequency, or some harmonic of it, to cover Bands 1-4. The SYTM Driver compensates for nonlinearities in the tuning magnet, past magnetic history, and magnetic delay. The Pin Switch in the SYTM allows the Band 0 signal to be switched off when Bands 1-4 is selected. Bias for this switch is generated on the Attenuator Driver/SRD Bias Board.

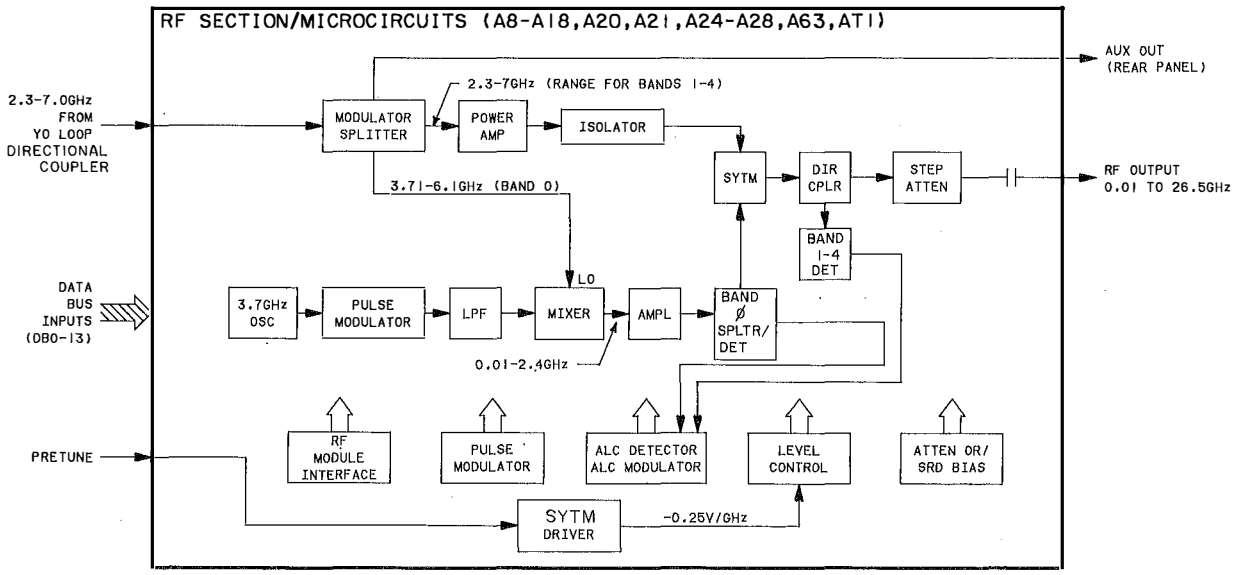


Figure 8I-1. RF Functional Group, Simplified Block Diagram

MICROCIRCUIT ASSEMBLIES

Introduction

The RF section includes all but two of the high frequency microcircuits, with their bias boards, that produce the RF output. The A44 YIG Oscillator (YO) and the A45 Directional Coupler are discussed in the YO LOOP Section. The components in this section include A8 through A18A1, AT1, and A63. The connections between microcircuits and other assemblies are shown on the troubleshooting block diagram.

A16 Band 1-4 Modulator/Splitter

Refer to Figure 8I-18, "A16 Band 1-4 Modulation/Splitter, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The A16 Modulator/Splitter divides the YO output into three paths. Band 0 output provides LO drive (+9 to +16 dBm) for the Band 0 Mixer. The output for Bands 1-4 delivers +9 to +16 dBm to the Band 1-4 Amp. And the third output port provides approximately 0 dBm to the Aux Output.

The Modulator/Splitter uses three PIN diode modulators. The Pulse Mod input drives the PIN diode pulse modulator full on or full off, and provides an RF on/off ratio of greater than 80 dB for pulse operation in Bands 1 through 4. The MOD HI input drives the linear modulator and provides amplitude control for Bands 1 through 4 and is used for amplitude leveling. The third modulator (located after the splitter) is used as a PIN switch and blocks the RF from entering the Band 1-4 section while Band 0 is activated.

The A16A1 Mod/Splitter Bias Board provides the required voltages for the 2 FET buffer stages. Adjustment resistors G1 and G2 are set at the factory for best harmonic performance.

A17 Band 0 Mixer

Refer to Figure 8I-19, "A17 Band 0 Mixer, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The A17 Mixer mixes a fixed 3.7 GHz signal with the swept 3.71 to 6.0 GHz YO output, producing the 0.01 to 2.3 GHz RF output in Band 0. Unwanted mixing products are minimized by a 3.7 GHz directional filter located before the single balanced mixer and a 2.75 GHz low pass filter at the output. The swept YO output, after passing through the A16 Modulator/Splitter, acts as the Local Oscillator signal for the mixer. Conversion loss of the assembly is high due mainly to the 3.7 GHz filter. Loss is approximately 9 dB at 1

GHz.

A8 3.7 GHz Oscillator

Refer to Figure 8I-10, "A8 3.7 GHz Oscillator, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The A8 3.7 GHz Oscillator provides a fixed 3.70 GHz RF output. The A8A1 Oscillator Microcircuit and A8A2 Oscillator Bias Board are located inside the A8 3.7 GHz Oscillator housing. This source is phased locked to the 100 MHz internal standard. A linear modulator is located at the output of the oscillator and provides amplitude control from nominally +1 dBm to -70 dBm.

The A8A2 3.7 GHz Oscillator Bias Board provides the necessary circuitry to amplify the 100 MHz input signal and phase lock the 3.7 GHz signal to it. A lock signal is generated when the oscillator is phase locked to the 100 MHz. The +20V and -10V microcircuit Bias Voltages are also delivered through the Bias Board.

A9 Band 0 Pulse Modulator

Refer to Figure 8I-11, "A9 Band 0 Pulse Modulator, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The A9 Pulse Modulator is a shunt PIN diode modulator and provides an on/off ratio greater than 80 dB in Band 0.

A15 Band 0 Low Pass Filter

Refer to Figure 8I-17, "A15 Band 0 Low Pass Filter", and Figure 8I-42, "RF Section Schematic Diagram". The A15 Low Pass Filter greatly attenuates the harmonics from the 3.7 GHz Oscillator and hence minimizes unwanted mixing products produced in the A17 Band 0 Mixer.

A18 Band 0 Power Amplifier

Refer to Figure 8I-20, "A18 Band 0 Power Amplifier, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The A17 Band 0 Power Amplifier is a bipolar amplifier and provides approximately 40 dB of gain with 20 dBm output power from 0.01 to 2.3 GHz. At 20 dBm, harmonic output is less than -25 dBc.

The A18A1 Band 0 Power Ampifier Bias Board provides the various bias currents for the Band 0 Amplifier. It is matched and attached at the factory, has no adjustments or replaceable parts, and cannot be replaced separately as an assembly. The +20V and -10V lines provide power. When the RF is OFF or the 8340A is operating in Bands 1-4, the -10 volt bias is removed, shutting

down the amplifier.

A12 Band 0 Splitter/Detector

Refer to Figure 8I-14, "A12 Band 0 Splitter/Detector, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The A12 Band 0 Splitter/Detector samples and detects the RF amplitude for Band 0 leveling. The device consists of a resistive power splitter and a Schottky diode detector. The Splitter stage has very good port matching characteristics. The detector stage produces a positive output proportional to the RF power. LDET BW input switches in additional filtering for leveling below 400 MHz. A thermistor (mounted inside the splitter/detector package) is used to compensate for detector temperature variations.

A14 Band 1-4 Power Amplifier

Refer to Figure 8I-16, "A14 Band 1-4 Power Amplifier, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The A14 Band 1-4 Power Amplifier is a GaAs FET amplifier that covers the 2.3 to 7.0 GHz frequency range. The amplifier provides approximately 26 dBm output power. The small signal gain is typically 25 dB but at maximum leveled output the amplifier can be 10 dB into compression.

A notch filter with its center frequency at 7.0 GHz is used to reduce harmonics out of the amplifier. This filter is switched in when the amplifier is operating below 4.5 GHz. Above 4.5 GHz the filter is switched out to allow maximum YO output power. The switching circuitry is on the A14A1 bias assembly and is controlled by the YO 1.4 Volts/GHz signal.

The A14A1 Bias Board assembly contains several factory adjusted gate bias potentiometers. These are set at the factory for optimum output power and minimum harmonics. The drain supply to the first two stages is removed when the RF is off or the 8340A is operating in Band 0.

AT1 Peripheral Mode Isolator

Refer to Figure 8I-23, "AT1 Peripheral Mode Isolator, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". AT1 Isolator provides 20 dB of isolation and has less than 1 dB of insertion loss. AT1 improves the match to the Switched YTM.

A13 SYTM (Switched YIG-Tuned Multiplier)

Refer to Figure 8I-15, "A13 SYTM, Component Location Diagram",

and Figure 8I-42, "RF Section Schematic Diagram". The A13 SYTM (Switched YIG-Tuned Multiplier) uses a PIN diode switch to turn the Band 0 signal off when Band 1-4 is selected. For Band 0, the SYTM provides a straight through path for the 0.01 to 2.3 GHz RF from the A12 Band 0 Splitter/Detector. Insertion loss for Band 0 is typically less than 0.5 dB.

For Bands 1 through 4, the RF input from the AT1 Isolator is fed to the SYTM. This RF input is applied through an impedance matching circuit to a Step Recovery Diode (SRD) which has an output that is rich in harmonics. The SRD BIAS applied to the diode is changed for each band to optimize the generation of the harmonic used for that band (Band 1 = Fundamental, Band 2 = Second Harmonic, Band 3 = Third Harmonic, Band 4 = Fourth Harmonic). The YIG Tuned Filter is a tunable bandpass filter which is tuned to the RF output frequency by the SYTM Coil drive-current supplied by the A28 SYTM Driver.

The filter's bandpass frequency is determined by a small YIG sphere with a resonant frequency that depends on the surrounding magnetic field strength. The magnetic field is established by an opposing pair of electromagnet coils. Changing the current through the coils changes the magnetic field strength, and hence the bandpass frequency.

A10 Directional Coupler

Refer to Figure 8I-12, "A10 Directional Coupler, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The A10 Directional Coupler has a -16 dB coupling coefficient. The reverse-coupled port is terminated. The coupled output is sent to the A11 Band 1-4 Detector for leveling in Bands 1 through 4. Although the Band 0 output (0.01-2.3 GHZ) must pass through the A10 directional Coupler, it plays no part in Band 0 leveling. The insertion loss is less than 1.3 dB at 26.5 GHz.

A11 Band 1-4 Detector

Refer to Figure 8I-13, "A11 Band 1-4 Detector, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The A11 Band 1-4 Detector detects the RF amplitude for leveling in Bands 1-4. It produces a positive output proportional to the RF power in the same way as the Band 0 Detector.

A63 RF Attenuator/J5 RF OUTPUT Connector

Refer to Figure 8I-22, "A63 90 dB Programmable RF Attenuator, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The RF Attenuator provides 90 dB of attenuation in 10 dB steps. Combined with the range of the ALC

loop, this yields a maximum power range of +20 to -110 dBm. The Step Attenuator functions as four fixed attenuators, with 10, 20, and two 30 dB attenuators. Latching relays close contacts which either insert these attenuators in the RF path or bypass them. The control and drive circuitry for the attenuator is located on the A24 Attenuator Driver/SRD bias Board. The insertion loss, with 0 dB attenuation selected is less than 2.8 dB at 26.5 GHz.

The J5 RF Output Connector is a APC-3.5 male RF connector with a series 1000 pF (non-replaceable) capacitor to provide DC blocking. The maximum dc voltage allowed across this capacitor is 50 volts.

ALC LOOP ASSEMBLIES

Description

The ALC Loop is a feedback control system which monitors RF power and maintains that power at a set level. The point at which the power is monitored may be inside the instrument (internal leveling), or the user may choose to monitor power at some point in his test setup (external leveling). A voltage derived from the power sensor (internal crystal detector, external crystal detector, or external power meter) is compared to a reference voltage at the loop summing point (Figure 8I-2, "Leveling Loop, Simplified Block Diagram"). If the resulting currents at the summing node do not cancel, the loop integrator output voltage will change. This voltage controls the modulator which varies the RF output power. The power will thus change until the voltage representing RF power cancels the reference, at which point the integrator output stops changing and the power remains constant. The feedback loop reduces the current into the integrator to zero. For any given reference voltage there is one detector output voltage which causes zero integrator current. Thus, the loop is controlling detector output voltage.

The detector output voltage is a function of RF power into the detector, but it also varies with temperature and RF frequency. Thus, forcing the detector output voltage to some particular level does not guarantee that the RF power will remain constant as the temperature or frequency changes.

A 16 dB directional coupler is used to sample the RF output power. Its coupled arm produces a signal 16 dB smaller than the level of the outgoing RF power. Any RF power coming into the instrument from the outside is ideally not coupled to the coupled arm at all. The detector is connected to the coupled arm. The 16 dB coupling factor is not perfectly flat (constant as a function of RF frequency), and the coupler does couple some reverse power into the detector. There is a 10 dB step attenuator (max 90 dB) between the coupler and front panel output connector, which is not flat either. Thus, as the leveling loop holds the detector output voltage constant, the RF output power will vary with frequency due to the flatness of the detector, coupler, attenuator, and RF hardware. If plotted on a graph, this variation can be approximated with several straight line segments to within ±1 dB. Straight line variations can be compensated out by making the reference voltage change as a function of frequency. This is essentially what is done using the "level correction" voltage produced on the A27 Level Control board. The temperature characteristics of the detector are corrected by temperature compensation circuits on the A25 ALC Detector board.

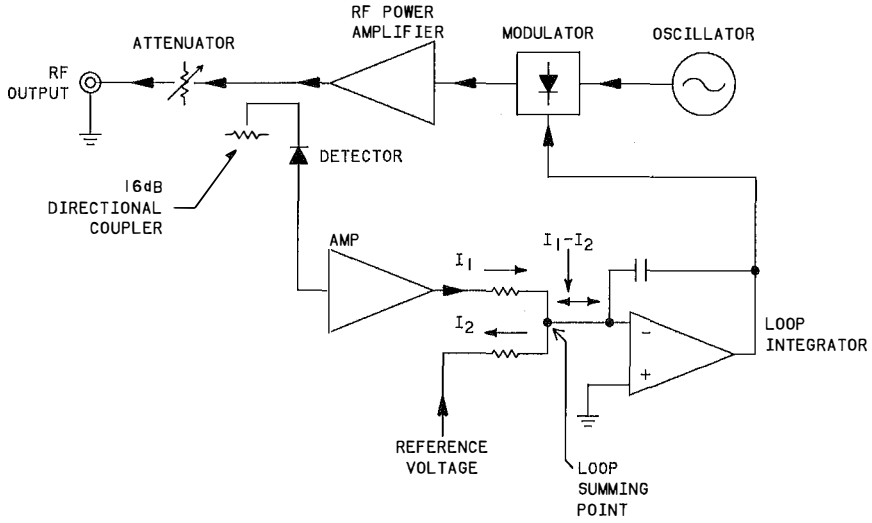


Figure 8I-2. Leveling Loop, Simplified Block Diagram

The normal range of power at the output of the coupler is from 0 dBm to -10 dBm. The attenuator is used to get lower powers. For instance, -56 dBm is achieved with 50 dB attenuation and the ALC loop set to -6 dBm. The loop is not normally set to less than -10 dBm for noise and drift reasons (the detector output is approximately 1 mV for -10 dBm RF output). The maximum attenuation is 90 dB. To get from -100 dBm to -110 dBm, the ALC is run from -10 dBm to -20 dBm. For powers greater than 0 dBm, the ALC Loop is run at the desired power. At some frequencies, the 8340A is capable of producing +20 dBm, the maximum power the ALC can be set to. To get +20 dBm output, the power amplifier is driven into saturation by about 10 dB. Thus, to reduce its output 30 dB (to -10 dBm), the amplifier input must be reduced 40 dB. This is done by the modulators which consist of PIN diodes shunting a transmission line. Another 20 dB of range is needed to provide 90% AM capability. The modulator has over 80 dB range, and is 60 dB down with less than 10 mA drive.

The attenuation of the modulator is a very non-linear function of drive current. If plotted on log-log paper, however, the plot is straight over the high current end of its range. If fed from a current source which is offset by about 1 mA, as shown in Figure 8I-3, "Modulator Characteristics", the plot of attenuation in dB vs. log I is quite straight over its entire range. Since the bandwidth and stability of the ALC Loop are a function of the gain and frequency response of each element in the loop, it is desirable that these parameters not change with operating conditions such as RF frequency and power level. Although not at all linear, the modulator characteristic described above lends itself to the construction of a constant gain ALC Loop. Let the output current from the current source circuit be an exponential function of some control voltage, as with the bipolar transistor in Figure 8I-3, "Modulator Characteristics". Then if the control voltage corresponding to each current is written along the current axis on the chart, one recognizes a characteristic whereby attenuation in dB's is linear with control voltage. In this case, the slope is -1 dB/mV. This sensitivity will be the same anywhere downstream of the modulator. For example, the output of the coupled arm of the coupler will vary -1 dB/mV. This sensitivity will be independent of variable RF losses (frequency response of components), and oscillator power. Furthermore, this scheme handles any non-linear element which can be described by;

$$V_{out} = (V_{in})^N$$

such as a properly biased harmonic frequency multiplier. The sensitivity simply is multiplied by the scalar N, remaining constant over all amplitudes.

The remaining non-linear element in the loop is the crystal detector. The ALC Loop operates from -20 dBm to +20 dBm. The detector is connected to a 16 dB coupler, so it is driven by signals ranging from -36 dBm to +4 dBm. Below -15 dBm, the detector is in its "square law" region where its output voltage is given by:

$$V_{det} = K_2 * V^2_{RF}$$

K2 is temperature dependent. At +4 dBm, the detector is almost into the linear region where

$$V_{det} = K_1 * V_{RF}$$

K1 is not temperature dependent. Between -15 dBm and +10 dBm, the detector exhibits a smooth transition between the asymtotes described by the above formulas (Figure 8I-4, "Detector Characteristics"). Let the detector output be processed by a log converter described by:

$$V_{LOG} = (kT/q) * \ln (V_{DET}/10\ mV)$$

V log is plotted next to Vdet in Figure 8I-4, "Detector Characteristics". Note that when the detector is in its square law region, V log changes 6 mV for each 1 dB change in RF, independent of RF level. In the linear region, the change is 3 mV/dB. A special log converter has been designed which smoothly changes its slope from:

At low levels: $(kT/q) * \ln (V_{det}/10\ mV)$

to

At high levels: $2(kT/q) * \ln (V_{det}/10\ mV)$.

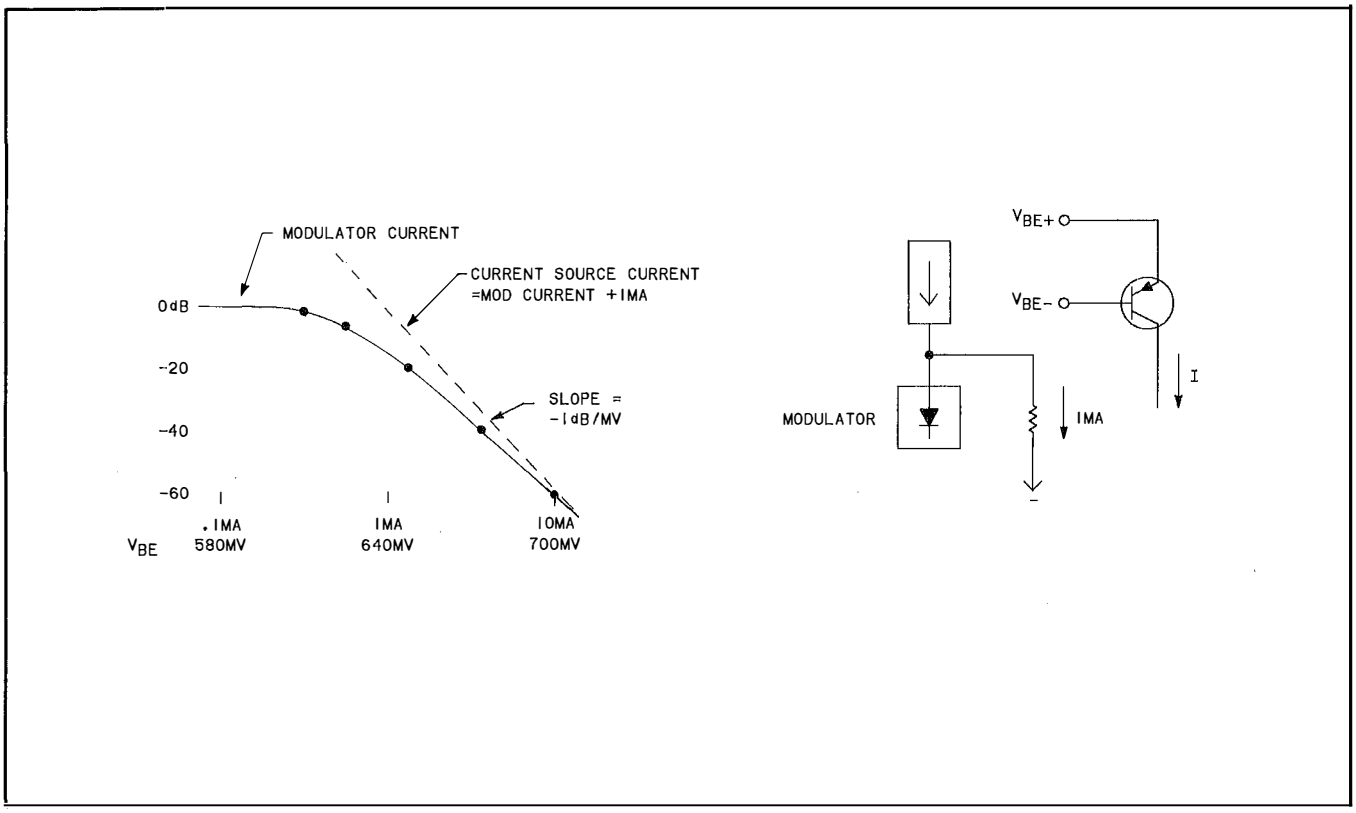


Figure 8I-3. Modulator Characteristics

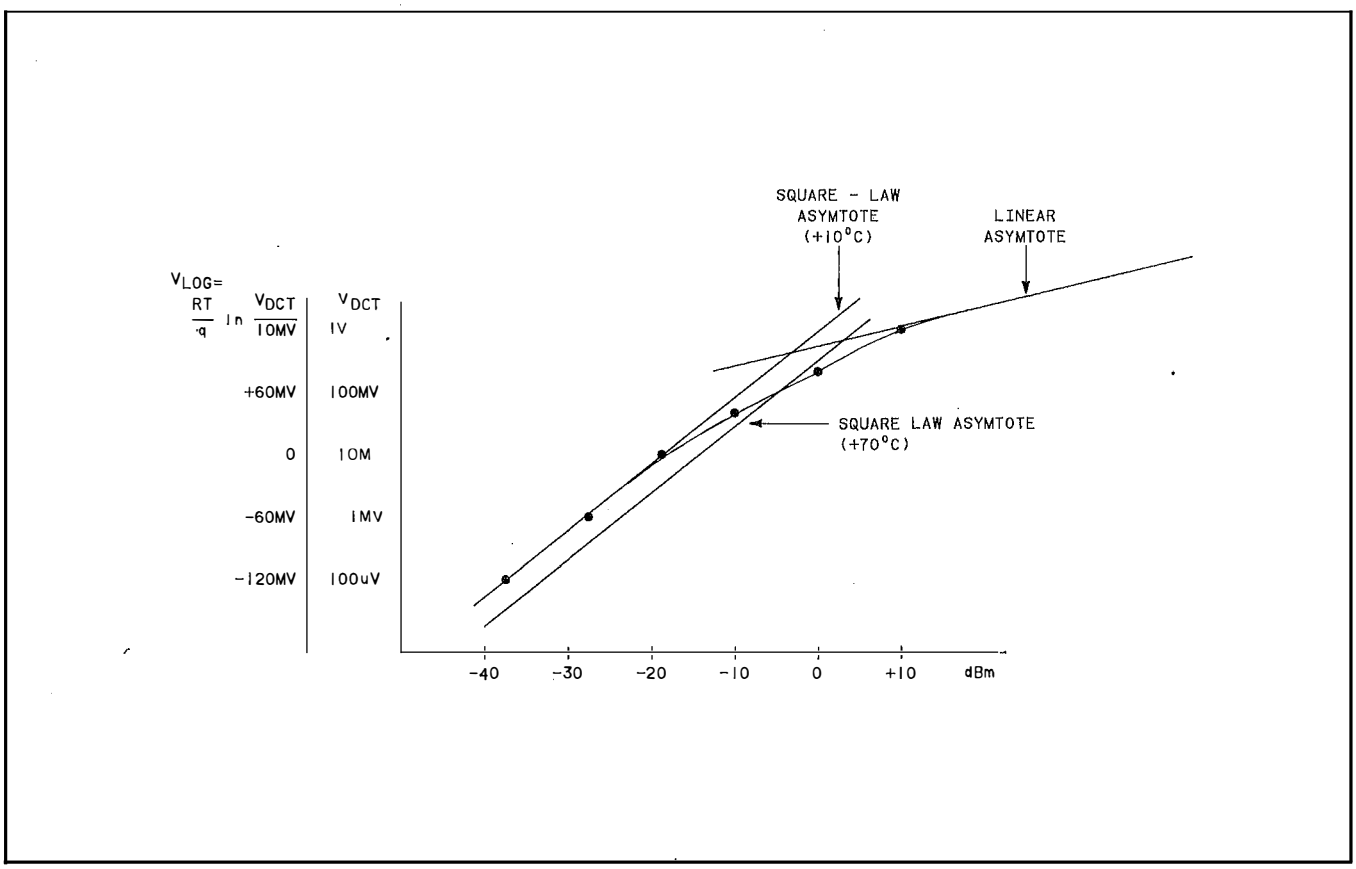


Figure 8I-4. Detector Characteristics

The transition matches that of the detector, and the circuit contains temperature compensation of the square law asymtote. The output of this logger is a constant 6 mV/dB, independent of RF level and detector temperature. The logger itself is temperature dependent due to the kT/q term. This variation is compensated by making the ALC reference voltage vary with temperature.

The combination of exponential modulator drive and dual-slope logger completely cancels (ideally) the gain variations of the RF hardware. In this example, a 1 mV change in modulator drive always produces a 6 mV change out of the logger. Since the rest of the circuitry in the loop is linear, a constant gain loop is realized. Actually, since all is not perfect, the gain varies $\pm$3 dB over frequency and 40 dB of power level. The actual modulator driver has a sensitivity of -.03 dB/mV to reduce noise sensitivity.

Figure 8I-5, "ALC Loop, Detailed Block Diagram", is a detailed block diagram of the ALC Loop without the RF hardware. The 8340A has two RF signal generation paths, one producing 0.01 - 2.3 GHz (Band 0), the other producing 2.3 - 26.5 GHz (Band 1-4). Each path has its own modulator and crystal detector. The dual slope logger has FET switches at its input to select the appropriate detector. The thermistor used for the detector temperature compensation is physically located inside the Band 0 Detector housing. This is mounted directly to the Band 1-4 Directional Coupler to which the Band 1-4 Detector is connected. Thus, the thermistor thermally tracks both detectors. The Band 0 Detector is designed to have the same temperature drift as the Band 1-4 detector.

The x5 amplifier following the logger has several functions. It has a high input impedance to prevent loading the logging elements. It boosts the signal to a high enough level so that noise, drift, and sample/hold offsets are not a problem. It is capable of driving the Sample and Hold capacitor which follows. It provides a point to add the level correction signal.

The level correction signal compensates for the frequency response of the RF hardware. If the instrument is sweeping frequency and the modulator is continually adjusted to keep the output power constant, the detector output voltage will not be constant due, to unflatness in the attenuator, coupler, detector, and connecting hardware. The level correction signal is made to approximate this unflatness with three straight line segments. This signal gets added to the detector voltage so that the output of the x5 amp is flat with frequency. This voltage is now an accurate representation of the actual front panel output power and is used to drive the front panel level meter as well as close

the feedback loop. The level correction signal could have been added at several other places in the loop but was done here for the benefit of the level meter. The level meter is read by the Test Analog-to-Digital Converter (ADC) on the A27 assembly. The output of the Test ADC is a digital representation of the actual Front Panel Output Power. The processor converts this into the appropriate display value for the Front Panel POWER dBm display.

During normal operation the instrument processor does not monitor the Test ADC output. The POWER dBm display is then a duplication of the ENTRY DISPLAY. During AM modulation, External leveling or when an unleveled condition occurs, the POWER dBm display indication is a function of the Test ADC output.

Following the x5 amplifier is a sample/hold circuit which is there primarily for pulse modulation. The 8340A provides internally leveled pulse modulation for pulse widths as narrow as 100 nanoseconds. Since the ALC Loop has a loop bandwidth of 100 KHz (rise time approximately 4 usec), the loop cannot be expected to generate shorter pulse widths. In pulse mode the linear modulator is held at a fixed level and another modulator (the pulse modulator) turns the RF ON and OFF with 10 nsec rise and fall times. The ALC circuitry must measure the detector voltage when the pulse is ON and use this information to control the linear modulator. The detector Sample and Hold gate is closed when the RF is ON, open when it is OFF. (The signal controlling the Sample and Hold gate is delayed to account for propagation delays through the logger and amplifier.) The Sample and Hold serves to stretch narrow pulses, holding their amplitude during the 10 usec that the integration gate is closed. It also provides a steady voltage to the level meter during pulse operation as well as during RF blanking.

The level meter signal is amplified by a factor of 6.6, to 200 mV/dB. The output of this amplifier is +5.0V at -25 dBm, -5.0V at +25 dBm. This voltage goes to an A-to-D converter on the A27 Level Control board. The attenuator setting is digitally subtracted from the A-to-D output and the result displayed on the front panel power dBm display. When internally leveled and AM is OFF, the POWER dBm display simply displays the number in the ENTRY DISPLAY. The level A-to-D circuitry is used whenever the actual output power may be expected to differ from the level entry. These conditions are:

- Unleveled light ON (instrument cannot put out as much power as is requested. The meter displays the actual output.)
- AM ON (User may put DC into AM input, changing output power.) The x6.6 amplifier contains a 5Hz, active low pass

filter, preventing the level meter from flickering for AM rates above 20 Hz.

- External leveling selected. (Actual output is a function of the user's detector, coupler, RF hardware, etc.)

The output voltage of the logger has a temperature dependence due to its kT/q term. Thus, for constant RF power, the logger output voltage is directly proportional to absolute temperature. (This effect is separate from the detector's temperature drift which is compensated by the thermistor.) To maintain the accuracy of the level meter, the gain of the x6.6 amplifier is made to vary inversely with absolute temperature. This is accomplished by using an input resistor with a temperature coefficient of +3400 ppm/degrees C. For the same reason, the ALC reference voltage must be made to increase with temperature at +3400 ppm/degree C so that with constant output power, the logger voltage will track the reference. As long as they track over temperature, the loop will not try to change the power. To accomplish this, the reference voltage from the A27 Level Control board is routed through an inverting amplifier on the A25 ALC Detector board whose gain is proportional to absolute temperature. The output of this amplifier goes to the A26 Linear Modulator board where it is fed to the loop summing point. Placing the temperature compensating amplifier on the detector board improves thermal tracking with the logger.

The remaining circuitry on the detector board is for external leveling. The 8340A may use either positive or negative polarity external detectors. The external input goes to an "Absolute Value" circuit which inverts positive inputs but not negative ones. The output of the absolute value circuit drives the external logger. This logger has no special compensation for detector T.C. or square law deviation. Its own inherent temperature drift is compensated by the drifting reference voltage, as for internal leveling. The logger output is amplified by a factor of 5 to 30 mV/dB.

A25 FET switches select either the output of the internal or external circuits to send to the A26 Linear Modulator board. When external meter leveling is selected, a crossover network is used to help stabilize the loop. Frequencies from DC to about 0.7 Hz may pass from the external input to the modulator board. Above 0.7 Hz, the external input is rolled off, and the loop is closed through the internal detector. In this way, the loop stability is maintained with a wide variety of meter bandwidths.

The external AM input goes to the AM logger on the A26 Linear Modulator board. The output of the logger is amplified by a factor of 10 to 30 mV/dB. This signal is summed into the loop at

the same point as the reference, causing the loop to change the RF output power accordingly. Since the detector logger has shaped the detector voltage to be linear in terms of decibels, the AM input provides very linear control.

The logged detector voltage, temperature compensated reference voltage, marker signal, and logged AM input are all summed together at the loop summing point. That point feeds the input of an integrator through a FET switch (integrate/hold gate). That switch is normally closed. If it is opened, as between pulses during pulse modulation, the input to the integrator is zero, causing its output to remain constant, thus holding the modulator drive at a constant level. The integrator controls the bandwidth of the leveling loop. The integrator gain is proportional to 1/FC, causing gain crossover to occur at F = 130 kHz for C = 1000 pF, and F = 6 kHz for C = 0.023 uF. The capacitor is selected by a FET switch. The loop is normally in its low bandwidth state, being switched to high bandwidth if sweep times are <5 sec, if AM is ON with pulse mode OFF, or if "shift AM" is ON with pulse mode ON.

The integrator output drives an exponential current source

$$I_{out} = I_{in} \times e^{I_{in}/0.1mA}$$

For Iout above 1mA (normal operation), this is a close approximation to an exponential. An exponential modulator drive helps keep loop gain constant as the power level is changed. The input to the current source is controlled by 5 loop gain adjustments selected according to the RF band in use (Bands 0 through 4). The YTM transfer function increases loop gain on its multiplying bands so separate adjustments are necessary. At the output of the current source, an appropriate offset current is subtracted, biasing the current source for a straight line modulator characteristic. The output current is sent to either the Band 0 or Bands 1 through 4 modulator by a pair of FET switches.

When the integrator output is at 0 volts, the modulator will be close to full output. When the loop gain is properly set, the modulator output will decrease at the rate of approximately 30 dB/volt. If increased output power is needed, the integrator moves positive. If more power is needed than the instrument can provide, the integrator will go more positive than the "full on" voltage. At this point, the feedback loop is open, and the integrator will try to saturate in a positive direction. A clamp circuit is activated at approximately +.7V, which dumps current into the integrator input preventing the output from going more positive. Preventing the integrator from saturating greatly speeds recovery time. When the integrator output moves above +.2V, a comparator is tripped which lights the front panel UNLEVELED annunciator. The overmod comparator trips for voltages more negative than -3.5V (OVERMOD annunciator), and another clamp is activated at -3.7V.

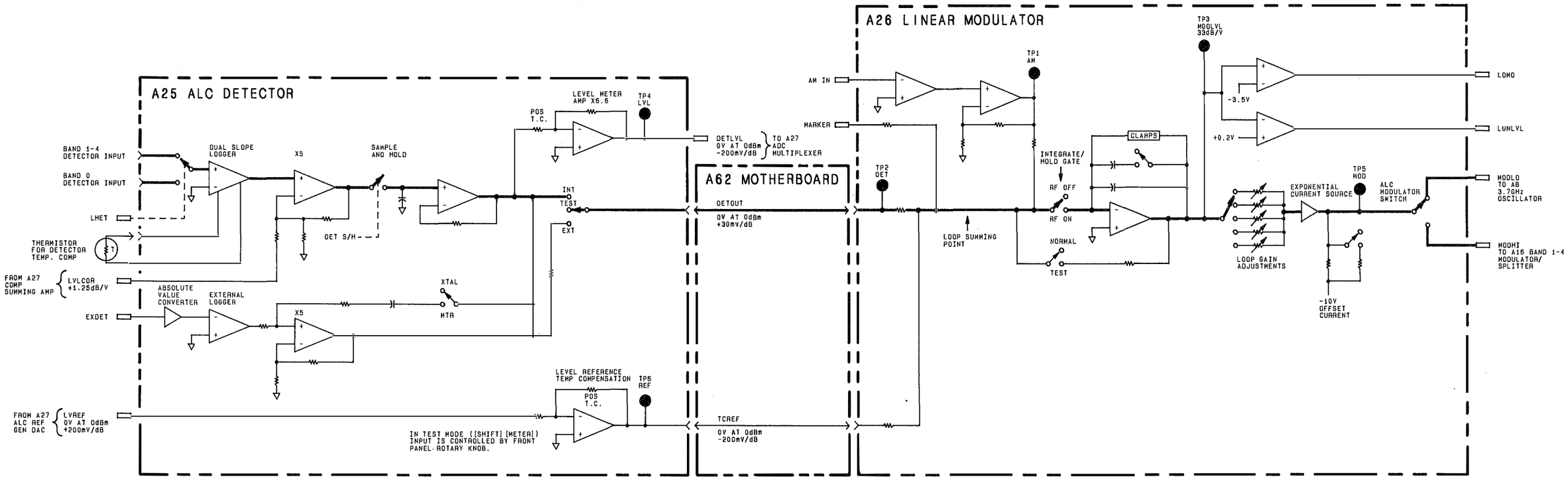


Figure 8I-5. ALC Loop, Detailed Block Diagram

When RF is turned OFF during RF blanking, both the pulse modulator and linear modulator are shut down. The linear modulator is used to provide a controlled RF turn-on with no overshoot. This does not happen during pulse modulation because the RF is not OFF long enough (10 msec. max) for the Sample and Hold circuits to drift. Also, during external leveling, a slow detector would cause turn-on overshoot if the RF were not brought up slowly. The RF ON/OFF control (HRFON) is fed to the clamp circuits in such a way as to force the integrator output to -3.0V. Note that this will not trip either comparator. When RF is turned ON, the voltage rises at the charge rate of the integrator. If external power meter leveling is selected, a capacitor is switched into the RF ON/OFF circuit slowing the turn-on to two seconds.

ALC Loop Troubleshooting

For troubleshooting purposes, the ALC Loop may be broken and a signal injected to be traced around the loop. When this mode is activated by pressing **[SHIFT] [METER]**, the FET switches will be switched to break the connection from the A25 ALC Detector board to the A26 Linear Modulator board (See Figure 8I-37, "A26 ALC Modulator, Schematic Diagram", Block **B**). A resistor (A26R17) is switched across the integrator capacitor on the A26 Linear Modulator assembly converting this stage to an inverting amplifier. Thus, the integrator output may be controlled via the reference DAC. The signal may then be traced from there to the modulator driver, RF output, detector output, logger output, x5 amp, through the Sample and Hold, level amp, and to the A-to-D driving the level meter. By putting a detector on the RF output, the external leveling circuits may be checked. The AM signal path is the only one left unchecked.

To enter the test mode, press **[INSTR PRESET]**, **[CW]**, and **[SHIFT] [METER]**. The UNLEVELED annunciator should be ON. The POWER dBm display should indicate the approximate RF output power. The ENTRY DISPLAY should indicate "ATN: -00, MOD: 0.0 dB". The modulators are being controlled by the voltage at A26TP3 (MODLVL). This voltage is programmed by the ALC Reference Generator DAC on the A27 Level Control assembly. The DAC can be controlled using the RPG. Rotate the RPG CCW and note that the ENTRY DISPLAY MOD level changes. Continue turning the RPG CCW until the Power dBm display begins to change. The absolute MOD level indication is not important, however, a further decrease in MOD level should generate a corresponding decrease in the Power dBm display and the RF output power (i.e., 10 dB MOD level change should generate 10 dB ±3dB power change). A defective circuit can be isolated by tracing the voltage from A26TP3 to the modulators or by tracing the RF path from the YO to the Level Meter Amplifier on the A25 ALC Detector assembly. The AM signal path must be checked separately.

SYTM RELATED ASSEMBLIES

Introduction

The two boards that directly provide control circuitry for the SYTM are the A28 SYTM Driver and the A24 Attenuator Driver/SRD Bias Board.

A28 SYTM Driver

The SYTM passband must track the appropriate harmonic of YO frequency to an accuracy on the order of 0.1% without the benefit of feedback. The main function of the A28 SYTM Driver is to tune the center of the SYTM passband to the correct frequency for Bands 1-4 by varying the magnetic field through the YIG sphere. The magnetic field is proportional to the current through the SYTM coil with a sensitivity on the order of 15 mA/GHz. The current is generated from the PRETUNE signal (-2.5 V/GHz YO frequency) from the A54 YO Pretune DAC/Delay Compensation Board and the latched band information from the A27 Level Control Board. In order to adequately track the correct harmonic of Y0 frequency, the SYTM Driver contains circuitry that adds corrections to the SYTM tuning current accounting for the effects of the nonlinear tuning curve, past magnetic history, and magnetic delay.

NONLINEAR TUNING CURVE COMPENSATION

The circuitry on the SYTM Driver contains three breakpoint adjustments to correct for the nonlinearities in the SYTM tuning curve. Two of the breakpoints are fixed in frequency but variable in magnitude of effect. The third breakpoint is variable over a limited range of frequency operation as well as in magnitude of effect.

PAST MAGNETIC HISTORY COMPENSATION

A series of kick pulses are summed into the SYTM tuning current at appropriate times to minimize the effects of past magnetic history. The kick pulses drive the SYTM magnetic field both above and below the normal tuning range.

MAGNETIC DELAY COMPENSATION

The SYTM magnet doesn't repsond fast enough to track the correct frequency when the current drive is changed rapidly. This presents an increasingly severe delay problem as the 8340A sweep rate is increased. To compensate for the slow response of the

SYTM, the delay compensation current is added to the SYTM tuning current that is a function of sweep rate and change in frequency from the start of sweep.

A24 Attenuator Driver/SRD Bias Board

Three SYTM functions are controlled by the A24 Attenuator Driver/SRD Bias Board. These are Step Recovery Diode bias, PIN Switch driver, and YIG sphere temperature control.

STEP RECOVERY DIODE BIAS

In Band 1 the step recovery diode (SRD) is forward biased with a negative voltage. The conversion efficiency of the SYTM in Bands 2, 3, and 4 is related to the DC bias voltage on the SRD. The proper biasing of the step recovery diode is also necessary to avoid squegging. To maintain optimum SRD bias for Bands 2, 3, and 4 the bias voltage is generated as a function of both frequency and power level. The variation of the SRD bias voltage with frequency is derived from BPRETUNE (a voltage from the A28 SYTM Driver that is proportional to the YO frequency). The SRD bias is adjusted for power level correction using SRD bias control from the A26 Linear Modulator Board (a voltage corresponding to the modulator voltage).

PIN SWITCH

In Band 0 the Band 0 RF input is allowed to pass unattenuated through the SYTM and the YIG sphere is tuned by the A28 SYTM Driver to a fixed non-interfering frequency. In Bands 1-4 the SYTM Driver provides a tuning current as previously described while the Band 0 RF input port to the SYTM is grounded to keep it from interfering with the desired Band 1-4 RF output. The process of selectively grounding the Band 0 RF signal is facilitated by the PIN Diode Switch in the SYTM. The PIN Diode Switch driver is located on the Attenuator Driver/SRD Bias Board.

YIG SPHERE TEMPERATURE CONTROL

The YIG sphere temperature control is required because the SYTM passband will drift if the temperature varies. The SYTM sphere temperature is held constant using heater resistors and a thermistor located on the SYTM substrate and the heater drive circuitry located on the Attenuator Driver/SRD Bias Board.

SYTM Peaking

SYTM Peaking is a function designed to tune the SYTM such that the RF signal (YO frequency or multiple of the YO frequency) is

in the center of the SYTM 1 dB passband insuring that maximum RF power is available.

The peaking routine is stored in ROM and can be accessed manually by pressing the front panel PEAK button or remotely by a "RP1" instruction. An "RP0" instruction will remotely turn OFF the peaking function. The peaking routine when accessed in this manner will execute only if the 8340A is in CW or MANUAL mode and if the RF is ON.

By manually pressing SHIFT AMPT MKR or remotely programming "SH AK", the peaking function will execute immediately even if not in the CW or MANUAL mode; however, only a fine search around the most recent slope DAC (A28U24) setting will be done. Since the SYTM passband is not tuned to track the output frequency in Band 0 (heterodyne band) the peaking routine will not execute if Band 0 is selected.

The ALC detector monitors the RF output level. The detected level is routed to the A25 ALC Detector Board. The DETOUT output (A25P1 Pin 32) is fed to the A26 ALC Modulator (A26P1 Pin 10). The MOD LVL (A26P1 Pin 32) is then fed to the A27 Level Control Board (A27P1 Pin 61) where it becomes one input to the ADC Input Multiplexer. The peak routine programs the ADC Multiplexer to route the MOD LVL voltage to the Test ADC. By monitoring the Test ADC output while tuning the SYTM the program can find the peak RF signal level.

The SYTM is tuned by varying the slope DAC setting. When the peak function is activated on the front panel, the 8340A will do a full peak (i.e.,coarse and fine search) if in CW or MANUAL. If the peak function is left ON, the 8340A will repeak every 7 minutes doing only a fine search around the most recent slope DAC setting. If the CW or MANUAL frequency is changed while peaking is ON using the RPG a fine search around the most recent slope DAC setting will be done; however, if the CW or MANUAL frequency is changed using the step keys or numerical entry keys, a full peak will be done.

The MOD LVL voltage is offset and scaled so that the 10 volt input range of the ADC covers MOD LVL voltages between -3.53 V to +2.47 V. The input range is equivalent to about 6 mV/bit. The sensitivity of the MOD LVL line is around 20 to 50 mV/dB so the ADC has a sensitivity of about 0.2 dB/bit.

The SYTM passband has a second narrower peak that is located 200-300 MHz lower in frequency than the desired peak. The coarse search routine starts at the top of the passband and searches for a peak in 15 MHz steps. Once a peak is found the coarse search continues for another 150 MHz to verify that the correct peak is

found and stops before the second peak is reached. 15 MHz was chosen for the step size because the minimum 1 dB bandwidth is 24 MHz so at least one of the steps will fall within 1 dB of the peak. Once the coarse search peak is located, the processor takes a reading of the modulator level to be used as a reference for the -1 dB points. The level control DAC (A27U14) is then stepped down 1 dB which causes the modulator level to drop 1 dB (since the ALC loop must generate the 1 dB change). The processor then uses the -1 dB reference and steps the slope DAC up until the modulator level is equal to or less than the -1 dB reference level. The slope DAC is then stepped down from the peak until the same reference threshold is reached. If the slope DAC goes out of range before the -1 dB reference level is reached, the routine searches the other side of the passband to the same modulator threshold present when the slope DAC reached the end of its range. The slope DAC is then set to the midpoint of the two values it had when the reference level was reached and the original power is restored. The setting for the slope DAC can be accessed by doing an IO read from subchannel 10.

Peaking is done at the current ALC power level because the SYTM passband may vary with power level. In the fundamental band, the YIG sphere in the SYTM may squeg if too much power is applied. To prevent this from interfering with peaking, the maximum ALC power setting (in the fundamental band only) is 0 dBm during the coarse search and +10 dBm for the fine search. Once the peaking is completed, the original power is restored.

When the instrument goes unleveled, the current driving the ALC modulator is turned off to give maximum available power. However, the MODLVL line has a soft clamp that still gives an indication of the detected power out of the SYTM with a sensitivity of 30 mV/dB. The absolute voltage level shifts by about 1 volt when the instrument goes unleveled but the incremental level remains valid. The absolute level shift poses no problem to the peaking routine since the peaking routine uses incremental changes.

SYTM tracking is accomplished by pressing **[SHIFT] [PEAK]** on the front panel or by remotely programming "SH RP" over the HP-IB bus. SYTM tracking updates calibration constants 9 through 12 and 50 through 52 to the best value for the SYTM tracking in each band. Each band is tracked independently of the other bands. To track a band, a single band sweep is set up and the sweep is stopped at several points across the band that each sweep is peaked. The number stored in the calibration constant represents the least squares fit to the slope DAC numbers returned from the peaking routine with the lowest power point receiving a double weighting. If the least squares number is out of the range of the slope DAC, the fault light is turned ON with the TRK indicator flashing when **[SHIFT] [MANUAL]** is pressed. In Band 1, the SYTM is

peaked at 2.3 GHz and at one GHz steps from 3 GHz to 7 GHz. In Band 2 the SYTM is peaked at 6.9 GHz and at one GHz steps from 7.5 to 13.5 GHz. In Band 3, the SYTM is peaked at 13.4 GHz and at one GHz steps from 14 GHz to 20 GHz. In Band 4, the SYTM is peaked at 19.8 GHz and at one GHz steps from 20.5 GHz to 26.5 GHz.

SYTM PEAKING TROUBLESHOOTING

If the FAULT annunciator comes ON the function that caused a fault can be determined by pressing the **[SHIFT]** key and then the **[MANUAL SWEEP]** key. If the peak indicator is flashing, it means that the peaking routine failed to find a peak within the range of the SYTM slope DAC. This can be caused by several different problems: the SYTM driver may not be shifting the passband, there may not be enough power out of the SYTM for proper ALC operation, the ALC modulator or the ADC might be defective. Looking at the CMP test point on the A28 SYTM Driver board will give an indication of how the slope DAC is varying slope compensation. This trace can be compared with the A-to-D IN test point on the A27 Level Control board to see if the A-to-D input is within reasonable limits. If the voltage on the A-to-D input doesn't trace out a passband as the slope DAC is varied, check the MODLVL test point on the A26 Linear Modulator board. The A-to-D IN test point should be a scaled version of the voltage at the MODLVL test point. If the fault is due to peaking, the fault light may be cleared by pressing the **[INSTR PRESET]** key or by turning the line power OFF and ON.

PULSE MODULATION ASSEMBLIES

Pulse modulation in the 8430 is produced by the A21 Pulse Modulator Driver Board driving one of the two pulse modulators in the instrument. The "Pulse Modulation Input" on the front panel of the 8340A is a TTL compatible input. A LOW signal on this input turns the RF OFF and a HIGH TTL signal turns the RF ON. With no connection, the Pulse Modulation Input is internally pulled up to a TTL HIGH level.

When a LOW signal is present on the pulse Modulation Input the A21 Pulse Modulator Driver PC Board delivers 20 mA to one of two pulse modulators. An output multiplexer on the A21 Driver Board directs the 20 mA modulator current to the A9 Band 0 Pulse Modulator when the 8340A is in Band 0 or the pulse modulator in the A16 Mod/Splitter when operating in Bands 1 through 4.

The leveled pulse modulation capability of the 8340A requires timing signals to be sent to the ALC assemblies. The timing signals coordinate the leveling operation with the pulse operation. Three timing signals are generated on the A21 Pulse Modulator Driver Board when a pulse is initiated. These are the Sample/Hold timing, the Analog to Digital Converter (ADC) timing, and the Integrator timing.

The Sample/Hold timing signal controls the sample/hold gate on the A25 Detector Board. This signal is adjusted to close the gate (sample) when the RF pulse is ON and open the gate (hold) when the RF is OFF. The Sample/Hold output voltage represents the peak RF amplitude.

The ADC timing enables the analog-to-digital converter on the A27 Level Control Board to monitor the output of the Sample/Hold. The ADC is enabled when the RF is ON, and for 1 msec after the RF is turned OFF. After 1 msec, droop renders the Sample/Hold voltage inaccurate.

The Integrator timing controls the Integrate and Hold gate on the A26 Modulator Board. This gate is closed when the RF is ON and stable. To speed response time for narrow pulses the gate is held closed for a minimum of 10 usec. In fast response mode **[SHIFT] [AM]** the gate is held closed for a minimum of 1 usec. The Sample/Hold maintains a valid integrator input after the pulse is turned OFF.

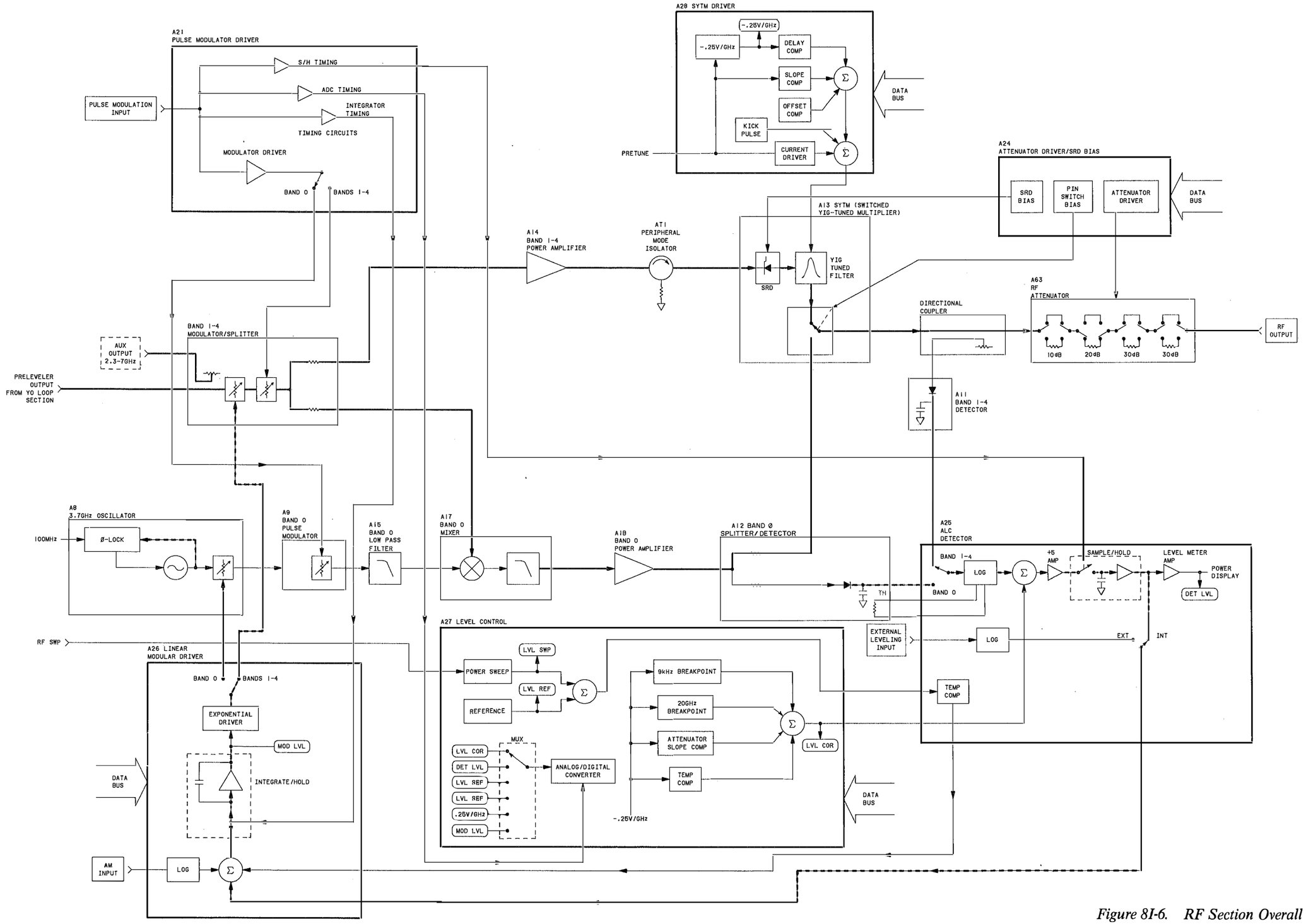


Figure 8I-6. RF Section Overall Block Diagram

TROUBLESHOOTING TO ASSEMBLY LEVEL

For ALC problems, refer to ALC Troubleshooting under ALC Loop Assemblies. For SYTM problems, refer to SYTM Troubleshooting under SYTM Related Assemblies.

For a troubleshooting block diagram, refer to Figure 8I-42, "RF Section Schematic Diagram", at the end of the RF Section documentation.

For other RF associated problems, refer to the **"OVERALL TROUBLESHOOTING PROCEDURE"** located in the **"SERVICE INTRODUCTION"** (beginning of Section 8).

REPAIR PROCEDURES

INTRODUCTION

This section contains: information on the Module Exchange Program; complete removal/installation procedures for all RF assemblies.

WARNING

Read all warnings and cautions in the "REPAIR PROCEDURES" chapter in the "SERVICE INTRODUCTION". The "SERVICE INTRODUCTION" is located in the beginning of Section VIII.

MODULE EXCHANGE PROGRAM

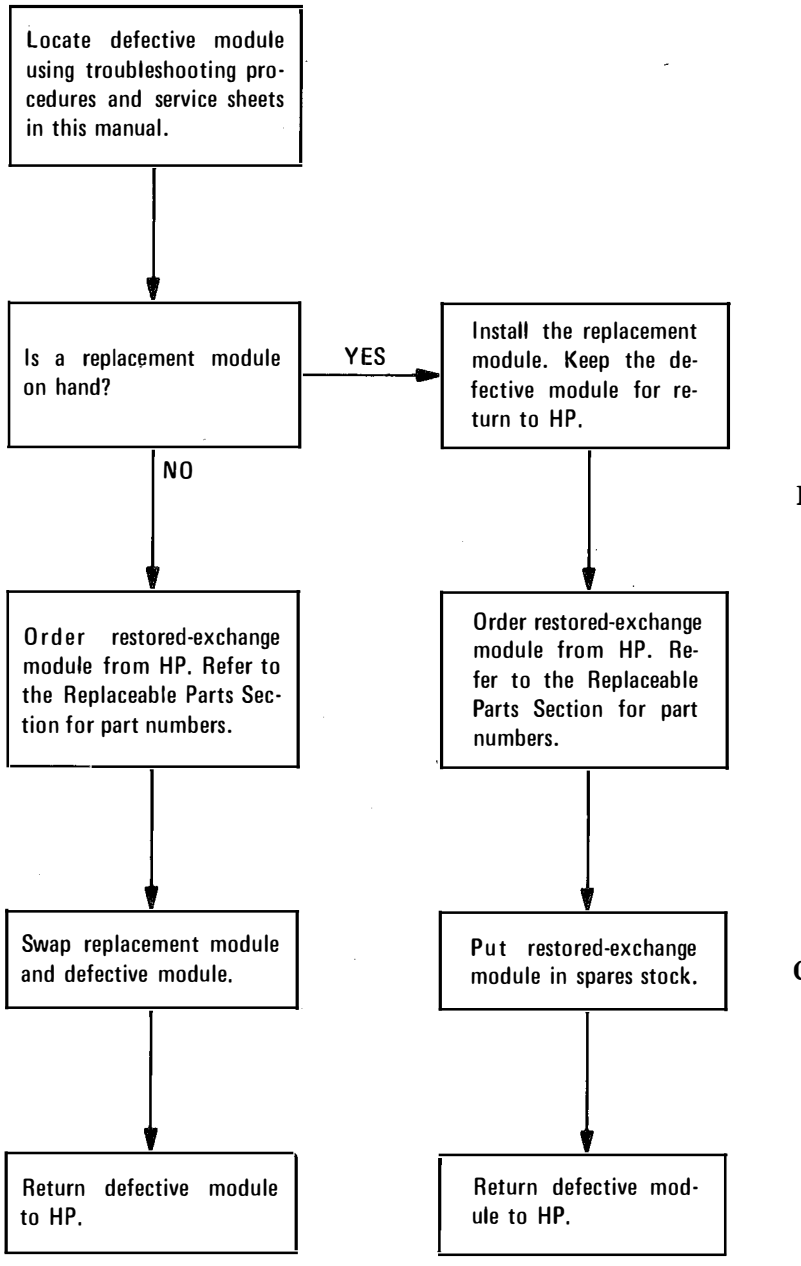
The A8 through A18, A63, and AT1 assemblies are not field repairable. Of these, the A8, A9, A13, A14, A16, A17, and A18 assemblies are available at a reduced cost through the module exchange program. This instrument may be repaired by replacing a defective module with a restored - exchanged module. To support the module repair concept, Hewlett-Packard has set up a module exchange program.

The procedure for using the module exchange program is given in Figure 8I-7, "Module Exchange Procedure". When you locate the defective module, order a replacement module through the nearest Hewlett-Packard sales office. The restored exchange module will be sent immediately, directly from a customer service replacement parts center. When you receive the exchange module, return the defective module in the same special carton in which the exchange module was received. DO NOT return a defective module to Hewlett-Packard until you receive the exchange module.

If you are not going to return the defective module to Hewlett-Packard, or if you are ordering a module for spare parts stock, etc., order a new module using the new module part number listed in Table 6-3.

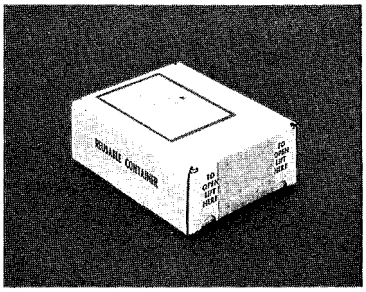
The Hewlett-Packard module exchange program allows you to obtain a fully tested and quaranteed restored - exchange module at a reduced price. (The reduced price is contingent upon return of the defective module to Hewlett-Packard.) Assemblies available for module exchange are listed in Table 6-1.

The module exchange program described here is a fast, efficient, economical method of keeping your Hewlett-Packard instrument in service.



*HP pays postage on boxes mailed in U.S.A.

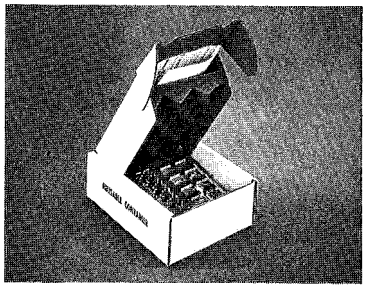
A.



Restored-exchange modules are shipped individually in boxes like this. In addition to the circuit module, the box contains:

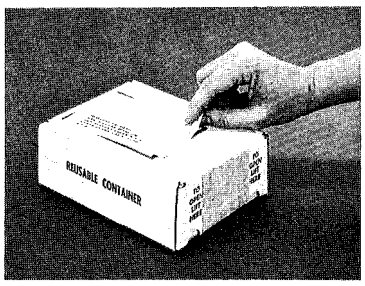
Module repair report
Return address label
Tape for resealing box

B.



Open box carefully - it will be used to return defective module to HP. Complete repair report. Place it and defective module in box. Be sure to remove enclosed return address label.

C.



Seal box with tape provided. Inside U.S.A.*, stick preprinted return address label over label already on box, and return box to HP. Outside U.S.A., do not use address label: instead, address box to the nearest HP office.

Figure 8I-7. Module Exchange Procedure

RF ASSEMBLIES REMOVAL AND INSTALLATION PROCEDURES

Equipment Required	HP Part Number
Large Pozidriv	8710-0900
Small Pozidriv	8710-0899
5/16 Wrench	8720-0015
Offset Pozidriv (A16 assembly only)	8710-0949
1/4 inch Nut Driver (A8 and A9 assy's only)	8720-0002
5/16 Special Wrench (A8 and A15 assy's only)	08555-20097
7/32 Wrench (A15 assembly only)	8710-0534

Introduction

The following procedures can be divided into two main categories: The first category is made up of the assemblies that require only the removal of attached cables or wires and the appropriate mounting hardware. The second category consists of assemblies that require the opening of a hinged "RF Deck" in order to access either the whole assembly or part of the mounting hardware.

NOTE

Before performing any of the following procedures it is necessary to: Remove the top, bottom, and perforated (right hand) side covers. Place the instrument on its left side (as viewed from the front).

A8 3.7 GHz Oscillator Replacement Procedure

Refer to Figure 8I-8, "RF Assemblies, Cables, Mounting Hardware Location", for related assemblies, cables, and mounting hardware location.

Remove all cables and wires from both the A8 and A9 assemblies:

Remove W10 from the instrument. To accomplish this it may be necessary to place a special 5/16 inch "slotted box end wrench" (HP Part Number 08555-20097) on A15J2 to keep the A15 assembly from turning when W10 is removed from A15J1. A standard 5/16 inch wrench is used to remove W10 From A15J1. Remove W10 from the A9 assembly and set aside.

Remove W25 from A62J10 (item 1). Remove the five screws (item 2) that hold on the combined A8 and A9 assemblies to the RF Deck. Remove one screw (item 3) that holds the A8 casting to the A62 Motherboard. Note that this screw (item 3) is longer than the five

other screws (item 2).

Carefully remove the A8/A9 assembly from the instrument. Remove W9 completely. When loosening W9 from A9J1 be careful not to damage the -10V terminal on the A8 assembly with the wrench. Use a 1/4 inch nut driver to separate the A8 assembly from the A9 assembly by removing the four nuts located in the corners of A9 assembly.

To re-install the new A8 assembly reverse the above procedure. When re-installing W10, completely tighten one end before starting the other.

A9 Band 0 Pulse Mod Replacement Procedure

Refer to Figure 8I-8, "RF Assemblies, Cables, Mounting Hardware Location", for related assemblies, cables and mounting hardware location.

Remove all cables from the A9 assembly.

Remove W10 from the instrument. To accomplish this it may be necessary to place a special 5/16 inch "slotted box end wrench" (HP Part Number 08555-20097) on A15J2 to keep the A15 assembly from turning when W10 is removed from A15J1. A standard 5/16 inch wrench is used to remove W10 From A15J1. Remove W10 from the A9 assembly and set aside.

Disconnect W9 from the A9 assembly by first loosening W9's A8J1 connector. When removing W9's A9J1 connector be careful not to damage the -10V terminal on the A8 assembly.

To install a new A9 assembly reverse the above procedure.

A10 Directional Coupler/A12 Band 0 Detector Replacement Procedure

CAUTION

A10J1, A10J2, and A10J3 are precision APC 3.5 mm connectors. The cables and A11 Band 1-4 Detector assembly that connect to them use SMA connectors. Extreme care should be taken when disconnecting or connecting an SMA cable from a mating 3.5 mm connector. The SMA cable center conductor must align with the 3.5 mm connector center conductor. If there is any axial force on the cable when disconnecting the SMA fitting, the 3.5 mm connector center conductor may be

damaged, necessitating the replacement of the A10 Directional coupler. Remove any axial force on the cable by first disconnecting the end of the cable that does not mate with a 3.5 mm connector or by removing the mounting screws of the device having 3.5 mm connectors. Perform both safeguards where possible. The A10J2 - A11J1 connection is not as critical because the A11J1 connector has a captured nut. This nut does not allow axial force on the APC 3.5 mm center conductor until well after the SMA center conductor is disengaged.

To remove the A12 assembly, perform step A. To remove the A10 assembly, perform both step A and B.

A. Refer to Figure 8I-8, View C (top of instrument). W13 is shown on the right-hand side of the figure. Disconnect W13 from the A18 assembly. Now look at Figure 8I-8, View B, which shows a portion of the bottom of the instrument. Disconnect W14 and W26 from the A12 assembly. Use a small Pozidriv to remove the two screws that hold on the A12 assembly (Item 13). Carefully remove the A12 assembly, with W13 still attached. If the A12 assembly must be removed, disconnect W13 and de-solder the three wires attached to it. Reverse the above procedure for re-installing the new A12 assembly.

B. Refer to Figure 8H-4, "Front Panel Disassembly", in the **FRONT PANEL - REAR PANEL** functional group. Remove the front panel according to the instructions given in steps 1 though 7. It is not necessary to remove the ribbon cables.

Remove the two screws (item 6) that hold in the A10/A12 assembly mounting bracket.

Remove the A11 Band 1-4 Detector assembly from A10J2.

Remove the W16 cable from the A13 SYTM assembly. Carefully remove the other end of W16 from the precision 3.5 mm A10J1 connector. Carefully remove the cable from the A10J3 connector (near the front panel). Use extreme care to avoid axial force on the cable.

Pull the A10/A12 mounting bracket out far enough to access the screws that hold the A10 assembly in place. Remove the screws that hold the A10 assembly.

To reinstall the new assembly, reverse the above procedure. The cable going to A10J3 is accessible through the front of the instrument (with the front panel removed).

Reassemble the front panel.

A13 Band 0-4 SYTM Replacement Procedure

Refer to Figure 8I-8, "RF Assemblies, Cables, Mounting Hardware Location", and Figure 8I-9, "A13, A16, A18, and AT1 Assembly, Cable, Mounting Hardware Location".

Open the hinged RF Deck assembly by following the "HINGED RF DECK ACCESS PROCEDURE". This procedure is located just after these disassembly procedures.

NOTE:

When removing the ribbon cable from A13A1 (See Below), be sure to note its proper orientation. Putting this cable on backwards causes all power supplies to shut down.

Remove W8 from AT1J2. Remove the ribbon connector (W33) from A13A1J1 by gently prying it up with a small, flat tool. Be careful to note the original orientation of this ribbon connector. Re-installing it backwards will cause all of the power supplies to shut down. Do not pull it off by hand as this may result in badly bent pins. Disconnect W8 from A13J1 and remove it completely from the instrument. Be careful not to bend the small terminals on the A13A1 PC Board with the wrench.

Completely remove W14 connecting A13J2 to A12J2.

While holding the A13 assembly, remove the two screws (item 8) shown in Figure 8I-9.

The A13 assembly is now free. When replacing it apply a thin but continuous layer of thermal compound (HP Part Number 6040-0454 CD0) to each side of the A13MP1 aluminum spacer that goes between the SYTM and the RF Deck.

CAUTION

Use only oil based thermal compound. The use of silicone based thermal compound

may cause serious reliability problems. Silicone based oil migrates to pass element sockets, switch contacts, or printed circuit board edge connectors. The compound then tends to raise contact resistance or electrically isolate the contacts. Silicone based thermal compounds disperse into the air and deposit themselves anywhere in the instrument. Applying this material to a warm component (e.g. a heat sink or pass element) increases the rate of dispersion.

AT1 Replacement Procedure

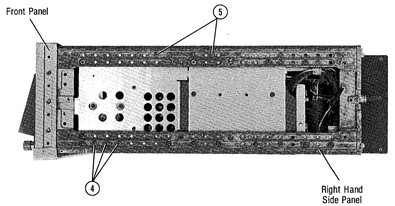
Refer to Figure 8I-8, "RF Assemblies, Cables, Mounting Hardware Location", View D, for related assemblies, cables, and mounting hardware location. Refer to the "HINGED RF DECK ACCESS PROCEDURE".

Remove W7 and W8 from the AT1 assembly.

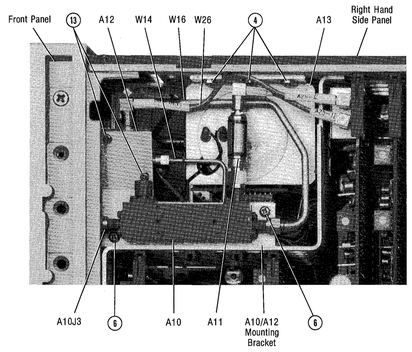
Remove the four screws shown in Figure 8I-8, View D. When removing the last screw, hold the AT1 assembly. Make sure W7 and W8 are clear of AT1J1 and AT1J2 when removing the AT1 assembly.

To replace, reverse the above procedure.

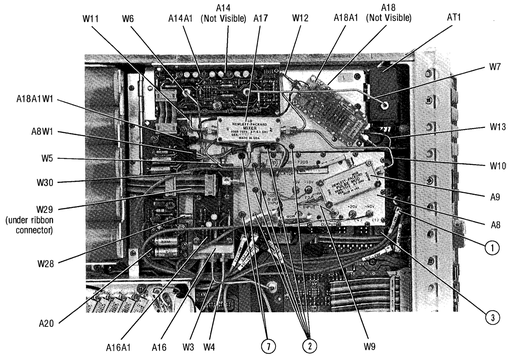
VIEW A



VIEW B



VIEW C



VIEW D

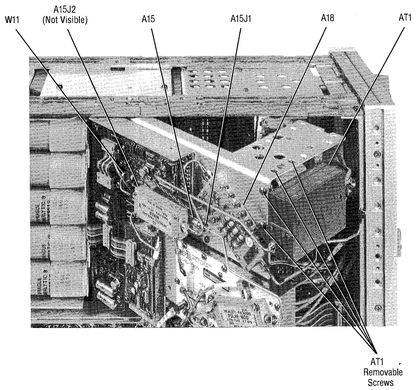


Figure 8I-8. RF Assemblies, Cables, Mounting Hardware Location

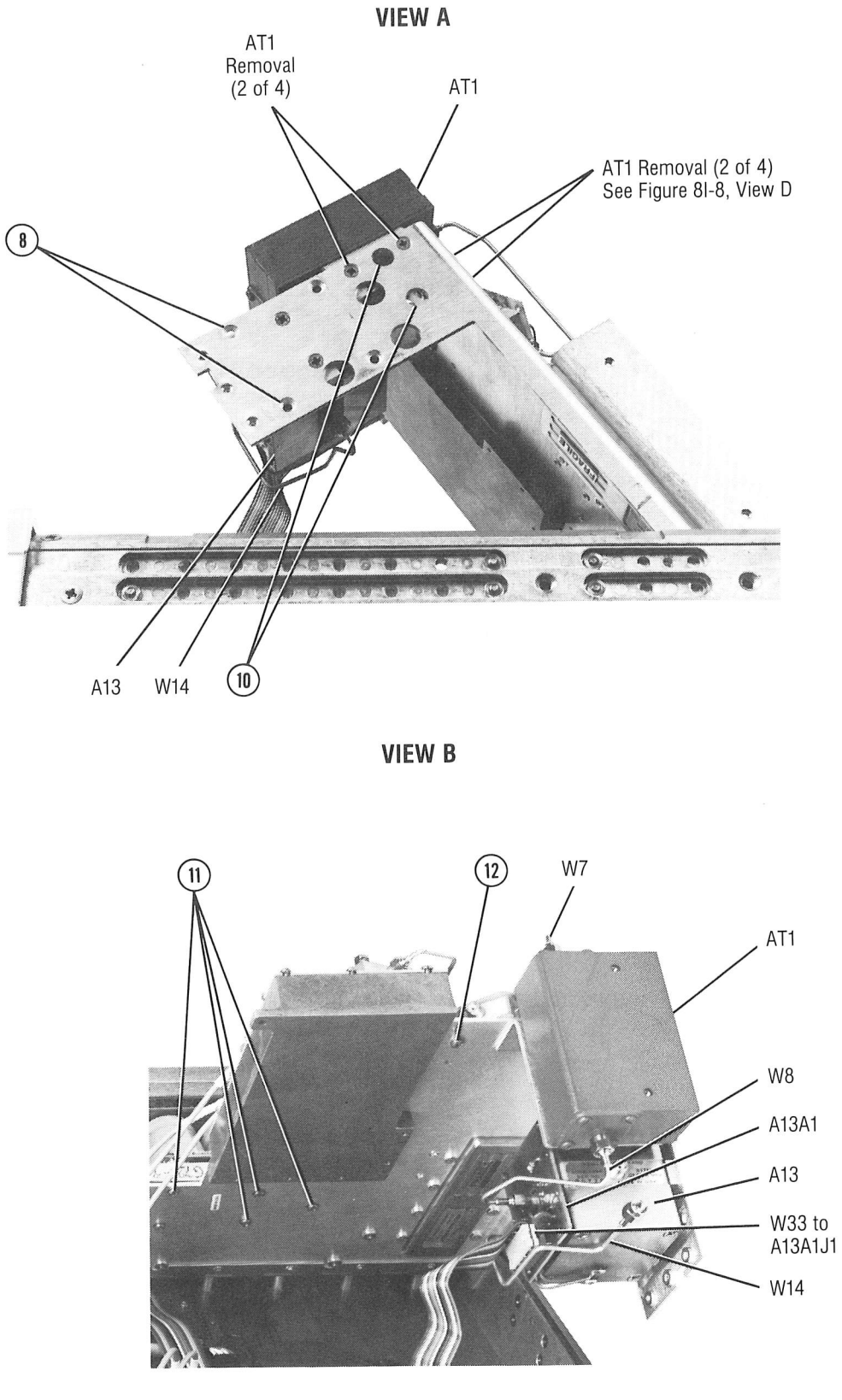


Figure 8I-9. A13, A13A1, A16, A18, and AT1, Asssemblies, Cables, and Mounting Hardware Location

A14/A14A1 Band 1-4 Power Amplifier Replacement Procedure

Refer to Figure 8I-8, "RF Assemblies, Cables, Mounting Hardware Location".

Remove the ribbon cable going to A14A1. Completely remove W7 from the instrument.

Remove W6 by first disconnecting it from A14. To disconnect W6 from A16, five-conductor A8W1 must be disconnected. Completely remove W6 from the instrument.

Remove the eight screws that hold the composite A14-A14A1 assembly together.

To install the new A14-A14A1 assembly, reverse the above procedure. When reconnecting the ribbon connector, be extremely careful not to bend the pins.

A15 Band 0 Low Pass Filter Replacement Procedure

Refer to Figure 8I-8, "RF Assemblies, Cables, Mounting Hardware Location".

Follow the procedure for the removal of the A20 assembly.

Remove the W10 connector from the A15 assembly.

Slide the A15 assembly to the left until the portion with flat sides is accessible. Remove W11 from A15 by placing a 5/16 inch wrench on the W11 connector and a 7/32 inch wrench on A15's flat section.

The A15 assembly may now be removed.

To replace the A15 assembly, reverse the above procedure.

NOTE

When tightening W10 to A15 do not tighten so hard that W10 is stressed.

A16 Band 0-4 Modulator/Splitter Replacement Procedure

Refer to Figure 8I-8, "RF Assemblies, Cables, Mounting Hardware Location", and Figure 8I-9, "A13, A16, A18, A18A2, and AT1 Assembly, Cable, Mounting Hardware Location".

Disconnect the ribbon connector from A16A1.

Remove the 5 contact A8W1 and 2 contact A18A1W1 connectors from the A20 assembly.

Disconnect W5, W6, W28, and W29 from the A16 assembly.

Perform the "HINGED RF DECK ACCESS PROCEDURE".

Using an offset posidrive, remove the five A16 mounting screws on the back of the RF Deck. Refer to item 11, Figure 8I-9, View B.

Pull the A16 assembly out far enough to access cables W28 and W29. Remove these cables by gently and carefully prying them upward with a small, flat implement.

The entire A16/A16A1 assembly is now free. Transfer the cable (W30) that interconnects A16 and A16A1 to the new A16/A16A1 assy. and reverse the above procedure to re-install.

A17 Band 0 Mixer Replacement Procedure

Refer to Figure 8I-8, "RF Assemblies, Cables, Mounting Hardware Location".

(1.) Remove the four screws located in each corner.

(2.) Disconnect the 3 cables going to the A17 assembly.

(3.) The A17 assembly is now free.

A18/A18A1 Band 0 Power Amplifier/Replacement Procedure

Refer to Figure 8I-8, "RF Assemblies, Cables, Mounting Hardware Location".

Perform the "HINGED RF DECK ACCESS PROCEDURE".

Remove the two screws (item 12) on the back of the RF Deck that hold this assembly in place.

Remove the cables that go to the A18 assembly.

The A18/A18A1 assembly is now free.

A20 RF Section Filter Replacement Procedure

Refer to Figure 8I-8, "RF Assemblies, Cables, Mounting Hardware Location".

Remove all connectors from the P.C. Board. One of the ribbon connectors goes to the A16A1 assembly as well as the A20 assembly and must also be removed from there.

Remove the four screws that hold the P.C. Board in place. (These are on the top of the board, one in each corner.) Remove A8W1 and A18A1W1. The A20 assembly is now free.

When reconnecting the ribbon cable to the A20 and A16A1 P.C. Boards, be extremely careful not to bend the pins.

A63 RF Attenuator Replacement Procedure

Refer to Figure 8H-4, "Front Panel Disassembly", in the **FRONT PANEL - REAR PANEL** functional group. Remove the front panel according to the instructions given in steps 1 through 7. It is not necessary to remove the ribbon cables.

Remove the two cables going to the A63 assembly. Remove the two screws that hold the A63 mounting bracket in place. Remove the two screws that hold the A63 assembly to its mounting bracket.

HINGED RF DECK ACCESS PROCEDURE

It is necessary to perform the following procedure to replace any of the following assemblies:

A13 Band 0-4 SYTM
A16 Mod Splitter
A18 Band 0 Power Amplifier
AT1 Band 1-4 Peripheral Mode Isolator

1. Remove the top, bottom, and perforated side covers. Place the instrument on its left side (as viewed from the front).

   Refer to Figure 8I-8, "RF Assemblies, Cables, Mounting Hardware Location".

CAUTION

A10J1 A10J2 and A10J3 are precision APC 3.5 mm connectors. The cables and A11 Band 1-4 Detector assembly that connect to them use SMA connectors. Extreme care should be taken when disconnecting or connecting an SMA cable from a mating 3.5 mm connector. The SMA cable center conductor must align with the 3.5 mm connector center conductor. If there is any axial force on the cable when disconnecting the SMA fitting, the 3.5 mm connector center conductor may be damaged, necessitating the replacement of the A10 Directional coupler. Remove any axial force on the cable by first disconnecting the end of the cable that does not mate with a 3.5 mm connector or by removing the mounting screws of the device having 3.5 mm connectors. Perform both safeguards where possible. The A10J2 - A11J1 connection is not as critical because the A11J1 connector has a captured nut. This nut does not allow axial force on the APC 3.5 mm center conductor until well after the SMA center conductor is disengaged.

Bottom of Instrument

2. Remove W15 from the A12 assembly. Disconnect W16 from the A13 Band 0-4 SYTM. Carefully disconnect the other side of W16 from the A10 assembly and completely remove W16 from the instrument. Use extreme care to avoid axial force on the W16 to A10J1 connection.

3. Remove three side panel screws (item 4) that hold the A13 assembly to the side rail.

4. Remove two side panel screws (item 5) that hold the RF Deck to the side rail.

Top of Instrument

5. Remove W3 and W4 from the A16 assembly.

6. Remove two screws (item 7) from the RF Deck (See View C).

7. Remove one screw (item 3) that holds the A8 casting to the A62 Motherboard.

Both Top and Bottom of Instrument

8. While holding W15 clear of A12J1 (Top), pull the A8 casting away from the instrument (Bottom). The RF Deck will swing open.

CAUTION

To avoid crushing A20 components mounted near the RF Deck hinge, do not open the RF deck to more than a 45 degree angle from its original position.

Removing the cable going to the A8 assembly "100 MHz 0 dBm INPUT" will allow the RF Deck to open farther.

INDIVIDUAL ASSEMBLY SERVICE SECTION

A8 Through A18, A63, and AT1 are not field repairable. Refer to the Module Exchange Program section of the **"RF SECTION REPAIR PROCEDURE."**

A8 3.7 GHz OSCILLATOR

Introduction

Refer to Figure 8I-10, "A8 3.7 GHz Oscillator, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The A8 3.7 GHz Oscillator Assembly provides a clean, stable 3.7 GHz signal against which a swept 3.71 to 6.10 GHz signal is mixed in order to generate Band 0 frequencies of 10 MHz to 2.4 GHz. This heterodyne scheme is used in the 8340A because the YO is not capable of generating frequencies below 2 GHz. In order to maintain the same frequency accuracy as Bands 1-4, the 3.7 GHz Oscillator is phase-locked to a 100 MHz instrument reference. Also provided within the A8 assembly are a phase lock detector and indicator and a linear modulator (for Band 0 ALC control).

The overall functions of the 3.7 GHz Oscillator can be divided into two major parts. A microcircuit assembly contains an oscillator, sampler, and modulator. A printed circuit board assembly contains a 100 MHz amplifier, a phase lock amplifier, and a phase lock indicator.

The oscillator consists of a bistable pair of bipolar transistors and a microstrip resonator, tuned with a varactor diode. The tuning range of the oscillator is nominally 3.685 to 3.715 GHz. Outputs from this oscillator are sent to a sampler and through a modulator and a bandpass filter to the SMA output port.

The modulator is a shunt reflective PIN modulator providing at least 60 dB of modulation at 20 milliamps bias current.

The sampler consists of a balanced pair of Schottky diodes driven by a step recovery diode. Its purpose is to provide a sampled (at 100 MHz) version of the 3.7 GHz signal to the phase locked loop.

One of two amplifiers on the printed circuit board is a narrow-band 100 MHz-tuned amplifier whose purpose is to drive the step recovery diode (of the sampler circuit). This amplifier is designed to raise the 100 MHz input signal level from 0 dBm to approximately 10 dBm to drive the step recovery diode.

The 100 MHz amplifier consists of two gain stages and a matching circuit for the step recovery diode.

This first stage of the amplifier involves Q1, operating in a class A configuration. R3 provides a stable dc bias. Capacitor C2 provides emitter bypass. C1 and L1 form a band pass input. C1 also provides a dc block. Base bias is through resistor R1, while collector bias is provided by L2.

Capacitor C3 acts as a supply bias. To ensure overall amplifier stability, C3 must provide good bypass at frequencies down to 100 kHz. At under 100 kHz, the amplifier gain is small enough so that stability is insured.

Interstage matching is accomplished by C4, C5, and L3. C5 also serves as a dc block. C4 is adjustable so that a good match can always be obtained.

The second stage amplifier is Q2, which is operated in a class B configuration to provide reasonable output power with low dc input power. Base bias is through a ground wire with two ferrite beads (E2 and E3) to provide high RF impedance. Collector bias is through R4 and L4, with supply bypass capacitor C6. R4 serves to lower dissipation in Q2 and as a low pass filter (along with C6) to enhance supply isolation.

Capacitor C7 is a dc block, while C8, L5 and R5 form a drive circuit for the step recovery diode. C8 and L5 provide a good match for the step recovery diode at 100 MHz, while R5 provides a good match at lower frequencies, as well as providing step recovery diode bias. Resistor R5 is necessary to prevent diode squegging.

Phase Lock Amplifier

The phase lock amplifier provides two major functions. First, it forms a phase-locked loop together with the microcircuit, tuned oscillator, and mixer. This loop keeps the oscillator output at 3.7 GHz. Second, when the loop is not locked, the amplifier provides a search oscillation that sweeps the VCO over a wide enough range to allow the loop to lock to the 37th harmonic of the 100 MHz input.

An RC network composed of R6-8, C9 and C10 combines and filters the two outputs from the microcircuit sampler. Potentiometer R8 provides an adjustment to compensate for unequal outputs from the two sampler ports, allowing the loop to close (with 0 Vdc at Q3A base). In the absence of signals from the sampler (i.e., microcircuit removed or defective), R9 provides bias for Q3A base. This allows a search oscillation to occur and keeps the amplifier from latching up in an unwanted mode.

Transistors Q3A and Q3B are a matched differential pair which form the amplifier inputs. Bias is provided by R10, R12, and R13. High frequency gain is set by R11. Output from the first amplifier is fed differentially to transistors Q4 and Q5, another differential pair. Tuning voltage output is taken single-ended from the collector of Q4.

The second amplifier bias is provided by the matched pair of Q6A and Q6B. Since the bases and emitters of Q6 are tied together, current through each must to be equal.

Resistors R19 and R20 lower the voltage drop across Q6 and thus, lessen power dissipation in Q6. R20 also limits the maximum current flow in Q6. Gain shaping for the overall amplifier is provided by R14-17. A feedback path including R21 and C14 causes the amplifier to oscillate at approximately 30 Hz whenever the loop is open (unlocked). This is the search oscillation required for signal acquisition.

Lock Indicator

The lock indicator senses when the phase lock loop is not locked. The out of lock condition is one where the tuning voltage is greater than 0 Vdc or less than -35 Vdc (regardless of whether the voltage is constant or due to search oscillation.

Timer U1 is set up as a monostabe multivibrator. Whenever the oscillator tune line is greater than 0 Vdc, transistor Q7 turns on. This makes U1 input pin 2 LOW and causes a pulse output on pin 3. If the voltage stays HIGH, pin 3 stays HIGH. Whenever the tune line goes below -35 Vdc, Q8 turns on and U1 pin 3 goes HIGH.

The output pulse width is approximately the period of the search oscillation (approx. 30 msec). During search oscillation, U1 pin 3 will continuously be HIGH.

When the tuning voltage stays between 0 and -35 Vdc, U1 pin 3 stays LOW. The search oscillator is a linear oscillator, therefore, the tuning voltage should always go to 0 or -35 Vdc unless the loop is locked.

The output can source at least 30 mA of current and can be used to directly drive an LED indicator.

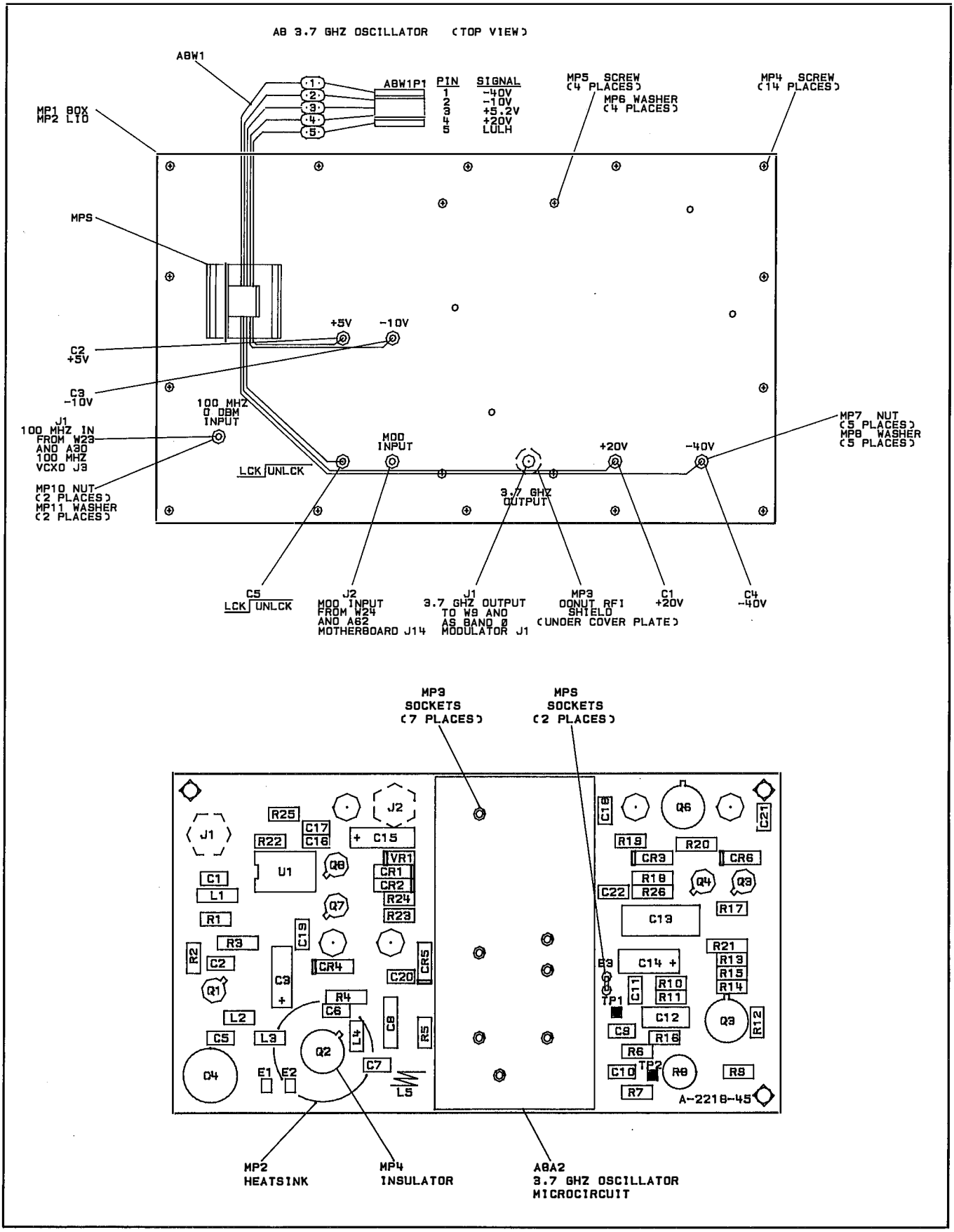


Figure 8I-10. A8 3.7 GHz Oscillator, Component Location Diagram

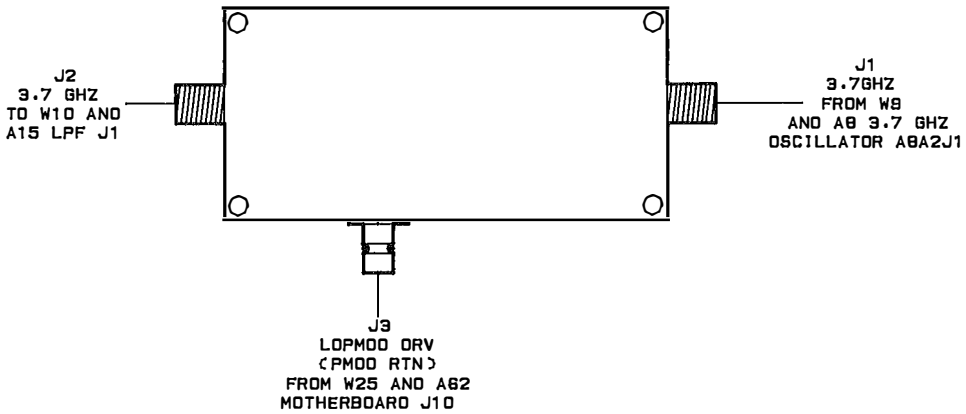


Figure 8I-11. A9 Band 0 Pulse Modulator, Component Location Diagram

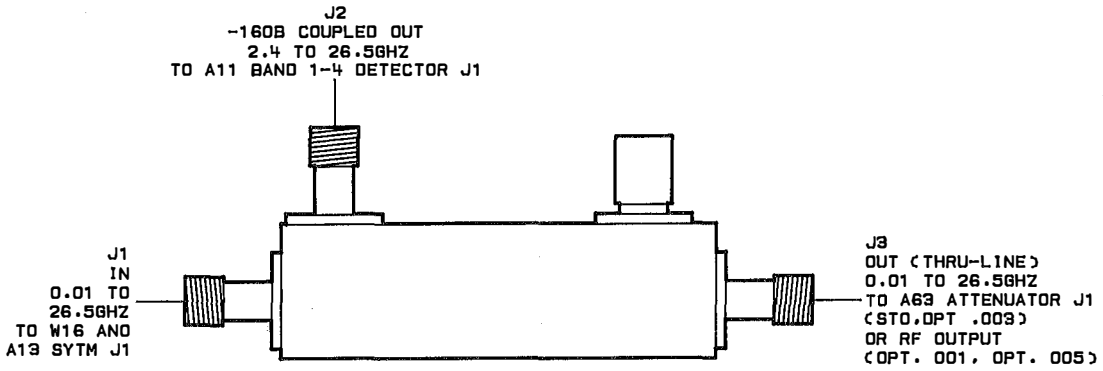


Figure 8I-12. A10 Directional Coupler, Component Location Diagram

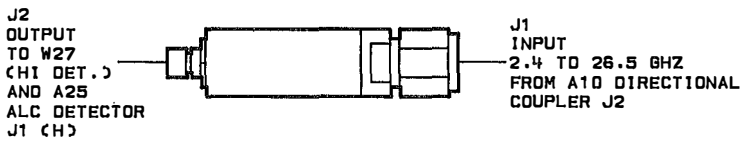


Figure 8I-13. A11 Band 1-4 Detector, Component Location Diagram

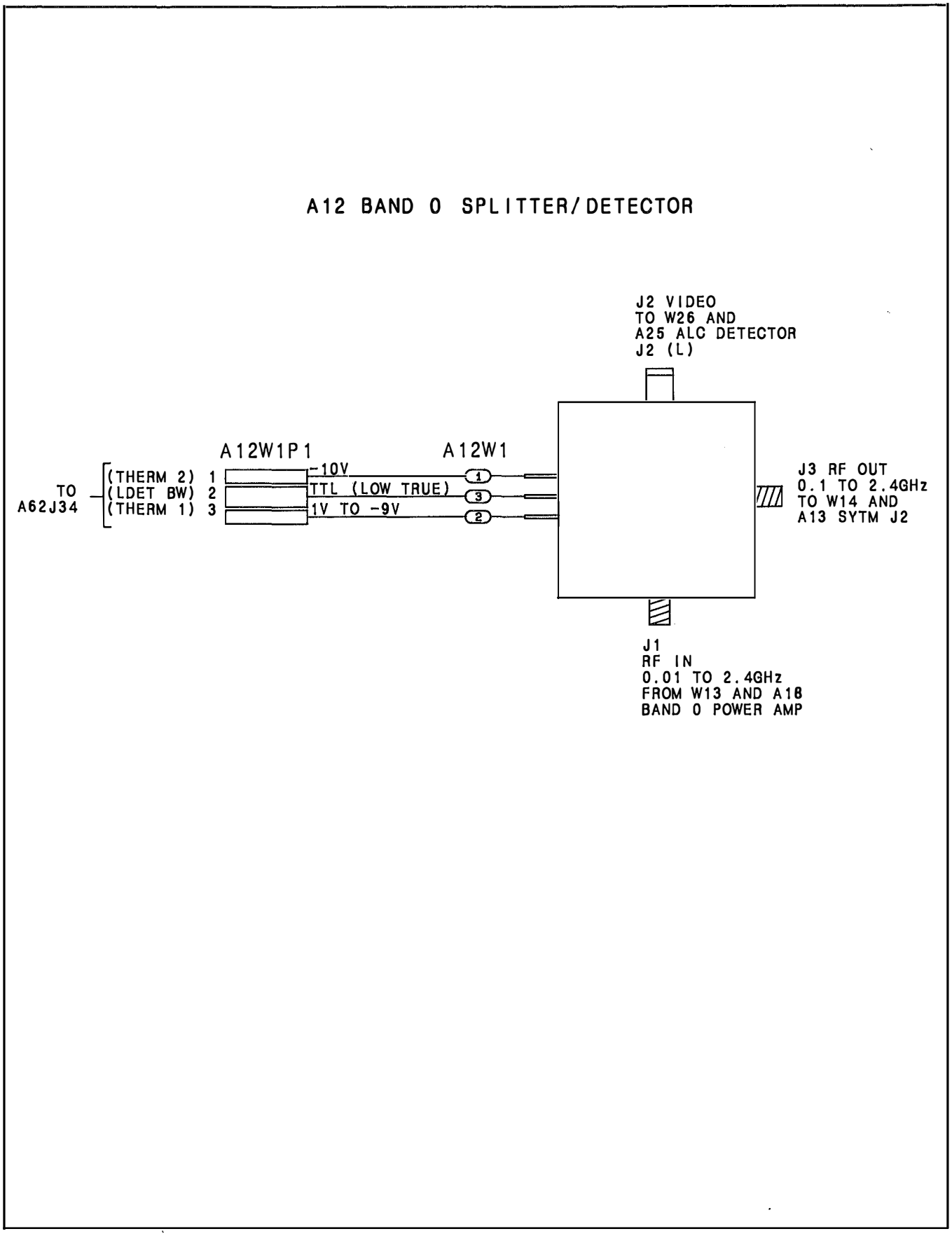


Figure 8I-14. A12 Band 0 Splitter Detector

A62J34 TO A12W1P1 PIN I/O

Pin	Mnemonic	A12W1P1	Levels
1	THERM 2	PIN 1	−10V
2	LOETBW	PIN 2	TTL (LOW TRUE)
3	THERM 1	PIN 3	1V TO −8V

Note: Refer to RF Section Schematic Diagram and A62 Motherboard Wiring List for signal source and destination information.

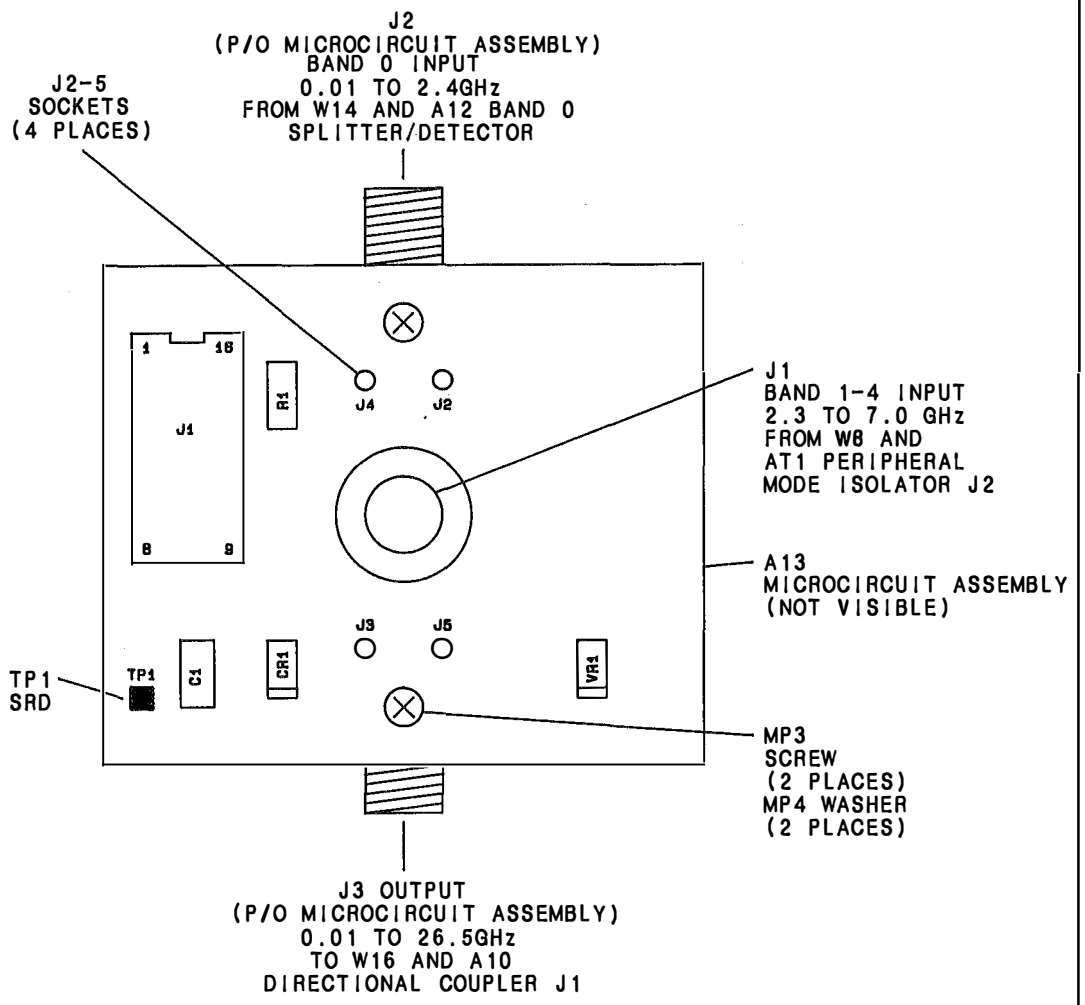


Figure 8I-15. A13 SYTM, Component Location Diagram

A62J18 TO A13A1J1 PIN I/O

Pin	Mnemonic	A13A1J1	Levels
1 2	SRD BIAS	PIN 2	−10V/THRU 2000 OHMS TO +5V
3 4	SYTM COIL −	PIN 4	−40V TO −25V
5 6	+20V	NOT USED	+20V
7 8	−10V SYTM HTR	NOT USED PIN 8	−10V 0V TO +20V
9 10	SYTMTHRM PINBIAS	PIN 9 PIN 10	APPROX. −5V −4V TO +12V
11 12	STYM COIL −	PIN 12	−40V
13 14	SYTM GNO SYTM GND	NOT USED PIN 14	0V 0V
15 16	SYTM GND	PIN 15	0V

Note: Refer to RF Section Schematic Diagram and A62 Motherboard Wiring List for signal source and destination information.

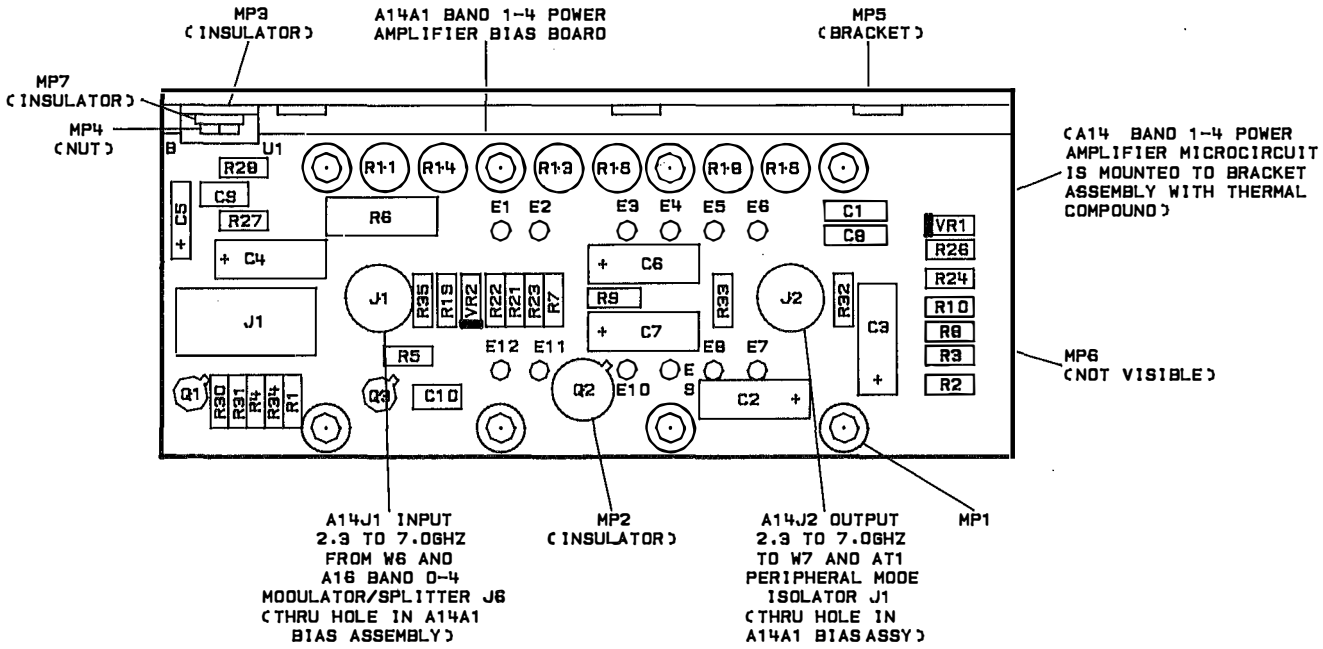


Figure 8I-16. A14A1 Band 1-4 Power Amplifier Bias Assembly Component Location Diagram

Figure 8I-17. A15 Band 0 Low Pass Filter

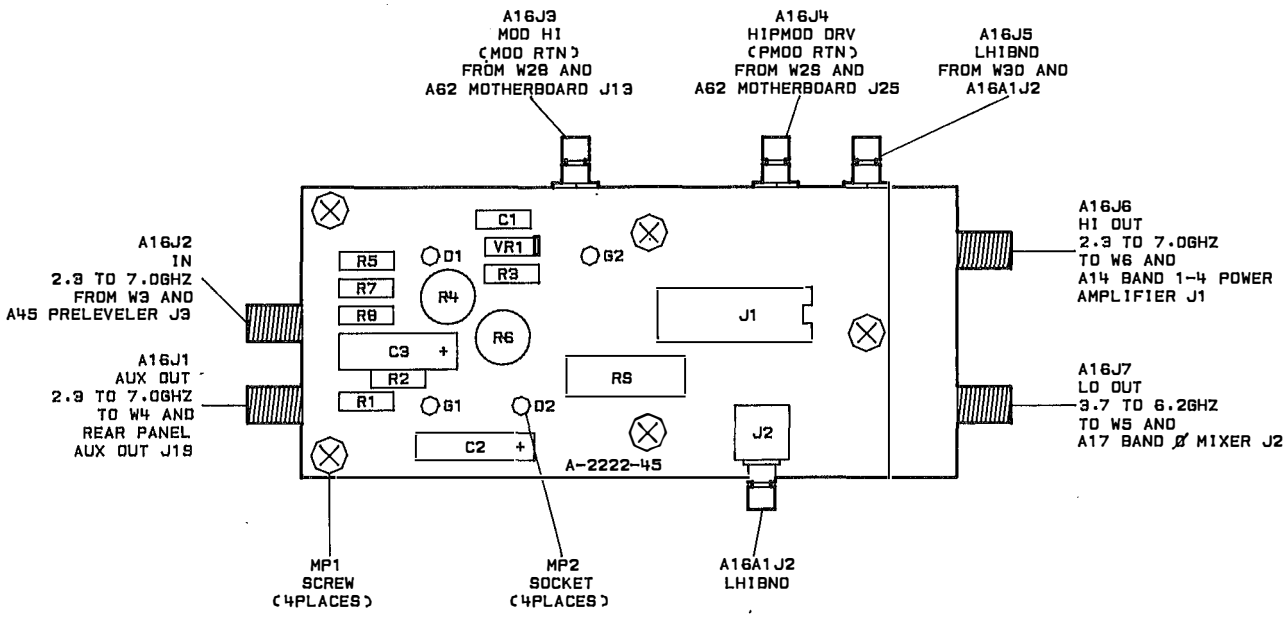


Figure 8I-18. A16 Band 1–4 Modulation/Splitter, Component Location Diagram

A62J19 TO A16A1P3 AND A20P2 PIN I/O

Pin	Mnemonic	A62W31P2	A62W31P3	A16A1J1	A20J1	Levels
1	GND PLANE	PIN 1	PIN 1	PIN 1	PIN 1	0V
2	+20V	PIN 2	NOT USED	NOT USED	PIN 2	+20V
3	+5.2V	PIN 3	PIN 3	PIN 3	PIN 3	+5.2V
4	−5.2V	PIN 4	PIN 4	PIN 4	PIN 4	−5.2V
5	−10V	PIN 5	NOT USED	NOT USED	PIN 5	−10V
6	−40V/−40V SENSE (−)	PIN 6	NOT USED	NOT USED	PIN 6	−40V
7	LHET	PIN 7	NOT USED	NOT USED	PIN 7	TTL (LOW TRUE)
8	LHET	PIN 8	NOT USED	NOT USED	PIN 8	TTL (LOW TRUE)
9	GND PLANE	PIN 9	PIN 9	PIN 9	PIN 9	0V
10	+20V	PIN 10	NOT USED	NOT USED	PIN 10	+20V
11	+5.2V	PIN 11	PIN 11	PIN 11	PIN 11	+5.2V
12	−5.2V	PIN 12	PIN 12	PIN 12	PIN 12	−5.2V
13	−10V	PIN 13	NOT USED	NOT USED	PIN 13	−10V
14	−.25V/GHZ	NOT USED	NOT USED	NOT USED	NOT USED	−.25V/GHZ
15	LHIBND	NOT USED	PIN 15	PIN 15	NOT USED	TTL (LOW TRUE)
16	HULH	PIN 16	NOT USED	NOT USED	PIN 16	TTL (HIGH TRUE)

Note: Refer to RF Section Schematic Diagram and A62 Motherboard Wiring List for signal source and destination information.

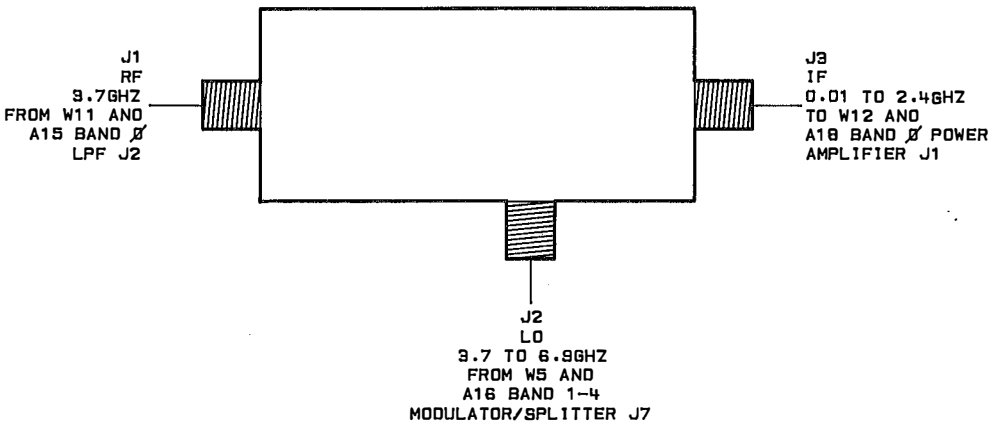


Figure 8I-19. A17 Band 0 Mixer, Component Location Diagram

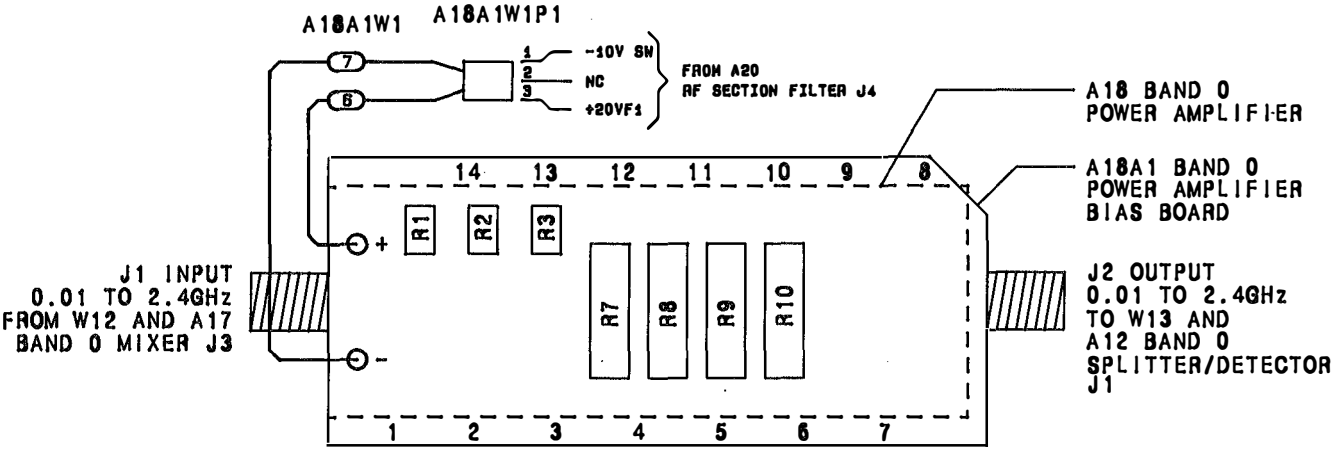


Figure 8I-20. A18 Band 0 Power Amplifier, Component Location Diagram

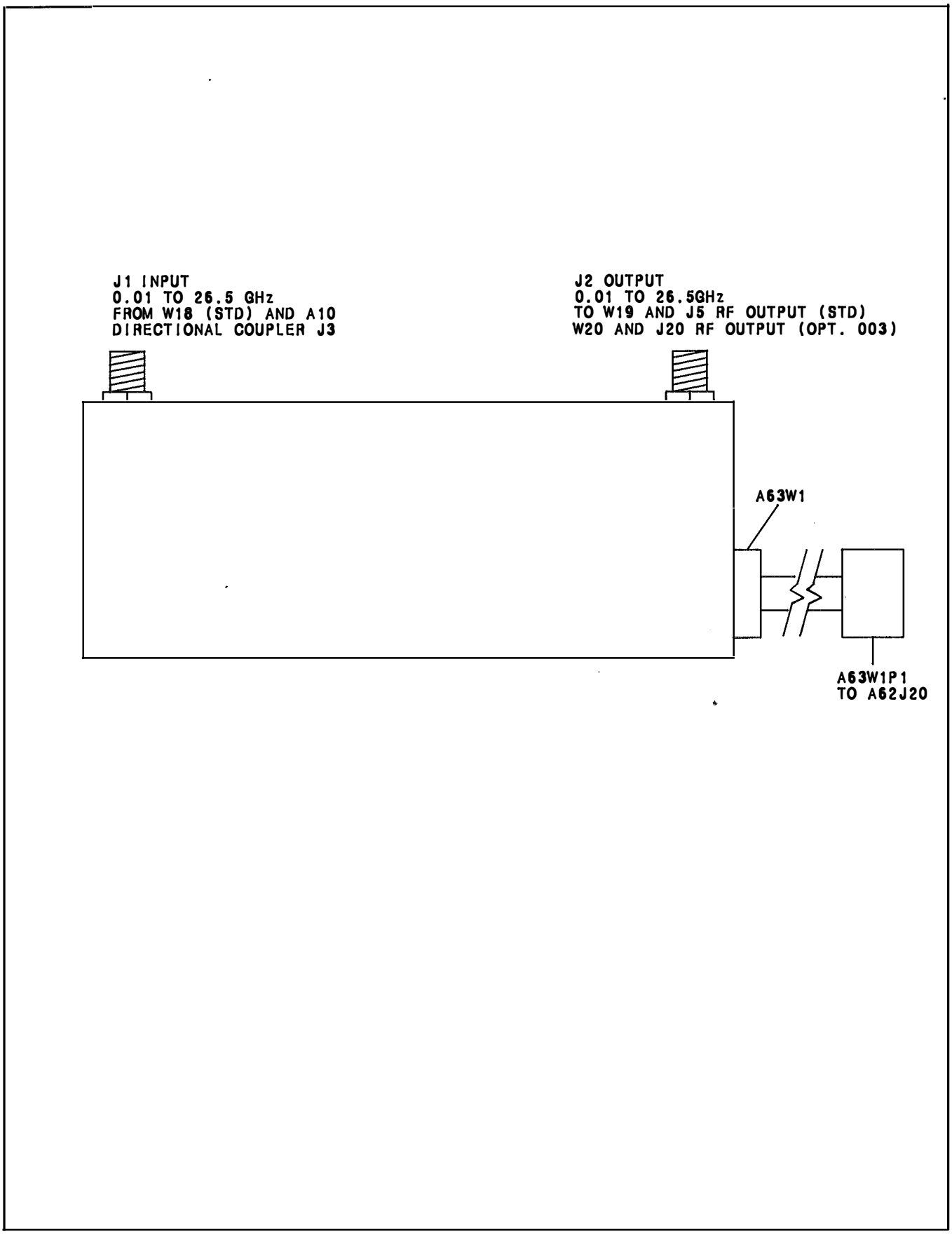


Figure 8I-22. A63 90 dB Programmable RF Attenuator, Component Location Diagram

A62J20 TO A63W1 P1 PIN I/O

Pin	Mnemonic	A63W1 P1	Levels
1			
2	ATNAT1	PIN 2	OPEN COLLECTOR
3	ATNTH2	PIN 3	OPEN COLLECTOR
4	ATNTH4	PIN 4	OPEN COLLECTOR
5	ATNAT3	PIN 5	OPEN COLLECTOR
6	ATN COIL +	PIN 6	+5V
7			
8			
9	ATNAT2	PIN 9	OPEN COLLECTOR
10	ATNAT4	PIN 10	OPEN COLLECTOR
11	ATNTH3	PIN 11	OPEN COLLECTOR
12			
13	ATNTH1	PIN 13	OPEN COLLECTOR
14	LATTN	PIN 14	TTL (LOW TRUE)

Note: Refer to RF Section Schematic Diagram and A62 Motherboard Wiring List for signal source and destination information.

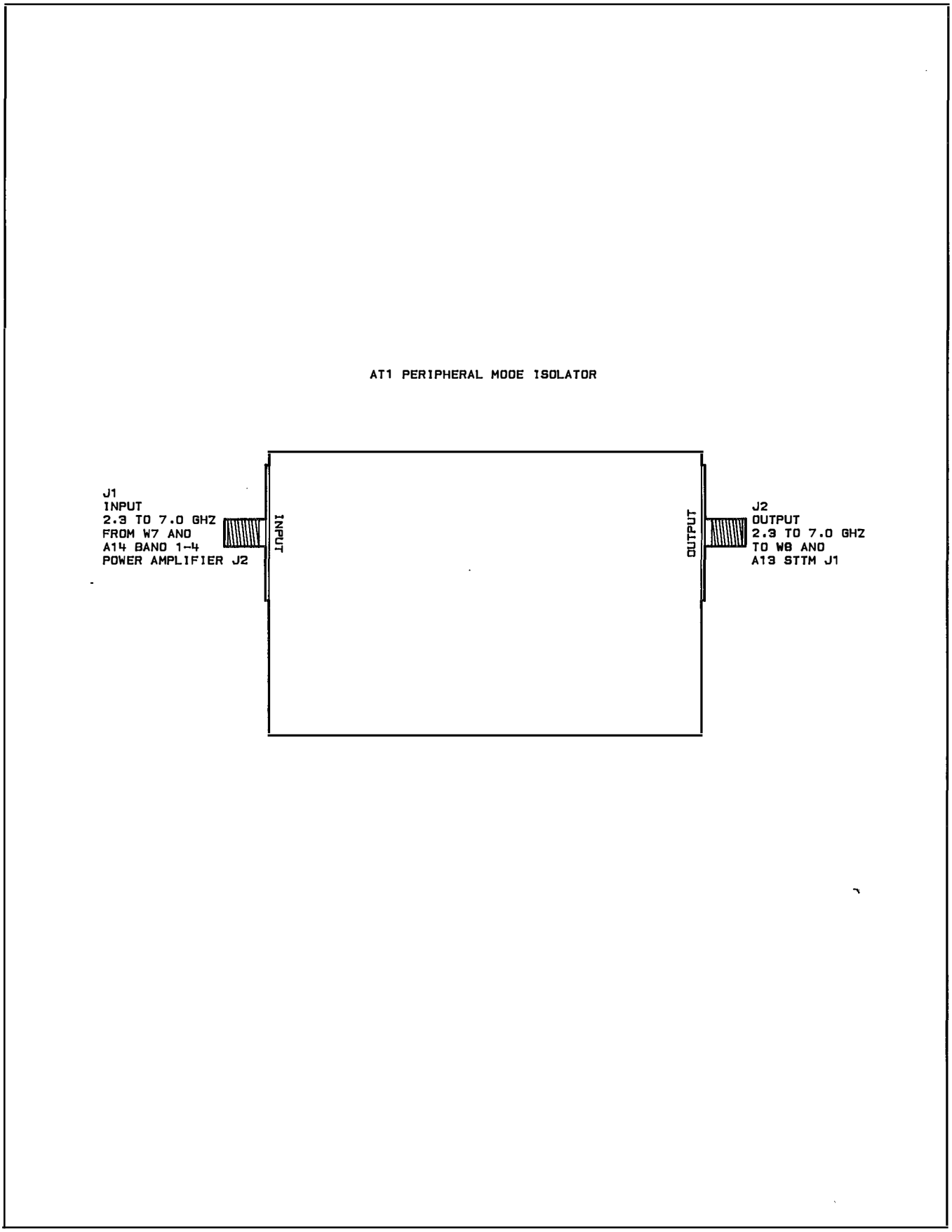


Figure 8I-23. AT1 Peripheral Mode Isolator, Component Location Diagram

A20 RF SECTION FILTER, CIRCUIT DESCRIPTION

Introduction

The RF Section Filter consists of the following major sections:

- Power Amplifier Supply Filters
- Band 0 Amplifier Switch.

Power Amplifier Supply Filters

Refer to Figure 8I-24, "A20 RF Section Filter, Component Location Diagram", and Figure 8I-42, "RF Section Schematic Diagram". The Band 1-4 Amplifier draws a substantial amount of current from the +5.2V and -10V supplies when operated at full power. During Pulse operation the input signal to the Power Amp is turned off and on at the pulse rate. This causes large surge currents in the supply lines which, if unfiltered, would cause the voltages to fluctuate at the pulse rate. (This occurs because the pulse rate is normally at a higher frequency than the power supply bandwidths.) These voltage fluctuations would affect the YO Phase Lock circuitry and the main YO Coil Driver circuitry causing large sidebands on the output carrier at the pulse frequency. To minimize this effect, a two stage LC filter is used in both the +5.2V and -10V supply lines going to the Band 1-4 Amplifier.

The sidebands would be of little consequence in the (pulsed) front panel output. They would be apparent, however, at the rear panel YO AUX output (producing 50-60 dBc sidebands) when the front panel output is being pulsed.

Band 0 Amplifier Switch

The Band 0 Amplifier Switch turns off the -10V supply to the Band 0 Amp when the instrument is not operating in Band 0.

When the LHET signal is LOW (indicating that the instrument is operating in Band 0 [Heterodyne Band]), Q1 is turned on by the voltage divider formed by R2 and R3. The collector of Q1 is pulled up to ground, and thus Q2 is biased on via the voltage divider formed by R4 and R5. Q2 saturates, and its collector is pulled down to -10V, turning on the Band 0 Amplifier. When LHET is HIGH, Q1 and Q2 are biased off, turning off the Band 0 Amplifier. The -10V input to this switch is derived from the filtered -10V supply that is also used by the Band 1-4 Amplifier.

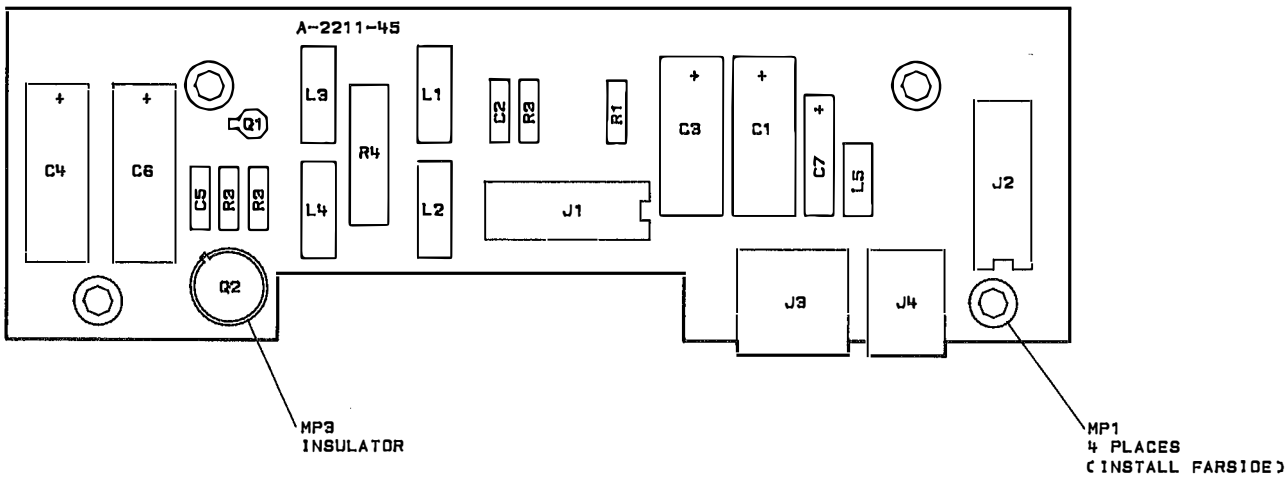


Figure 8I-24. A20 RF Section Filter, Component Location Diagram

A62J19 TO A16A1P3 AND A20P2 PIN I/O

Pin	Mnemonic	A62W31P2	A62W31P3	A16A1J1	A20J1	Levels
1	GND PLANE	PIN 1	PIN 1	PIN 1	PIN 1	0V
2	+20V	PIN 2	NOT USED	NOT USED	PIN 2	+20V
3	+5.2V	PIN 3	PIN 3	PIN 3	PIN 3	+5.2V
4	−5.2V	PIN 4	PIN 4	PIN 4	PIN 4	−5.2V
5	−10V	PIN 5	NOT USED	NOT USED	PIN 5	−10V
6	−40V/−40V SENSE (−)	PIN 6	NOT USED	NOT USED	PIN 6	−40V
7	LHET	PIN 7	NOT USED	NOT USED	PIN 7	TTL (LOW TRUE)
8	LHET	PIN 8	NOT USED	NOT USED	PIN 8	TTL (LOW TRUE)
9	GND PLANE	PIN 9	PIN 9	PIN 9	PIN 9	0V
10	+20V	PIN 10	NOT USED	NOT USED	PIN 10	+20V
11	+5.2V	PIN 11	PIN 11	PIN 11	PIN 11	+5.2V
12	−5.2V	PIN 12	PIN 12	PIN 12	PIN 12	−5.2V
13	−10V	PIN 13	NOT USED	NOT USED	PIN 13	−10V
14	−.25V/GHZ	NOT USED	NOT USED	NOT USED	NOT USED	−.25V/GHZ
15	LHIBND	NOT USED	PIN 15	PIN 15	NOT USED	TTL (LOW TRUE)
16	HULH	PIN 16	NOT USED	NOT USED	PIN 16	TTL (HIGH TRUE)

Note: Refer to RF Section Schematic Diagram and A62 Motherboard Wiring List for signal source and destination information.

A21 PULSE MODULATOR, CIRCUIT DESCRIPTION

Introduction

The A21 Pulse Modulator assembly controls the pulse modulation functions for the 8340A. The front panel BNC "PULSE MODULATION INPUT" is the main control signal. The A21 Pulse Modulator then drives the PIN switch RF modulators in the A9 (for Band 0) or A16 (for Band 1-4) microcircuits. In addition, timing circuits send control signals to key elements of the ALC loop to coordinate the leveling function with the pulse modulation.Refer to Figure 8I-26, "A21 Pulse Modulator Driver, Schematic Diagram".

Input Buffer and Control Logic A

The input buffer (Q7 circuit) buffers the "PULSE MODUATION INPUT" (TTL compatible; HIGH = RF ON; LOW = RF OFF), and protects Q7 from higher input voltages. Two control lines gate the pulse input. HPLSEN gates the buffered pulses (HIGH = Enabled; LOW = Disabled). HRFON overrides the pulse input, causing the RF to be turned OFF (HIGH = RF ON; LOW = RF OFF). TP5 is the assembly's primary gated control line (HIGH = RF OFF; LOW = RF ON).

With no input signal CR1 is forward biased, Q7 is on and U1C pin 10 is LOW. During the LOW state of an input signal, CR1 is turned off, Q7 is off and U1C pin 10 is HIGH. The output of U1C (pin 8) will not go LOW unless HPLSEN is HIGH. If either input to U1B is LOW the RF is turned OFF.

The input impedance is established by R14. If necessary R14 can be changed to 51.1 ohms to provide a 50 ohm input impedance. If this is done, however, an open-circuit input will no longer be pulled HIGH. Thus, if pulse modulation is activated with open-circuit input, the RF will go OFF.

Modulator Driver B

The Modulator Driver provides the current and voltage bias for the RF pulse modulators, controlled by TP5. Differential current switch Q2 and Q3 control the bias for the drivers Q5 and Q8. With TP5 HIGH (HIGH = RF OFF), Q2 is off and Q3 is on, sourcing current through CR4 and CR5. This turns Q5 on, sourcing 20mA through R11 to bias the PIN diode modulator on, turning the RF OFF. With TP5 LOW (LOW = RF ON), Q2 is on and Q3 is off. Now the drivers are biased through CR8, CR3, CR4, CR6, and R10 to -10VF. This turns Q8 on, back-biasing the PIN diodes and turning the RF ON. C3 and C4 AC-couple the transition current spikes from the modulators back to the A21 assembly.

Output Multiplexer C

The Output Multiplexer selects one RF modulator to receive the pulse modulation control. With LHET LOW (LOW = Band 0), U3D and U3C turn Q12 on and Q11 off, selecting A9 (Band 0) to pulse modulate. With LHET HIGH (HIGH = Band 1-4), Q12 is off and Q11 is on, pulse modulating A16 (Band 1-4). U3B biases A16 off when HRFON is LOW (LOW = RF OFF) when the front panel "RF" is OFF and during retrace.

ADC Timing D

The ADC Timing enables the ADC (A27) to monitor the detected power level when either the RF is ON or up to 1 millisecond after the RF has been turned OFF. This is to prevent the "POWER dBm" display from showing an invalid power level if the RF has been turned OFF for over 1 millisecond (ALC Sample/Hold droop). With TP5 LOW (RF on), TP3 is forced HIGH to enable the ADC. When TP5 goes HIGH, one-shot U2B is triggered to output a 1 millisecond LOW pulse, holding the ADC enabled. If the RF is not turned ON again within 1 millisecond, U2B returns HIGH, forcing TP3 LOW to disable the ADC.

Integrator Timing E

The Integrator Timing controls timing to gate the integrator input of the main ALC amp (A26), ensuring that the integrator responds to RF power level error signals only when the RF level detected is ON and stable. When TP5 goes LOW (RF ON), U1A output is forced HIGH. The following LOW-pass filter section delays the transition by 1 microsecond. When TP2 goes HIGH, the integrator (A26) is enabled. When TP5 goes HIGH again (RF OFF), U1A output goes LOW to put the integrator circuits into hold. One-shot U2A is triggered when TP5 goes LOW, outputting a LOW pulse to U1A. This determines the minimum time that TP2 is HIGH (integrate) for each RF pulse with very narrow pulse widths. The one-shot time period depends on the ALC loop bandwidth and is controlled by HLBW. With HLBW HIGH, the minimum sample time is 1 microsecond; with HLBW LOW, the minimum sample time is 10 microseconds.

Sample/Hold Timing F

The Sample and Hold Timing controls timing of sample/hold gate in detector circuits (A25) during pulse modulation. The key timing element is C13. The time delay constant is independent and adjustable for both RF ON and RF OFF. The voltage on C13 is detected by Schmitt trigger Q6/Q9. The squarewave output is then delayed from the pulse at TP5, with both leading and trailing edges delayed by independent and adjustable time periods.

The circuit functions as follows: Presume C13 to be charged. When TP5 goes LOW (RF ON), Q1 turns off, and C13 discharges through R24, R23, R22, and R21. R21 adjusts the "ON DELAY" (discharge). When the voltage on C13 reaches the lower threshold, +1.2V, Q6/Q9 fires and TP1 goes HIGH to sample. When TP5 goes back HIGH (RF OFF), Q1 turns on, and charges C13 through R23 and R24. R23 is adjustable and controls the "OFF DELAY" (charge). When the voltage on C13 reaches the upper threshold, +1.5V, Q6/Q9 fire and TP1 goes LOW to hold. If C13 is not fully discharged before TP5 goes HIGH again, the rising edge of TP5 will turn on Q4 very briefly through C12 to fully discharge C13. This ensures that the "OFF DELAY" is independent of pulse width.

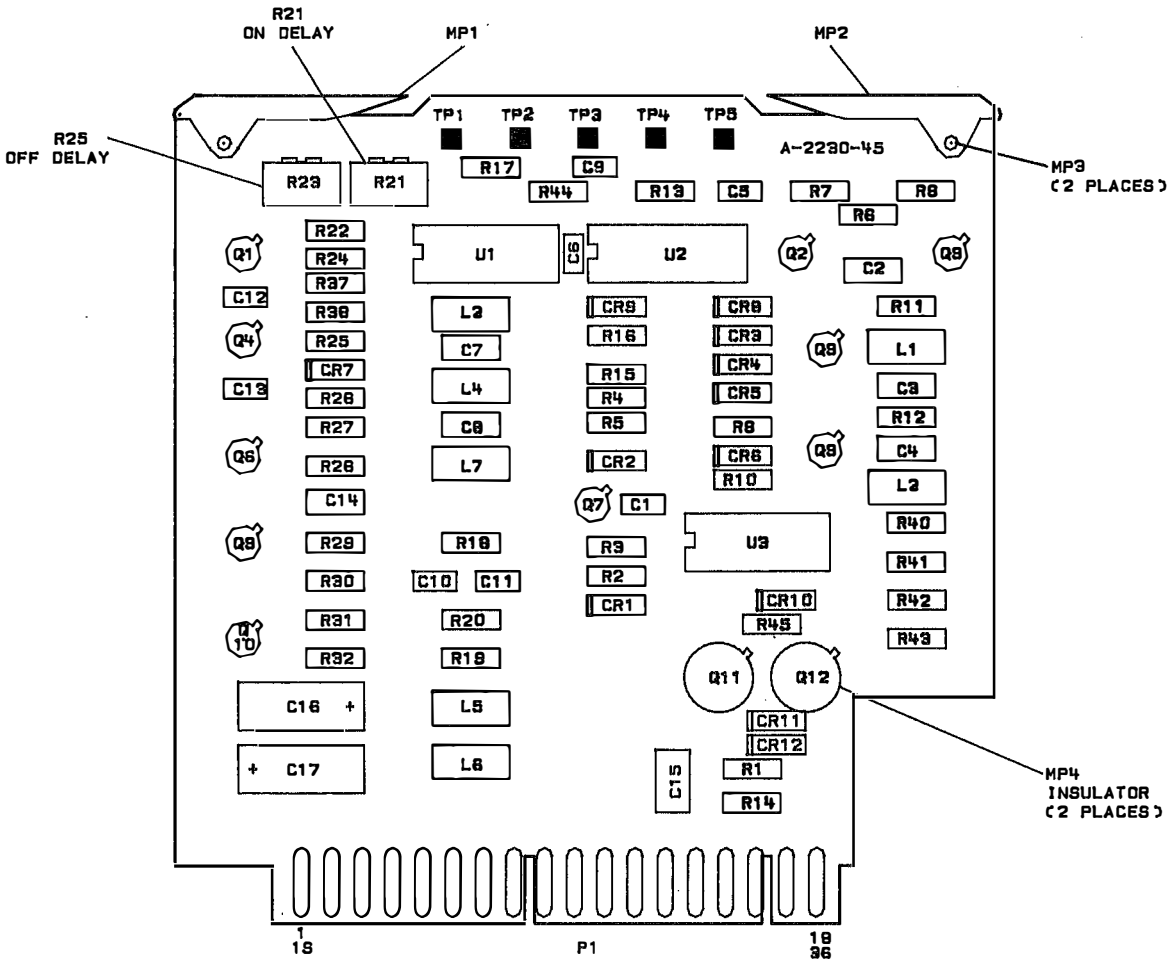


Figure 8I-25. A21 Pulse Modulator Driver, Component Location Diagram

A21 Pulse Modulator Driver P1 Pin I/O

A21

Pin	Mnemonic	Levels	Source	Destination
1 19	HADCEN	TTL (HIGH TRUE)	D	XA27P1-8
2 20	LMODHLD	TTL	E	XA26P1-1
3 21	DET S/H + DET S/H −	+4.5V/+3.5V +3.5V/+4.5V	F F	XA25P1-2 XA25P1-24
4 22	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*G *G
5 23	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*G *G
6 24	HLBW	TTL (HIGH TRUE)	XA26P1-33	XA26P1-33
7 25	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*G *G
8 26	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
9 27	HPLSEN HRFON	TTL (HIGH TRUE) TTL (HIGH TRUE)	XA26P1-2 XA57P1-105	*A *A C
10 28				
11 29	LHET	TTL (LOW TRUE)	XA27P1-20	*C
12 30				
13 31				
14 32				
15 33				
16 34	LOPMOD ORV	CURRENT SOURCE	C	A62J10-SMC CENTER
17 35	PLS IN RTN PMOD RTN	0V 0V	* B	*A *A
18 36	PLS IN HIPMOD ORV	TTL CURRENT TO PIN DIODE	A62J26-SMC CENTER C	A A62J25-SMC CENTER

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

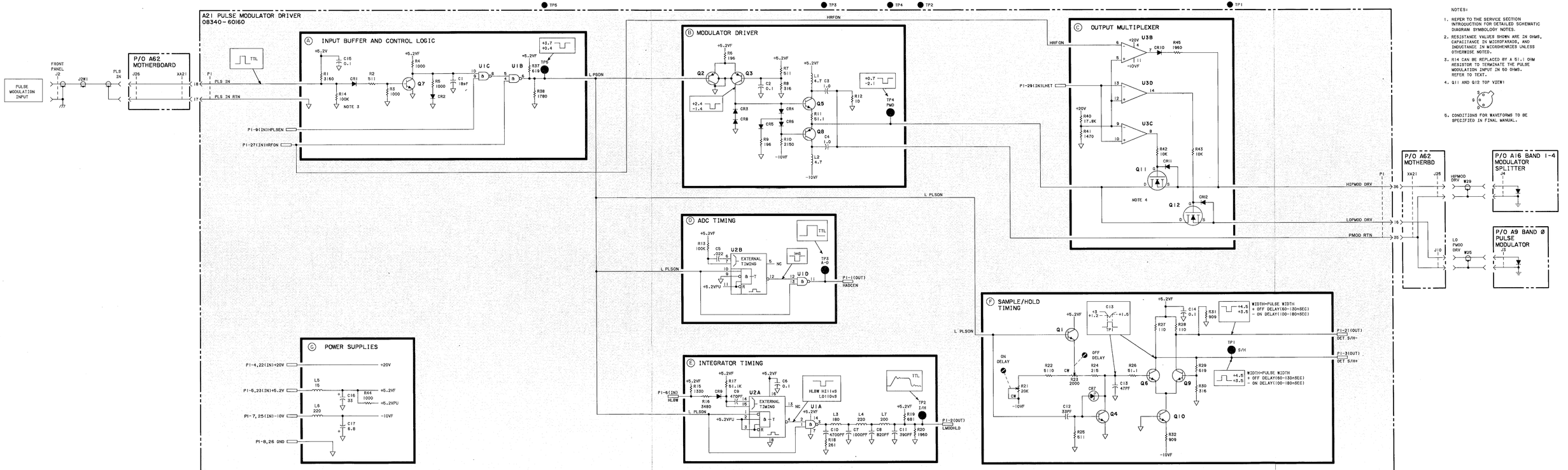


Figure 8I-26. A21 Pulse Modulator Driver, Schematic Diagram

A24 ATTENUATOR DRIVER/SRD BIAS, CIRCUIT DESCRIPTION

Introduction

Refer to Figure 8I-28, "A24 Attenuator Driver/SRD Bias, Schematic Diagram".

The A24 assembly has two primary functions. One is to control the 90 dB RF step attenuator. The other is to supply the correct bias voltage to the Step Recovery Diode (SRD) in the A13 Switched YIG-Tuned Multiplier (SYTM). The optimum bias voltage is a function of both RF power level and frequency, and also depends upon the frequency band being used. In addition, a simple circuit provides the correct bias for the PIN Diode switch in the A13 SYTM to select Band 0 or Band 1-4.

Frequency Ramp Generator A

The Frequency Ramp Generator provides two frequency-tracking ramp voltages for the frequency-dependent element of the SRD bias circuits. A 1.4V/GHZ signal is generated on the A28 assembly and sent to the Frequency Ramp Generator through A24P1-6. U1A amplifies and offsets this ramp to produce a descending ramp at TP4. This ramp is again offset and inverted to produce an ascending ramp at TP5. These two opposing ramps are each attenuated through variable resistors and then summed together to form a new ramp in Block **B**.

Modulator Voltage Clamp B

This circuit generates a voltage dependent on RF power level. Optimum SRD bias depends heavily upon RF power level to the A13 SYTM. SRD BIAS CONT from A26 supplies this information for the SRD bias adjustments. However, when the ALC loop goes unleveled, the SRD BIAS CONT line moves abruptly positive and no longer represents RF power level. The Modulator Voltage Clamp adds two frequency-dependent voltage ramps to this signal. The offsets are adjusted such that when the SRD BIAS control jumps positive, the base-emitter junctions of Q1, Q2, and Q3 (Block **D**) become reverse-biased, breaking the connection between SRD BIAS control and the SRD BIAS.

Band Decoder C

The Band Decoder provides control signals based upon the frequency band being used. HLB0, HLB1, and HLB2 are encoded with the current band. They are decoded by U5 into five distinct control lines (TP6 through TP10). Three of these control

open-collector comparators to drive FETs which control SRD bias. Two of the comparator outputs are in the SRD Bias Amplifier to select reverse-bias in Band 0, forward-bias in Band 1, and the freqency- and power-dependent bias in Bands 2, 3, and 4.

SRD Bias Adjustments D

The SRD Bias Adjustments circuitry provides the frequency and power-dependent bias adjustments for the SRD in Bands 2-4. Three identical circuits, each with three adjustments, sum together a synthesized control signal. Only one of these three circuits is used at a time, dependent upon the band being used, as switched by the FETs. In each section, two adjustments add currents proportional with frequency to Block **D**'s output current; a third adjustment subtracts current proportional to the RF power level through a transistor controlled by the Modulator Voltage Clamp circuit (Block **B**).

Exponential Generator E

The Exponential Generator shapes the current generated by the SRD Bias Adjustments circuitry to produce an exponentially shaped current output. Dual transistor Q7 is responsible for the relationship of collector current being an exponential function of base-emitter voltage. The use of a positive temperature coefficient resistor as well as a dual transistor helps cancel out thermal effects. The resulting output is a current sink which is an exponential function of the current input.

SRD Bias Amplifier F

The SRD Bias Amplifier converts the exponential current to a voltage that is fed to the SRD; it also establishes bias for special cases of Band 0 and Band 1. U3 converts the current sunk by the Exponential Converter to a voltage. The MIN adjustment determines the minimum bias voltage (about -0.5V) for very low power levels when the input current is zero. In the special case of Band 0, the L0 line is pulled LOW, sinking current through R34 and forcing the voltage at TP12 to about +7V. This reverse biases the SRD, attenuating the Band 1-4 RF path. In Band 1, the L1 line is pulled LOW, turning off Q8 and pulling about 5 milliamps through R35. This forward biases the SRD and allows the fundamental frequency to pass through the SYTM easily while minimizing harmonics. In Bands 2-4, Q8 is turned on and the exponential bias shaping previously discussed is used to bias the SRD.

PIN Diode Bias G

When Band 0 is selected, the PIN diode in the SYTM is reverse-biased, thus allowing the Band 0 signal to pass through the coupling loop to the output of the SYTM. When Band 1-4 is selected, the PIN diode in the SYTM is turned on, grounding one side of the output coupling loop. This is necessary for efficient coupling from the YIG sphere and helps attenuate any stray signals in the Band 0 path. Comparator U12B controls the bias applied to the cathode of the PIN diode in the A13 SYTM. The PIN diode is biased off (TP11 +12V HIGH) when Band 0 is selected and biased on (TP11 -10V LOW) when Band 1-4 is selected.

Read Status Output Buffer H

Several status lines are provided in the RF section which may be used to communicate information back to the instrument processor. Most of these lines are not used at present but may be used to provide information to the processor about the operating condition of PC boards in the RF section. This output buffer (U14) is a six bit tri-state buffer which is enabled by the RSTAT strobe (15,R3:) from the Address Decoder on the A24 assembly. The enable line has a pullup to prevent this buffer from being enabled when the A27 Level Control board is removed.

Attenuator Control Latch I

The Attenuator Control Latch (U5) is a 74LS175 latch which has both inverting and non-inverting outputs for each of four latched inputs. Data bits 10 through 13 are latched from the instrument data bus when the WLEVEL strobe (10,R1:) goes low, then high. A pull-up is provided on the WLEVEL strobe to prevent inadvertent writes if the A27 Level Control board (source of the strobe) is removed. Each data bit latched is used to control one of four attenuator sections. The non-inverting output of each bit is used to activate the driver which removes the attenuator card and inserts the through card for that section. The inverting output is used to activate the driver which removes the through card and inserts the attenuator card. The required inputs (DB 10 through DB 13) to select each attenuation (0 to 90 dB) is shown in a table on the A24 schematic.

Attenuator Coil Drivers J

The A63 Attenuator contains four attenuator cards (10 dB, 20 dB, 30 dB, 30 dB) and four through cards. Each section can switch in an attenuator card or a through card depending upon the total attenuation desired. These sections are switched in by latching solenoids. Once the actuator reaches full travel, the solenoid

coil is de-energized by opening contacts internal to the attenuator. Each coil draws 300 milliamps for approximately 8 milliseconds until the internal contacts open the coil circuit. Since each attenuator card requires two solenoids, there are a total of eight separate coils that must be driven at various times, depending upon the section switched and whether a through card or attenuator card is being inserted.

The coil drivers (U8, U9, U10, and U11) are 75451B peripheral positive-AND drivers. These devices are capable of driving 300 milliamps with a saturation voltage of less than 0.7 volts which is sufficient to drive the 5 volt coils of the attenuator. These drivers do not have diode protection to prevent damage from inductive kick back by the coils. For this reason a TID 125 array of diodes (U13) is connected to provide diode clamping to both ground and to +5.2 volts.

Since the peak current that must be provided to the attenuator and drivers is quite large, a separately filtered power source is provided for this circuitry via L5, C10 and C11 (Block **L**). The above filtering will prevent current transients from disturbing other functions on this P.C. board.

SYTM Heater Control K

In order to provide a reasonably constant temperature for the A13 SYTM, a heater (resistor) and a thermistor are installed inside the A13 SYTM.

The A13 SYTM uses the internal thermistor to provide a voltage that changes as the temperature inside changes. This voltage (SYTMTHRM) is sent to the A24 Assembly SYTM Heater Control where it is compared to a reference voltage and amplified by op-amp (A24U4). The inverting input of this op-amp is referenced to -5 volts to set the operating point of the amplifier. The -5 volts is obtained from the divider formed by R50 and R51.

As the temperature inside the A13 SYTM rises, the thermistor resistance decreases, causing the voltage at A24TP2 to increase. A24R48 is the input resistor to the op-amp. When the voltage at A24TP2 increases, the voltage at the op-amp output (U4 pin 6) increases, decreasing the current to the base of Q9. This decreases the amount of current provided to the A13 SYTM heater, and thus decreases the temperature. Feedback is provided around this circuit by A24R49 and A24C13. This feedback allows a very large gain at dc and sets a gain of 30 at frequencies above a few hundredths of a Hertz.

The reverse of the above occurs if the temperature inside the A13 SYTM decreases. This circuit is designed to maintain the

temperature of the YIG sphere at approximately 85 degrees centigrade, independent of the ambient temperature.

Power Supply L

An LC filter circuit is used on each power supply line. The component values for these filters were chosen to form a low Q circuit to reduce any chance of resonances.

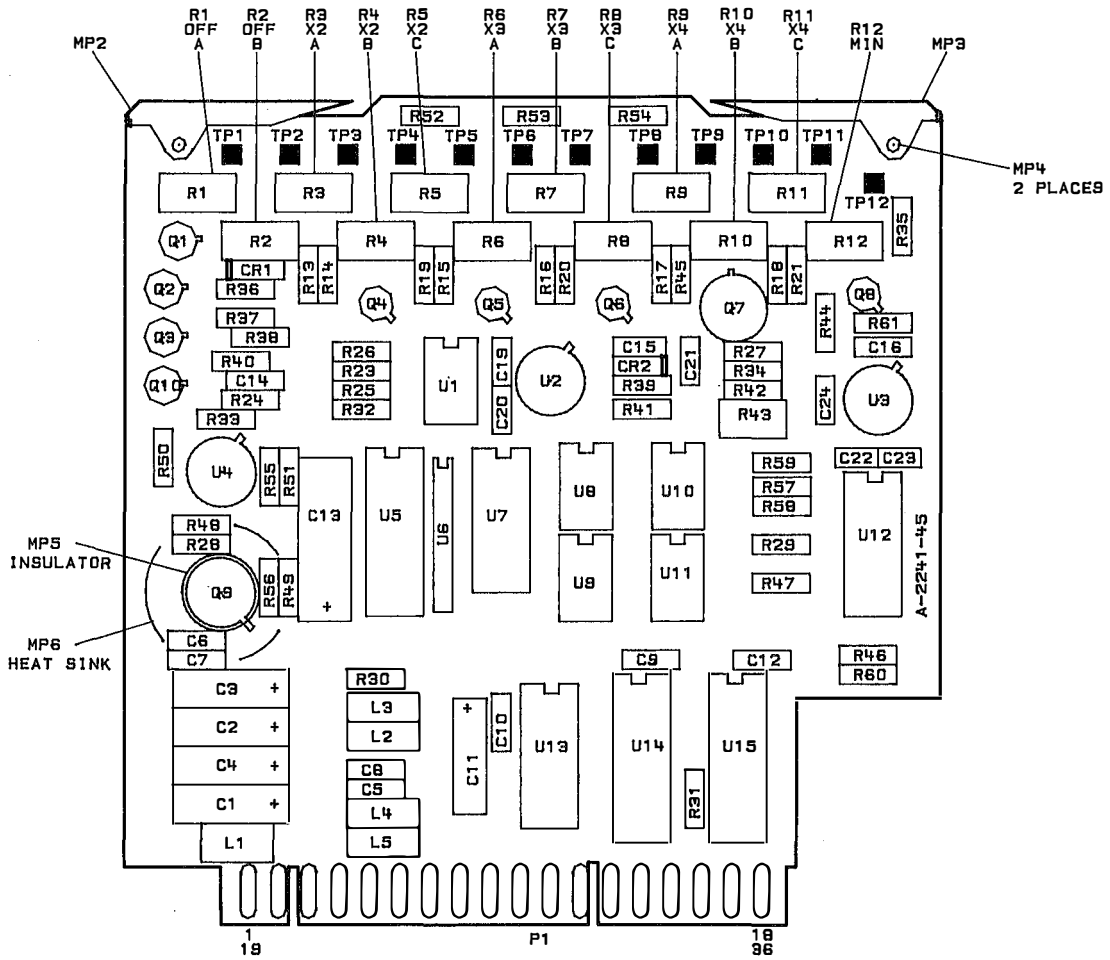


Figure 8I-27. A24 Attenuator Driver/SRD Bias, Component Location Diagram

A24 Attenuator Driver/SRD Bias P1 Pin I/O

A24

Pin	Mnemonic	Levels	Source	Destination
1 19	+20V SYTMHTR	+20V 0 TO +20V	XA52P1-16, 40 K	*L A62J18 PIN 8
2 20	SYTMTHRM HLBO	APPROX. −5V TTL (HIGH TRUE)	A62J18-9 XA27P1-46	K *C
3 21	+5.2V HLB1	+5.2V TTL (HIGH TRUE)	XA52P1-17, 18, 41, 42 XA27P1-16	*L *C
4 22	STAT10 HLB2	TTL (LOW TRUE) TTL (HIGH TRUE)	XA23P1-22 XA27P1-47	H *C
5 23	−10V RSTAT	−10V TTL (LOW TRUE)	XA53P1-12, 13, 31, 32 XA27P1-45	*L *H
6 24	1.4V/GHZ PIN BIAS	+1.4V/GHZ −4V TO +12V	XA28P1-7 G	*A A62J18 PIN 10
7 25	ATN COIL + SRO BIAS	+5V −10V THRU 2K TO +5V	L F	A62J20 PIN 6 A62J18 PIN 2
8 26	GNO GNO PLANE	0V 0V	A62 STAR GNO INSTRUMENT GNO	*L *L
9 27	ATNTH4 ATNAT4	OPEN COLLECTOR OPEN COLLECTOR	J J	A62J20 PIN 4 A62J20 PIN 10
10 28	ATNTH3 ATNAT3	OPEN COLLECTOR OPEN COLLECTOR	J J	A62J20 PIN 11 A62J20 PIN 5
11 29	ATNTH2 ATNAT2	OPEN COLLECTOR OPEN COLLECTOR	J J	A62J20 PIN 3 A62J20 PIN 9
12 30	ATNTH1 ATNAT1	OPEN COLLECTOR OPEN COLLECTOR	J J	A62J20 PIN 13 A62J20 PIN 2
13 31	SRO BIAS CONT HENOKICK	0 TO −5V (LEVELED) TTL (HIGH TRUE)	XA26P1-18 XA28P1-18	B H
14 32	OB9 OB11	TTL TTL	*H *H	* *I
15 33	OB10 WLEVEL	TTL TTL (LOW TRUE)	*H XA27P1-12	*I I
16 34	OB12 OB13	TTL TTL	*H *H	*I *I
17 35	SYTM GNO	0V	A62J18-13, 14, 15	*L
18 36	RGNO	0V	STAR GNO POINT	*L

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

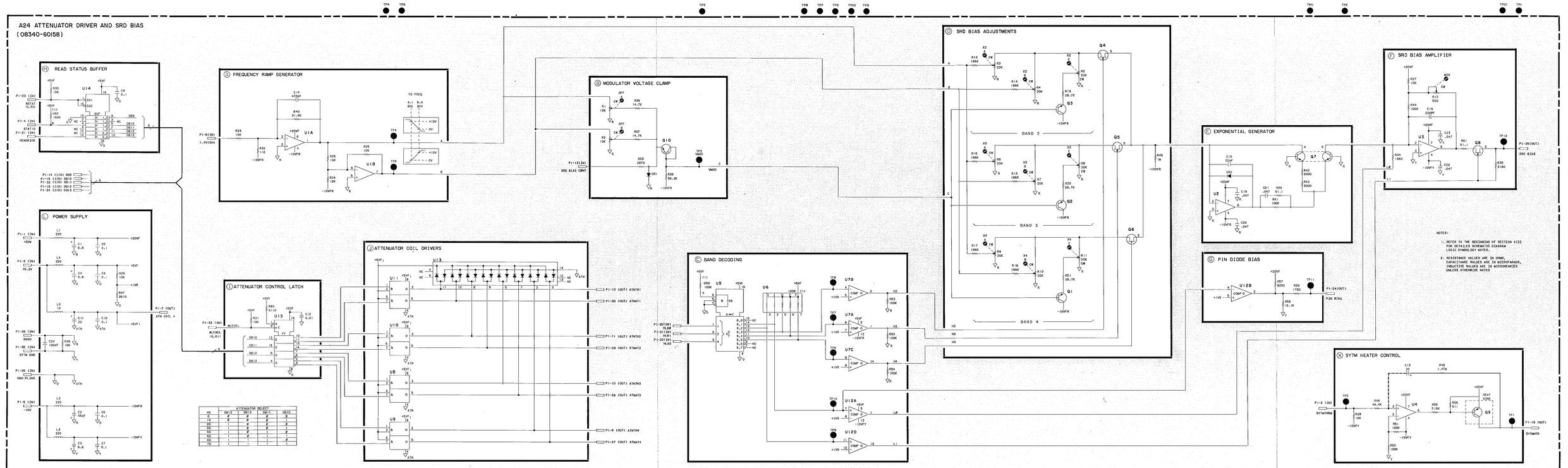


Figure 8I-28. A24 Attenuator Driver/SRD Bias, Schematic Diagram

A25 ALC DETECTOR, CIRCUIT DESCRIPTION

Introduction

Refer to Figure 8I-32, "A25 ALC Detector, Schematic Diagram".

The A25 ALC Detector assembly processes the voltage from either internal or external detectors, producing an output voltage proportional to the RF power level. This output voltage is then compared to a reference level voltage on the A26 Linear Modulator Assembly, and the resulting error is used to drive the RF modulators to control the RF leveling loop. Two "log converters"; one for the internal detectors, another for external detectors or power meters, convert the detected RF voltage to a signal proportional to RF power in dBm. In addition, an amplifier buffers this proportional signal and sends it to an analog-to-digital converter on the A27 Level Control board. This ADC converts the signal into digital information for the "POWER dBm" display. The reference level voltage is temperature-compensated on this assembly.

Internal Detector Log Converter A

The Internal Detector Log Converter receives the detected RF voltage and outputs a signal proportional to RF power level in dBm.

Crystal detectors characteristically exhibit two distinct regions of operation. At low power levels (less than 0 dBm), the detectors are in their square-law region. The detected output voltage then varies with the square of the RF voltage. At high power levels (more than +10 dBm), the detected output voltage varies linearly with the RF voltage. The log function converts the detected RF voltage into a DC voltage proportional to RF power, but to track the detectors accurately through both regions requires halving the gain at low power levels. Alternately, the gain can be doubled at high power levels. The Log Converter is a dual-slope design that accomplishes this with a smooth transition between square-law and linear regions.

Figure 8I-29, "Simplified Single-slope Log Converter Diagram", illustrates a simplied single-slope log converter. The log function is accomplished by Q6A using the transistor characteristic that collector current is the exponential of base-to-emitter voltage. U1 amplifies the detector voltage, driving the emitter of Q6A until the collector current sensed through R21 equals the input voltage. Q6A's emitter voltage is then the log of the input voltage, which passes through Q6B (wired as a diode) to the output.

To make a dual-slope Log Converter, a second pair of transistors with bias current sources is added, as in Figure 8I-30, "Simplified Dual-slope Converter Diagram". Bias currents Ib1 and Ib2 are constant and nearly equal. Q6A and Q6B still carry the logging current Iin;

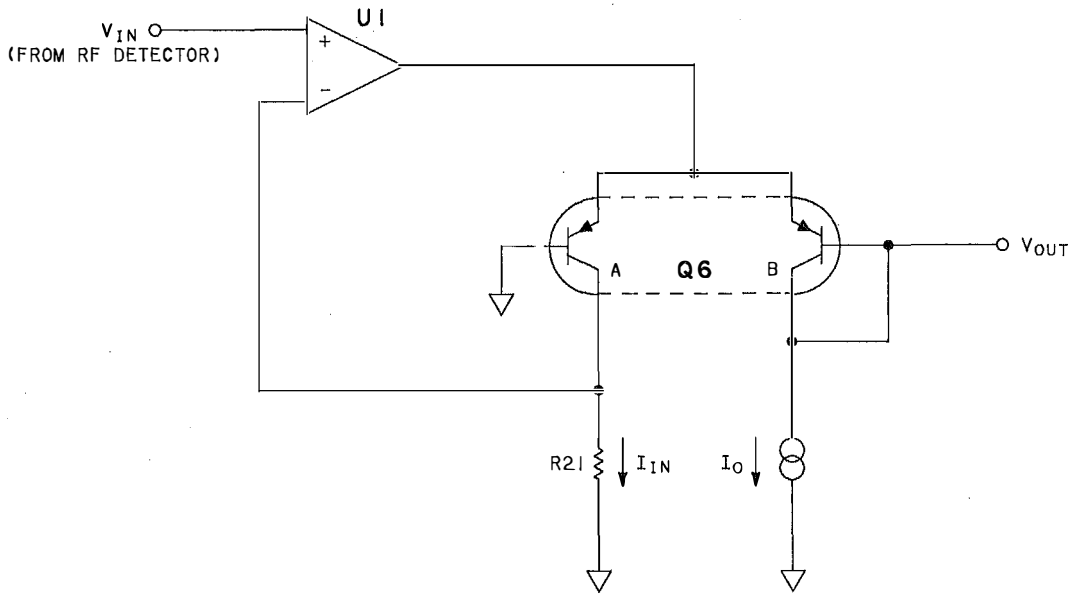


Figure 8I-29. Simplified Single-slope Log Converter Diagram

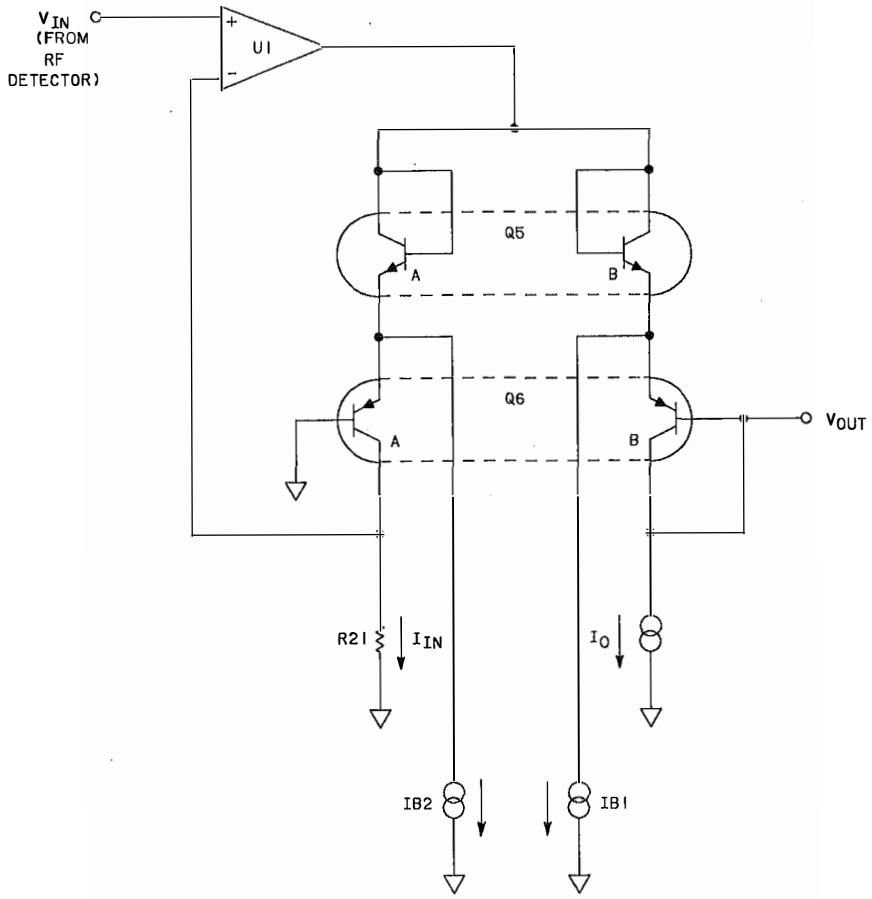


Figure 8I-30. Simplified Dual-slope Converter Diagram

however, Q5A and Q5B now carry Ibl and Ib2 as well. For low power levels (square-law region), assume Iin is much less than Ibl and Io is much less than Ib2. (Iin = Vin/R21) Then Q5A and Q5B are carrying essentially identical currents, and their base-to-emitter voltages are identical. In effect, then, the emitter of Q6A is at the same voltage as the emitter of Q6B, and the circuit acts like the single-slope logger of Figure 8I-29, "Simplified Single-slope Log Converter Diagram". For high power levels (linear region), Iin is much greater than Ibl. Now Q5A and Q6A both carry the same current Iin (Ibl can be ignored), and the base voltage of Q5A varies twice as much as the emitter of Q6A (both base-to-emitter junctions contribute to the logging function). Thus, the gain of the logger is doubled when the detectors are in their linear regions, and the Log Converter outputs a voltage proportional to RF power in dBm over a wide range of power levels encompassing both square-law and linear regions.

Internal Detector Log Converter **A:** Q1 and Q2 select the A12 Band 0 Detector or A11 Band 1-4 Detector when appropriate. U2D and U2C, through R33 "L-20" and R34 "H-20", add minute offsets in Band 0 and Band 1-4 respectively to adjust low RF power levels. U1 and Q3 form a low drift, high gain DC amplifier to drive the logger. Q12, Q13, Q14, and Q15 form a high-speed differential AC amplifier to improve the loggers high-frequency response. Q4 sums the DC Amplifier and AC Amplifier to drive current through the logger. Q7 biases Q4. The logger consists of Q5 and Q6, and functions like the simplified dual-slope logger described in Figure 8I-30, "Simplified Dual-slope Converter Diagram". R24 is added to compensate for bulk resistance in Q5A and Q6A at high currents. Q8 and Q9 provide the adjustable bias currents Ibl and Ib2, respectively. U2B and U2A turn on the logger bias for Band 0 and Band 1-4 respectively. R38 ("L+10") and R108 ("LOFS") adjust the bias for Band 0. R39 ("H+10") adjust the Band 1-4 bias. A thermistor mounted inside A12 Band 0 Detector changes the bias current Ibl to improve temperature tracking. Q16A provides the bias current Io. Q16B serves to clamp the logger's negative excursions when pulse modulation turns the RF OFF. The clamp voltage is approximately -0.12 Vdc, but varies slightly with changes in power level, reference power level, and temperature to minimize recovery time. Q16B is normally non-conducting.

X5 Amplifier B

Q17, Q18, Q19, and Q23 form a discrete differential amplifier to buffer the Log Converter's high-impedance output. In addition, the LVLCOR (level correction) signal from the A27 Level Control Assembly is summed together with the detected voltage.

Sample/Hold C

The Sample/Hold circuit stores the detected RF level when the RF power is off during pulse modulation. Sampling switch Q25, holding capacitor

C25, and buffer U8 are the key elements. Sampling switch Q25 is controlled by the A21 Pulse Modulator assembly through drivers Q30 and Q31. When Q25 goes open ("Hold" mode), some charge on C25 is lost through gate capacitance. C24 injects a charge into C25 to compensate for this charge loss, adjustable by R58 "BAL". The charge lost through Q25 during switching depends on the gate voltage excursion, which in turn depends on the sample/hold input voltage. Q24 monitors the output voltage and adjusts the excursions of Q25's gate so that the charge lost during switching is independent of power level. During bandswitching, the logger may produce negative transients large enough to accidentally turn on Q25; CR4 and CR5 clamp these excursions. Note that R61 will keep Q25 on if the A21 Pulse Modulator Assembly is removed.

Level Meter Amplifier D

Q20 and U4B buffer and filter the sample/hold voltage level. The amplifier has a voltage gain of approximately 6.6, and a low-pass filter cutoff frequency of only 5 Hz. Temperature sensitive resistors R64 and R66 track the gain drift of the logger. U5B buffers the signal to be read by the ADC on the A27 Level Control assembly. The microprocessor can then monitor the RF power level and display it on the front panel POWER dBm display.

External Log Converter E

If the RF power level is monitored externally though the "LEVELING EXT INPUT", the External Detector Log Converter provides the logging function similar to the log converter in Block **A**. U10 and U6 form an "absolute value converter" to permit both positive and negative detectors to be used. U10 is a non-inverting amplifier with gain of 2.2, so when the "EXT INPUT" is positive, U10 pin 6 goes positive. U6 pin 6 will then go negative, turning CR9 on and configuring U6 like an inverting amplifier to drive the logger through R86. When the "EXT INPUT" is negative, U10 pin 6 goes negative, causing U6 pin 6 to go positive and turn CR9 off. Thus, U6 is effectively removed from the circuit, and U10 drives the logger through R81, R85, and R86 directly. Resistor values are used to make the current to the logger the same for both positive and negative voltages. R80 "EX-" adjusts the voltage offset of U10; R84 "EX+" adjusts the voltage offset of U6.

CR6 prevents large differential voltages from occurring across U6's inputs when it is open-loop (negative ext. inputs). Large differential inputs will turn on U6's internal protection diodes, loading the junction of R81-R85.

U7 and Q22 form an inverting log converter. U7 drives the emitters of Q22A until the collector current equals the input current. (The input current may be driven by either U10 or U6.) Q22B is wired like a diode, and passes the base-to-emitter voltage out. Q21B provides bias

current for Q22B. Q21A will clamp the logger's negative excursions to approximately -0.3 Vdc, and is normally turned off. R88 compensates for bulk resistance in Q22A at high logger currents.

Note that when external detectors are used, the Sample/Hold is not effective during pulse modulation. Furthermore, the front panel POWER dBm display will continue to display the internally detected power level (instrument output power), not the externally detected power level.

Function Switches and External Detector Frequency Compensation F

U3 buffers the External Detector Log Converter, with a DC voltage gain of approximately 10. Open-collector drivers U9 and FET swtiches Q27 and Q28 select the internal or external detector signal, as appropriate, for use on the A26 Linear Modulator assembly. Q29 adjusts the frequency compensation for external meter leveling. The U9 open-collector FET drivers pull down to -10 Vdc to turn the FETs off, and float HIGH to turn the FETs on. Refer to Table 8I-1 for a function select truth table.

Level Reference Temperature Compensation G

To compensate for gain drift in the log converters, the reference voltage is made to change with temperature. This is accomplished by inverting amplifier U4A which has a temperature-dependent feedback resistor R101. The temperature-compensated reference voltage (TCREF) goes to the A26 Linear Modulator board where it is summed with AM and marker inputs, then compared to the output of the A25 ALC Detector board.

Power Supply H

LC filtering removes noise from the +20VF and -10VF lines for use on the A25 ALC Detector Assembly. Additional RC filtering keeps +20VL and -10VL extra clean for use in the internal logger. The +1.5VF is the TTL reference voltage for the comparators.

Table 8I-1. Function Select Truth Table

Leveling Mode		Q27	Q28	Q29
Internal		ON	OFF	OFF
External	Crystal Detector	OFF	ON	OFF
	Power Meter	OFF	ON	ON
Unleveled (Shift Meter)		OFF	OFF	OFF

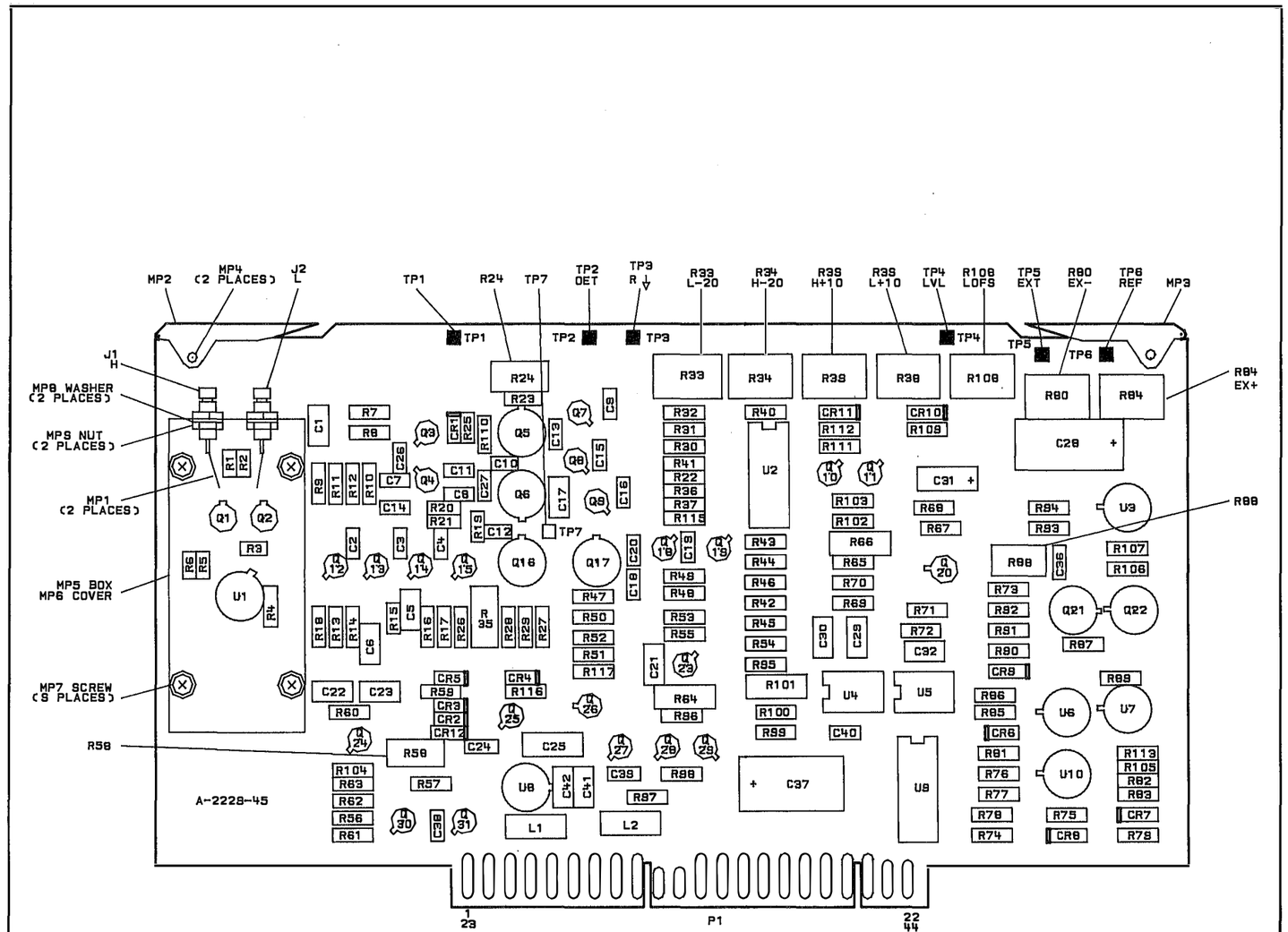


Figure 8I-31. A25 ALC Detector, Component Location Diagram

A25 ALC Detector P1 Pin I/O

A25

Pin	Mnemonic	Levels	Source	Destination
1 23				
2 24	DET S/H + DET S/H −	+4.5/+3.5V +3.5/+4.5V	XA21P1-3 XA21P1-21	C C
3 25	HPLSEN	TTL (HIGH TRUE)	XA26P1-2	*NOT USED
4 26	THERM 1 THERM 2	−1V TO −8V −10V	A62J34-3 A62J34-1	A A
5 27	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*H *H
6 28	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*NOT USED *NOT USED
7 29	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*H *H
8 30				
9 31	GND GNO	0V 0V	A62 STAR GND A62 STAR GND	* *
10 32	GND DETOUT	0V −30mV/dB, 0V = 0dBm	A62 STAR GND F	* XA26P1-10
11 33	DETLVL	−200mV/dB, 0V = 0dBm	D	XA27P1-29
12 34	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*H *H
13 35	LVLREF TCREF	0.2V/dB, 0V = 0dBm −200mV/dB, 0V = 0dBm	XA27P1-30 G	G XA26P1-12
14 36	LVLCOR HMTR	+1.25dB/VOLT, 0V = 0dB TTL (HIGH TRUE)	B XA26P1-13	XA27P1-62 A F
15 37	LHET	TTL (LOW TRUE)	XA27P1-20	*A
16 38				
17 39	LDETBW	TTL (LOW TRUE)	XA26P1-9	*NOT USED
18 40				
19 41				
20 42	HINT	TTL (HIGH TRUE)	XA26P1-42	F
21 43	EXDETR	0V	*	E
22 44	EXDET	0.5mV − 2V	A62J16 SMC CENTER	E

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

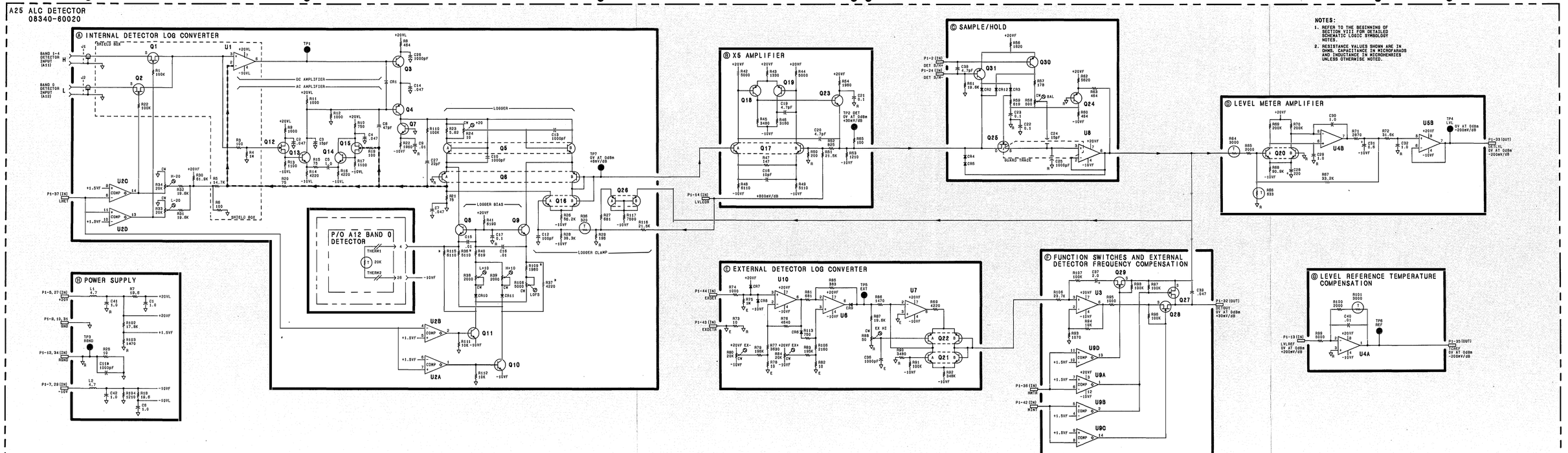


Figure 8I-32. A25 ALC Detector, Schematic Diagram

A26 LINEAR MODULATOR, CIRCUIT DESCRIPTION

Introduction

The A26 Linear Modulator assembly compares the detected RF power level against the level reference voltage, and drives the RF modulators to correct any errors. This closes the ALC loop and levels the RF power. The amplitude modulation (AM) input is logged and added to the level reference on this assembly.

AM Log Converter A

U12 buffers the front panel "AM MODULATION INPUT" with approximately unity gain. U1 and Q24 form the log converter. (See Figure 8I-33, "External AM Log Converter, Simplified Diagram", and Figure 8I-34, "HLBW Algorithm".) U12 drives a current through R23 to U1; a constant bias current Ib (through R26) establishes the operating point of the logger. U1's output will drive the emitter of Q24A until its collector current equals the total input current. The base-to-emitter voltage is then logarithmically related to the input voltage. This voltage is sensed through Q24B to the output. U2 buffers the log converter's high output impedance, and has a voltage gain of about 10. FETs Q23 and Q1 switch out the log converter when AM is not selected.

ALC Loop Integrator B

The ALC loop summing node is at the source of FET Q16. At this point, the detected RF power level voltage (DETOUT) is summed with the reference power level voltage (TCREF). When the loop is closed and leveled, these signals should be equal and opposite, thus perfectly cancelling. If they do not cancel, the error current is integrated by U8 and changes the RF modulation level to correct the power level. The marker pulses (HMRKR) and logged external AM (if enabled) are also added to the summing node.

U8 is the main ALC amplifier, forming an integrator with capacitor C6 (ALC Loop BW = 100kHz). C15 is switched in parallel with C6 by FET Q20 in any externally leveled mode (ALC Loop BW = 20kHz). Under a variety of conditions, C7 is also connected in parallel with C6 (ALC Loop BW = 7 kHz; see Figure 8I-34, "HLBW Algorithm"). Q17 clamps the negative voltage excursions of U8 to about -3.9 V when the loop goes unleveled. Likewise, Q18 clamps the positive excursions to about +0.5 V. U11B and Q25 alter the bias on these clamps when HRFON goes LOW to turn the RF power off, clamping the MODLVL voltage at about -3.0V. When external power meter leveling is selected, FET switch Q30 is closed to put C23 across Q25's control line. This makes the "turn-on" time at bandswitches or beginning of sweep very slow and avoids ALC overshoot due to slow power meter response times. (Leveled ALC Loop BW is not affected.) Q10 is normally off, but can be turned on to shunt R17

across the integrating capacitors C6, C7, and C15. This makes U8 an inverting amplifier instead of an integrator for the open-loop mode. Q10 also parallels R3 with R58, doubling the reference sensitivity to achieve a wide control range when open-loop.

Overmodulation/Unleveled Detectors C

The MODLVL voltage will remain within certain bounds when the RF power is leveled. If MODLVL exceeds these bounds, comparators detect the condition and send the information to the microprocessor. Q27 and U14 detect excessive amplitude modulation. When MODLVL falls below about -3.6 V, Q27 turns on, trips U14, and sends LOMD to A27 for the microprocessor to read. Likewise, Q26 and U13 detect the MODLVL when the RF modulators are no longer attenuating and the RF power is unleveled. If MODLVL rises above about +0.2 V, Q26 will turn on and trigger U13 to send LUNLVL to A27. Both functions are disabled by Q28.

Jumper W1 allows instruments with a serial prefix of 2320A and above to be immune to a problem where the UNLEVELED annunciator may go ON briefly after the end of sweep. This problem occurs because the YO and the SYTM may not track after end-of-sweep. If they do not, the power to the leveling detector may decrease. The ALC loop will try to compensate for the decrease in power and generate an UNLEVELED condition.

W1 must be in position B for instruments with a serial prefix of 2320A or higher. This position allows HSP (HIGH SWEEP) to turn on Q28, directly disabling the OVERMODULATION/UNLEVELED circuitry at end-of-sweep.

W1 must be in position A for instruments with a serial prefix of 2319A or before. This is because HSP does not go to the A26 assembly in these units. Instead, the processor turns on Q28 to disable OVERMODULATION/UNLEVELED via COMPEN. The problem occurs because during sweep the processor is disabled (to reduce system noise). When the processor activates at end of sweep, it receives a service request (LSRQ). After determining the cause of the service request from A59 Block I, the processor programs COMPEN to disable the OVERMODULATION/UNLEVELED Detectors. By the time the processor has done all this, however, an UNLEVELED condition may have already occurred. This problem only affects the Maximum Leveled Power Test in Section IV, PERFORMANCE TESTS. Actual instrument Performance is not affected.

ALC Modulator Switch D

FET swtiches Q21 and Q22 select either the Band 0 (P/O A8) or Band 1-4 (P/O A16) RF modulators to be driven by the Modulator Driver. In Band 0, U4PW14 goes LOW, causing U11D pin 14 to go to ground to turn Q21 ON. At the same time, U11C pin 8 goes HIGH to turn Q22 OFF. Note that U11C also turns the HIGH band switch (P/O A16) off in Band 0. (Refer

to the Figure 8I-42, RF Section Schematic Diagram.) In Bands 1-4, the situation is reversed: Q21 is off, and Q22 is on. R62 sinks a fixed current from the exponential current mirror in Band 0, as described above. In Band 1, R61 sinks this current; in Bands 2-4, R60 in parallel with R61 sinks the bias current. In bands 1-4, Q31 and R56 source 25 mA to the Band 0 Pulse Modulator to help reduce 3.7 GHz spurious outputs.

ALC Loop Function Switch Drivers E

U15 latches digital information from the microprocessor to control the major ALC functions. Many of U15's outputs are used on other boards in the ALC loop. HMTR and HINT determine the primary leveling mode. These two lines, with decoders U10C and U10B, drive comparators to control the Main ALC Amplifier. See Table 8I-2 for their functions. The other lines and comparators control functions for loop bandwidth, enable amplitude modulation, and enable the OVERMODULATION/UNLEVELED comparators. U9C controls the A12 Band 0 Detector bandwidth.

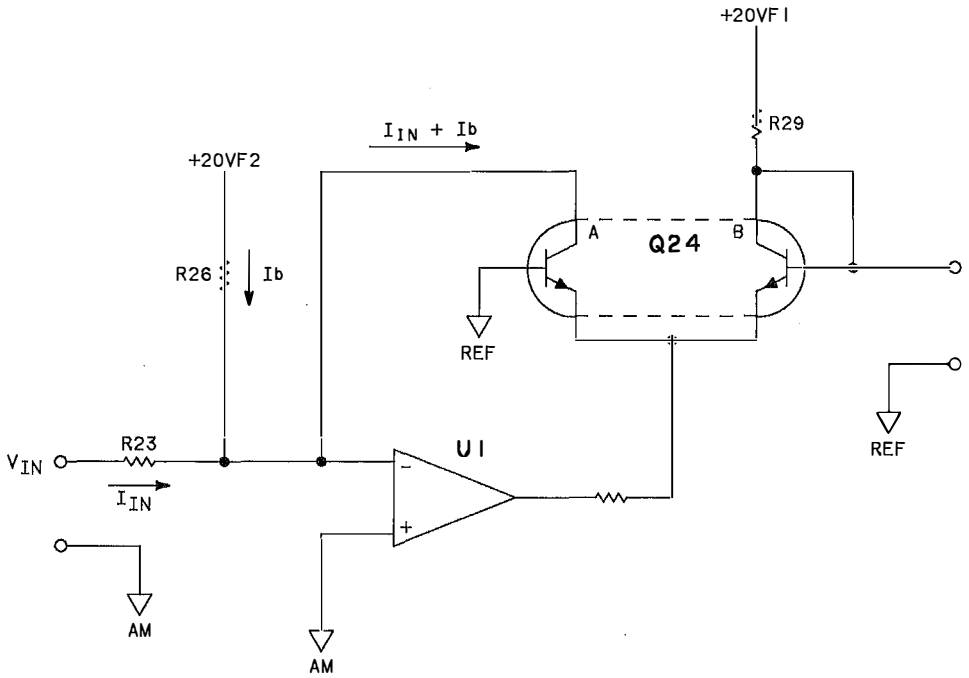
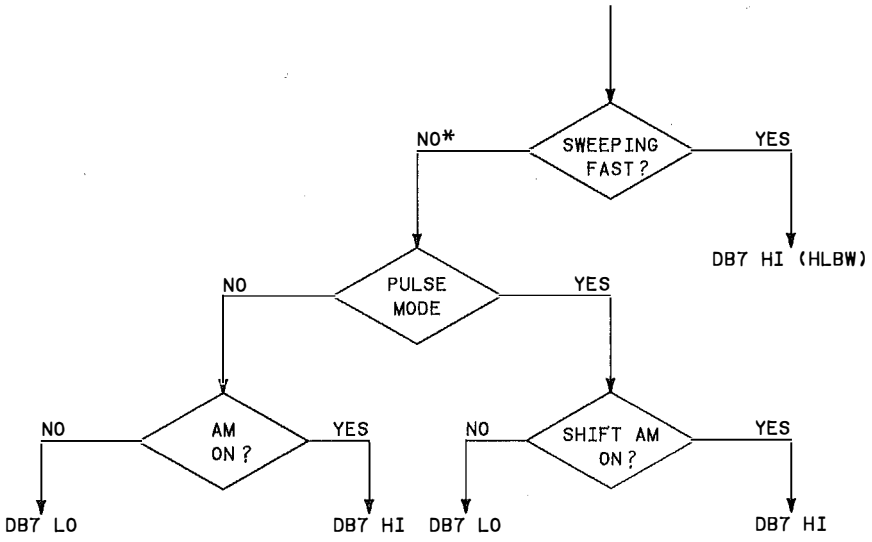


Figure 8I-33. External AM Log Converter, Simplified Diagram



FAST SWEEP: <5 SEC

*INCLUDES MANUAL & CW

SHIFT AM ACTIVATES AM

TURNING AM OFF DE-ACTIVATES SHIFT AM

Figure 8I-34. HLBW Algorithm

Table 8I-2. HMTR and HINT Functions

HMTR	HINT	
	Low = 0	**High = 1**
High = 1	External Power Leveling	"Open-Loop"
Low = 0	External Crystal Leveling	Internal Leveling

Band Switch Drivers F

U4 decodes the band information from HLB0, HLB1, and HLB2. Each output goes LOW for the selected band, causing the output of each respective comparator to go HIGH for the selected band. U10A senses the Band 0 and Band 1 lines, but actually drives U11A pin 1 HIGH during Bands 2-4 to alter the modulator bias for the multiplying bands.

ALC Modulator Driver G

The ALC loop gain is adjustable for each band separately. Q2, Q3, Q4, Q5, and Q6 select the MODLVL to pass through an adjustment for Band 0 through 4 respectively. U7 buffers this voltage for Bands 2-4 and sends it to the A24 assembly for use in biasing the Step Recovery Diode in the A13 SYTM. Each of the five adjustments drives the emitter of Q15B one at a time. Q15B forms a common-base current summing node. Q7 and Q8 form an "exponential current mirror" to drive current through the RF modulators.

The exponential function is desirable to linearize the RF modulators' attenuation characteristics. (See Figure 8I-35, "Modulator Characteristic".) The RF attenuation of the modulator is a very non-linear function of drive current. If plotted on log-log paper, however, the plot is straight over the high current end of its range. Therefore, converting the MODLVL voltage to an exponential current would best fit the modulators' characteristics at high attenuation levels. To track the modulator curve better at low attenuation, simply subtracting a fixed current from the exponential current mirror's output will "bend" the modulation curve on log-log paper. This gives the desired result; RF attenuation in dB is proportional to the MODLVL voltage. In Bands 2-4, non linearities in the power transfer characteristics of the A13 SYTM require additional modulator drive shaping.

R54 and Q15A bias Q15B's emitter at about 0.0V. Q15B is a common-base current summing node. Q15's collector current is the same as the emitter current. Q8, with R85 and R55, form an exponential current mirror; current through Q8A causes a voltage drop across R85 and R55. This causes Q8B's base-to-emitter voltage to change linearly, causing Q8B's collector current to change exponentially. Q7 is added in a Darlington configuration to buffer Q8B. R86, R87, R88 "MO" (Modulator Offset), and R44 provide a bias current to the exponentiator input (Q15 emitter) so that when "mod level" (TP3) is at 0 volts, the exponentiator will be outputting some current. This current equals the current being shunted from the modulators by R61 and R62. Q14 increases the bias in bands 2 - 4, compensating for the increased shunt current through Q29 and R60 in those bands.

Power Supply H

The power supply filtering consists of ordinary LC filters. R80 and R81 generate the +1.5VF reference voltage for TTL comparators.

Slow Rise Time Pulse Driver I

Fast rise time pulse modulation produces a very broad spectrum of RF Harmonics, resulting in errors with some measurements. For this reason, the 8340A has a pulse modulation mode implemented through the linear modulator. This mode produces pulses with approximately 2 usec rise and fall times. The mode is activated by pressing **[SH] [PULSE]**, and hooking the pulse input to the AM jack. The pulse input requirements are: -6V = off, > -2V = on. This works with the +-6V modulator drive produced by the 8755C or 8756A.

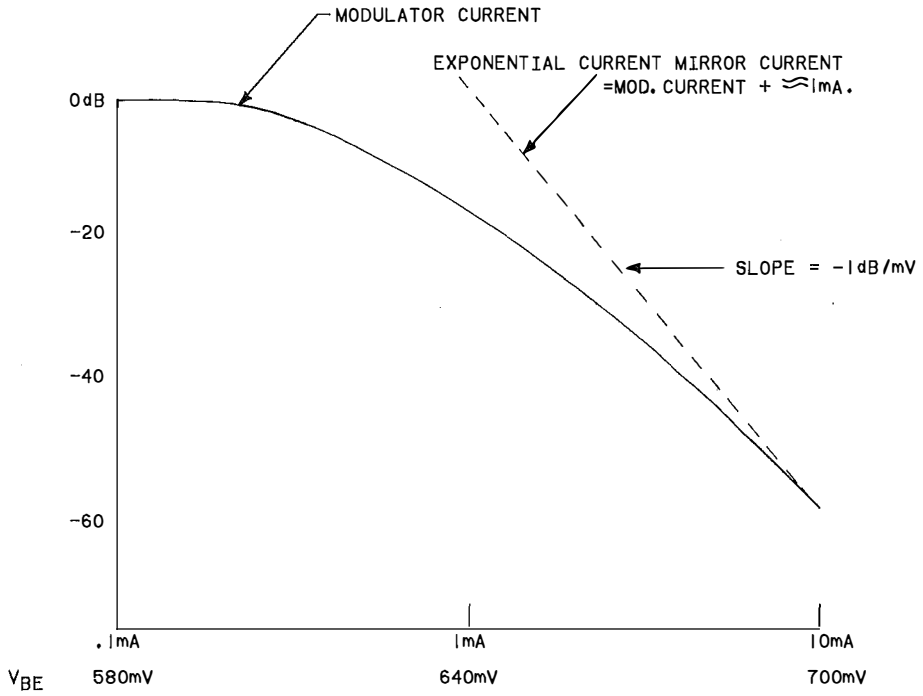
When **[SHIFT] [PULSE]** has been pressed, the front panel AM light comes on and the AM signal (U9 pin 13) goes low, disabling normal AM circuitry. HSRT goes high, forcing U3 pin 1 low, thereby enabling the Q32/Q9 comparator circuit. When the AM input voltage is more positive than -3V, Q32 is on and Q9 is off. When the AM input voltage becomes more negative than -3V, the base of Q32 is pulled negative through CR3, causing the comparator to switch states and turn Q9 on. This pulls current through CR9, CR10, and CR14.

With no current through CR14 (AM input more positive than -3V) the network R95-R98, L7, and CR13 does nothing because it is connected from ground to a point at ground potential (emitter of Q15, located in Block **G**). When the AM input is more negative than -3V and Q9 is on, current is drawn through CR14, L7, R96, R95, and the emitter of Q15. Removing current from the emitter of Q15 causes increased current to the linear modulator, causing the RF power to drop by at least 40 dB. L7 slows this transition producing the 2 usec fall time.

When the AM input is more positive than -3V the comparator changes states, leaving Q9 off. This change in current through L7 causes an inductive kick which forward biases CR13. This positive pulse through R95 into Q15's emitter speeds the turn-on of the modulator, which would otherwise have a long rise time due to its long carrier life.

When the AM input goes more negative than -3V (to shut off the RF), it is necessary to open the integration gate Q16, thereby holding the MODLVL voltage at a constant value. When Q9 conducts, some of its collector current goes through CR10 and CR9 to the base of Q12, opening the integration gate. When the input goes

positive, the inductive kick from L7 back biases CR10. C36 discharges slowly, delaying the closing of the integration gate. This assures that the RF has reached the proper level.



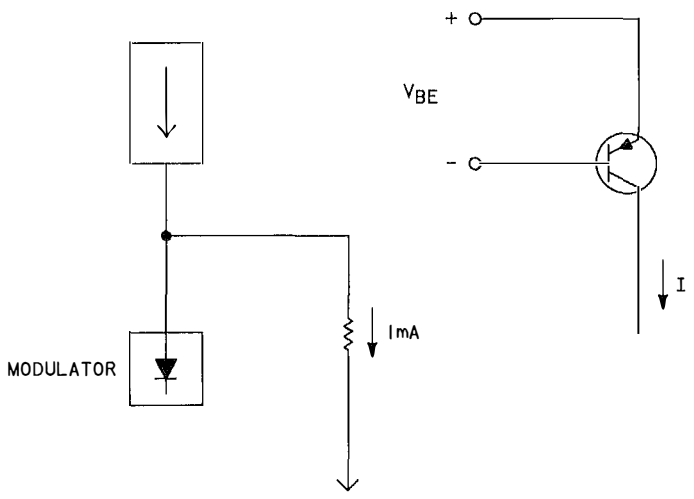


Figure 8I-35. Modulator Characteristic

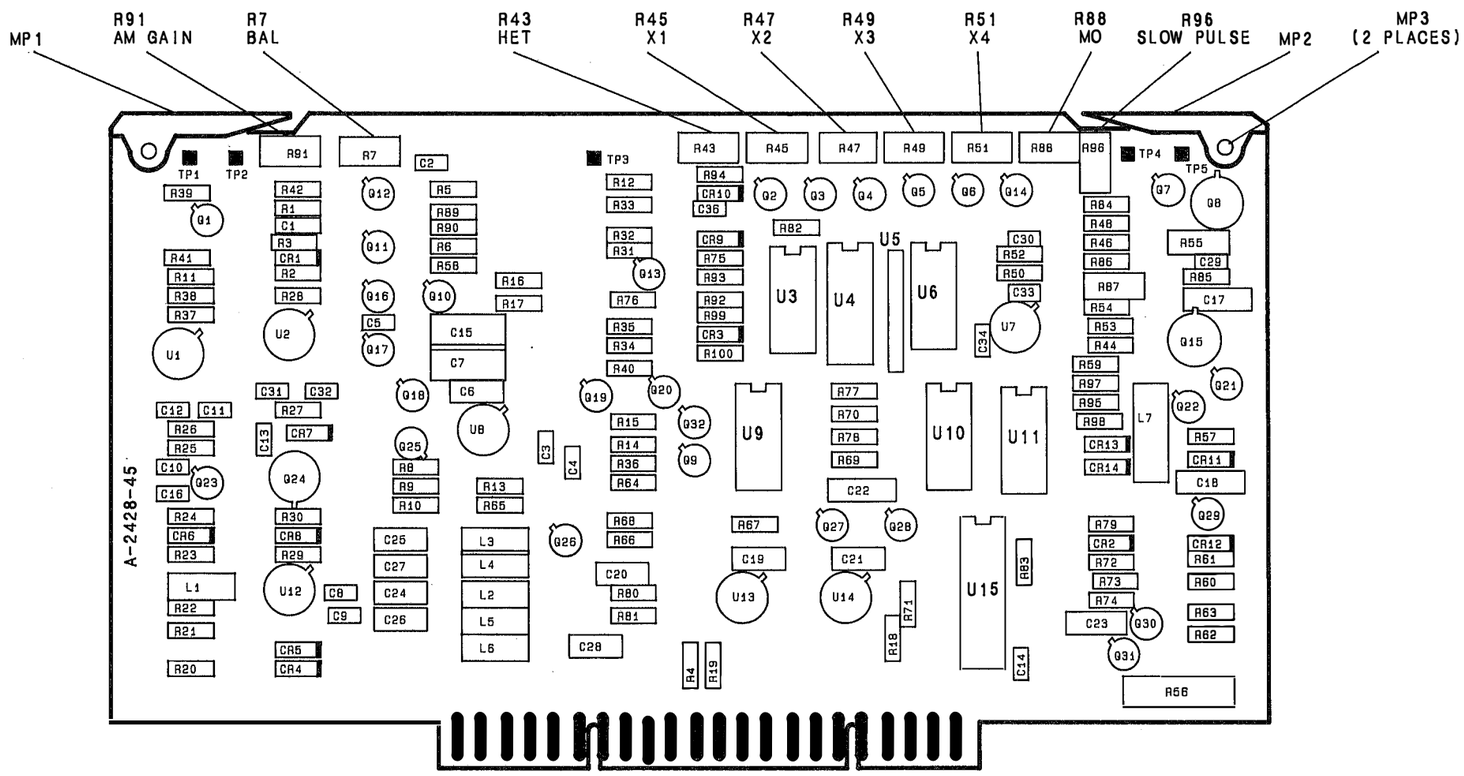


Figure 8I-36. A26 ALC Modular Component Location Diagram

A26 Linear Modulator P1 Pin I/O

A26

Pin	Mnemonic	Levels	Source	Destination
1 23	LMODHLD LHIBND	TTL TTL (LOW TRUE)	XA21P1-2 D	B A62J19 PIN 15
2 24	HPLSEN HRFON	TTL (HIGH TRUE) TTL (HIGH TRUE)	E XA57P1-105	* *B
3 25	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*H *H
4 26	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*H *H
5 27	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*H *H
6 28	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
7 29	HSP HLB0	TTL (HIGH TRUE) TTL (HIGH TRUE)	XA57P1-13 XA27P1-46	* *F
8 30	LOMD HLB1	TTL (LOW TRUE) TTL (HIGH TRUE)	C XA27P1-16	XA27P1-48 *F
9 31	LDETBW HLB2	TTL (LOW TRUE) TTL (HIGH TRUE)	E XA27P1-47	*XA25P1-39 *F
10 32	DETOUT MODLVL	−30mV/dB, 0V = 0dBm 0V TO −3V (LEVELED)	XA25P1-32 B	B XA27P1-61
11 33	RGND HLBW	0V TTL (HIGH TRUE)	STAR GND POINT E	*H XA21P1-6
12 34	TCREF RGND	−200mV/dB, 0V = 0dBm 0V	XA25P1-35 STAR GND POINT	B *H
13 35	HMTR DB11	TTL (HIGH TRUE) TTL	E *	XA25P1-36 *E
14 36	LHET LUNLVL	TTL (LOW TRUE) TTL (LOW TRUE)	XA27P1-20 C	*NOT USED XA27P1-52
15 37	DB0 DB1	TTL TTL	XA60P1-20 XA60P1-76	*E *E
16 38	DB2 DB3	TTL TTL	XA60P1-21 XA60P1-77	*E *E
17 39	DB4 DB6	TTL TTL	XA60P1-22 XA60P1-78	*E *E
18 40	SRD BIAS CONT DB7	0 TO −5V (LEVELED) TTL	G XA60P1-79	XA24P1-13 *E
19 41	AM IN AM RTN	±1V MAXIMUM 0V	A62J15-SMC CENTER *	A A
20 42	MODHI HINT	CURRENT SOURCE TTL (HIGH TRUE)	D E	A62J13-SMC CENTER XA25P1-42
21 43	MOD RTN HMRKR	0V TTL (HIGH TRUE)	D XA57P1-2, 12	A62J13-SMC SHIELD B
22 44	MODLO WMOD	CURRENT SOURCE TTL (LOW TRUE)	D XA27P1-59	A62J14-SMC CENTER *E

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

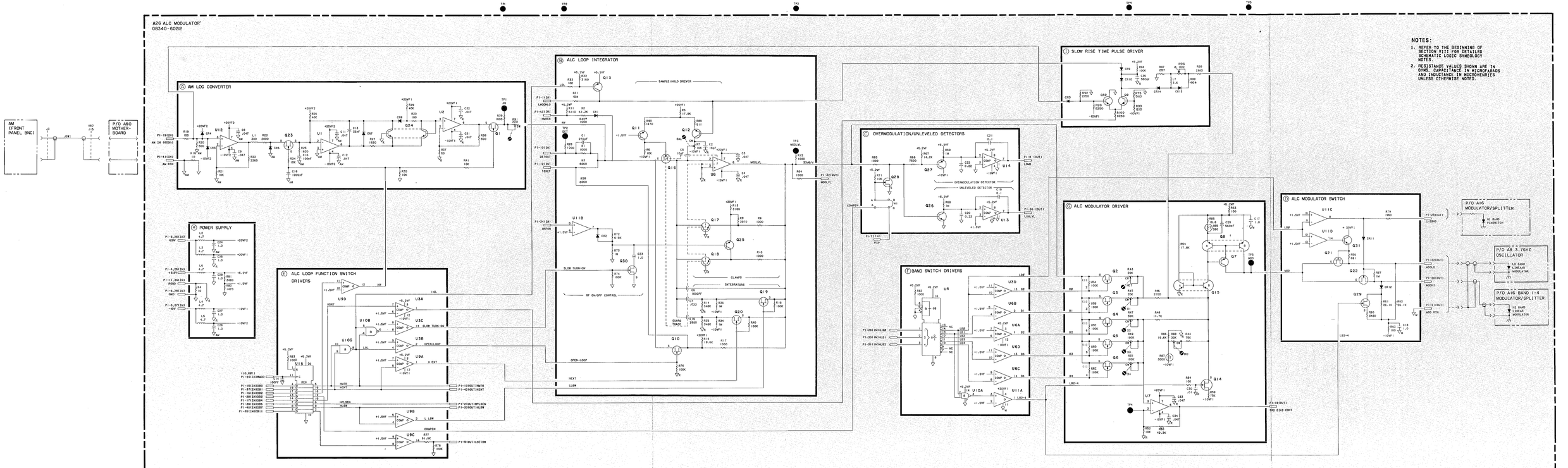


Figure 8I-37. A26 ALC Modulator, Schematic Diagram

A27 LEVEL CONTROL ASSEMBLY, CIRCUIT DESCRIPTION

Introduction

The A27 Level Control board performs the following functions:

- Flatness Compensation - provides error compensation to the ALC as a function of frequency.
- Power Sweep Control - uses the RF Sweep to generate a processor-controlled power level sweep.
- ALC Reference Generator - controls the reference voltage for the A26 Linear Modulator's Level Control Circuits.
- Test ADC - (Analog-to-Digital Converter) monitors any one of several dc levels (modulation level, sweep voltage, ALC level, etc.) via an analog multiplexer. The ADC sends a digital equivalent of the chosen dc voltage to the instrument processor.

Band Switch Control A

A 74LS175 latch (U28) is used to latch data bits 0,1 & 2 off of the data bus when WBAND strobe (U27 pin 13 Block **B**) goes LOW and then HIGH. These latched data bits produce the encoded latched band information HLB0 (U28 pin 2), HLB1 (U28 pin 7) and HLB2 (U28 pin 10).

LHET is decoded by using a NAND gate as a dual negative input OR gate (U26B). The inverting outputs of latch (U28) HLB1-not (U28 pin 6) and HLB2-not (U28 pin 11) go to this NAND gate and cause its output (LHET U26 pin 6) to go HIGH when either input (U26 pin 4 or 5) goes LOW.

Address Decoding B

The I/O strobe decoding consists of two 74LS138 3 line to eight line decoders (U20 & U27) and one NAND gate (U26A) connected as an inverter. These two decoders decode address lines A0 through A4 and SIOA I/O strobe to produce input and output strobes for the RF section of the instrument.

20 GHz Breakpoint Slope Compensation C

The 20 GHz breakpoint is used to compensate for directional coupler forward losses and coupler detector coupling losses which occur beyond 20 to 23 GHz.

The breakpoint circuit is exactly the same as the 9 GHz

breakpoint except the breakpoint will occur when the voltage on the V/GHz line is -10.0(R6/R7+R8).

The output of this breakpoint circuit is connected to the V referance input of a NE5018 DAC (U10 pin 14). This DAC is exactly as described for the attenuator slope compensation DAC or 9 GHz Breakpoint DAC.

9 GHz Breakpoint Slope Compensation D

At about 9 GHz the detector's specifications indicate that it could have either increasing or decreasing output versus frequency. Since the detector's specifications indicates that either situation could occur from unit to unit, a bipolar breakpoint was placed at approximately 9 GHz.

When creating a correction to the level reference voltage to compensate for detector losses, the following must be considered: If the output of the detector decreases for any reason, the ALC circuitry will increase the output power to force the detector output to be the same. So to compensate for detector losses we must create a correction that decreases the level reference.

The location of the breakpoint (the frequency at which the correction begins to occur) is controlled by an amplifier with diode feedback paths. An op-amp (U4B) has a diode (CR3) in series with its output (U4B pin 7) so whenever its output voltage is less than zero volts the diode will be reverse biased. Furthermore, a diode clamp (CR2) clamps its output (pin 7) to be no more negative than one diode drop. When its output (pin 7) is positive, the series diode (CR3) is forward biased, the diode clamp (CR2) is reverse biased and the op-amp is now in a standard inverting gain configuration with a 10K feedback resistor (R5). The V/GHz line (-0.25 V/GHz) and an offset are summed into the inverting input of the op-amp (U4B pin 6). The offset resistor (R3 + R4) is connected to the +10.00 volt precision reference. The input resistor (R2) is connected to the V/GHz line. As long as the current provided by the offset resistor (R3 +R4) is greater than the current sunk by the input resistor (R2), the output of this circuit will remain at 0 volts. As soon as the current sunk by the input resistor is greater than that provided by the offset resistor, the output of the circuit will begin to increase at a rate of +0.25 V/GHz since the amplifier has a gain of 1. The breakpoint will occur when the voltage on the V/GHz line equals 10.0 V(R2/R3+R4). The offset resistor is a fixed resistor in series with a pot so the point at which the breakpoint occures can be adjusted over some range.

The output of this breakpoint circuit is connected to the V reference input of a NE5018 DAC (U9 pin 14). This DAC is exactly

the same as the attenuator slope DAC. When the digital input is 0 the output is -V reference, when the digital input is 128 the output will be 0 volts and when the digital input is 255 the output will be +(127/128) * V reference.

Attenuator Slope Compensation E

Attenuator slope compensation is used to increase or decrease the level reference voltage as a function of frequency. When this reference is increasing, it causes the leveling circuitry to increase the output power as a function of frequency to compensate for power losses in the attenuator or cabling between the detector coupler and the output of the 8340A.

In Band 0 this slope compensation is used to compensate for the frequency response of the Band 0 detector. Since the Band 0 detector can have either a positive or negative slope versus frequency response, it was necessary to make this compensation circuit bipolar.

The rate at which the output power increases is determined by the number written into the attenuator slope compensation DAC (U8). This number may be different for each RF attenuator step if their frequency characteristics are different.

The frequency reference for this circuit is the V/GHz line which comes from the A28 SYTM driver board. The voltage on the V/GHz line is -0.25 volts per GHz. V/GHz is derived from the pretune voltage.

The V/GHz line goes into an inverting amplifier (U5B pin 6) which has a gain of -(10/12.1). This gain block is necessary since the reference voltage required at the DAC (U8 pin 14) must be positive.

The Signetics NE5018 DAC is used for all three compensation DACs (U8, U9, and U10). It contains input latches and an output buffer. Inside this DAC, the reference voltage is converted into a reference current.

Digital data is latched off of the data bus when the Latch Enable signal (U8 pin 10) goes LOW. This latched data controls the current switches inside the DAC to produce a current that is proportional to the Reference voltage and the latched digital information. This current is then fed into a current-to-voltage conversion stage and appears at the output (U8 pin 18) as a voltage which is proportional to the voltage on the VREF input (pin 14) and the digital information.

The diode (CR1) connected to the summing node of the DAC (U8 pin

20) prevents the summing node from droping more than a diode drop below ground and therefore improves the DACs settling time.

A capacitor (C10) is connected in parallel with the internal feedback resistor (U8 pins 18 and 20) provides high frequency stabilization under all conditions. Another capacitor (C9) is connected between the summing node and the amplifier compensation pins (U8 pins 20 and 21) and is required to make the output amplifier as fast as possible while still remaining stable.

Cable Slope Compensation F

The Cable Loss TC Compensation is accomplished by summing a modified form of the V/GHZ voltage into the summing amp (U5A pin 2). R70 and R71 form a voltage divider which decreases the temperature compensation for front panel output options where the cable length is short. The amount of compensation at 25 degrees C is approximately 0.0027 dB/GHz. In the rear panel options where the cable length is long, R71 is removed and R70 is shorted to provide 0.0052 dB/GHz compensation at 25 degrees C. Since RT1's resistance decreases as its temperature increases, the amount of compensation increases with temperature.

Compensation Summing Amplifier G

The summing amplifier (U5A) sums four compensation terms together with the correct polarity and gain.

The Attenuator Slope Compensation is summed into the inverting input (U5A pin 2). This signal has a gain of -2.5. The NE5018 DACs have a voltage gain of 2 so the overall gain from input (R58 in Block **E**) to output (U5A pin 1) is = -4.13. One GHz Change in frequency will produce -0.25 volts change of the V/GHz line and 1.033 volts change at the output (U5A pin 1). The sensitivity of the LVLCOR output (U5A pin 1) is 1.25 dB/V so the above 1.033 volts represents a change in power of 1.033 V(1.25 dB/V)=1.29 dB. The above was assuming that the DAC was set at full range (input = 255). If we now want to know the effect that one bit change of the DAC has on the output we divide by the number of bits (256). The resulting sensitivity of the Attenuator Compensation DAC is (1.29 dB/GHz)/256 bits=0.00504 dB/GHz/Bit which is approximately 0.005 dB/GHz/Bit.

The 9 GHz Slope Compensation is summed into the inverting input (U5A pin 2) with a gain of -1.0. The overall gain is 2.0. One GHz change in frequency will produce 0.50 V change at the output. The resulting sensitivity of the 9 GHz Slope Compensation is [0.50 V/GHz(1.25 dB/V)]/256 Bits=0.0025 dB/GHz/Bit.

The 20 GHz Slope Compensation is summed into the inverting input

(U5A pin 2) with a gain of -2.0. The overall gain is 8.0. One GHz change in frequency will produce 2.0 V change at the output. The resulting sensitivity of the 20 GHz Slope Compensation is [2.0 V/GHz(1.25 dB/V)]/256 Bits=0.01 dB/GHz/Bit.

Cable losses after the ALC detector must be accounted for by increasing the compensation voltage as a function of frequency. This cable loss increases with increasing temperature; therefore a temperature-dependent frequency compensation must be summed in.

ALC Reference Generator H

A CMOS 10-bit multiplying DAC (U14) is used to control the reference voltage for the Level Control circuits.

The temperature accuracy of the entire leveling system cannot be any better than the reference voltage. Therefore an AD581L 10.00V precision reference (Q1 in Block **S**) is used for the reference into the level DAC. The T.C. of this device is less than 5 ppm. The +20 volt supply is used as the input voltage (Q1 pin 1) to minimize the load on the +15 V supply that is created on this board.

From this 10.00 volt reference, the level DAC (U14 pin 15) creates a current that is a function of the 10-bit digital input. Each LSB represents 1/1024th of the reference current. The current created above is a differential current between I1 (U14 pin 1) and I2 (U14 pin 2). Internal to the CMOS DAC (U14) there is a feedback resistor
connected between I1 and RFB feedback (U14 pin 16). This resistor's value tracks the T.C. of the current produced by the DAC.

I1 is connected to the inverting input of the output op-amp (U17 pin 2). I2 is connected to the non-inverting input of this op-amp (U17 pin 3) and to reference ground. The feedback resistor (U14 pin 6) is connected to the output of the op-amp (U17 pin 6).

If we consider the op-amp ideal, then the voltage at I1 must be zero; furthermore, the input current to the op-amp must be zero. The current sourced by the DAC must go somewhere and therefore the op-amp produces a voltage at its output that is exactly sufficient to sink this I1 current through the feedback resistor. This produces a voltage drop that is proportional to Rfeedback. A larger digital value increases I1 in proportion, and the voltage at the output of the op-amp (U17 pin 6) must become more negative to sink the appropriate amount of current through Rfeedback.

From the above we can conclude that the voltage produced at the output will be negative and will be between 0 volts and

(1023/1024) * Vref.

A schottky diode (CR8) is placed accross the I1 and I2 pins of the DAC. This prevents the voltage at these pins from exceeding the supply voltage during turn-on which would cause latch-up.

The digital inputs to this DAC are latched off of the instrument data bus by two 74LS174 6-bit latches (U13 & U16). The clock for these latches is the WLEVEL strobe (U27 pin 14 in Block **B**). The outputs of these latches are pulled up to the 5 volt supply with 1K ohm resistors. These pullups reduce the magnitude of digital noise feeding through the latches by pulling each output up hard to the supply.

Power Sweep Generator I

The level sweep DAC provides the power sweep function by sweeping the level reference as a function of the sweep ramp. This feature may also be used by the customer to compensate for line length external to the 8340A.

The operation of the level sweep DAC (U24) circuitry is exactly the same as the level DAC (U14) except that its reference voltage (U24 pin 15) is the RF Sweep ramp. This input linearly varies between 0 and +10 volts as the frequency sweeps between the start and stop frequency. The RF Sweep ramp is clamped to ground and VDD by two schottky diodes to prevent any latch-up problems. The operation of output op-amp (U31) and the input latches (U23 & U30) is the same as the equivalent circuitry in the ALC REFERENCE GENERATOR, Block **H**.

Fail Test LED K

The Fail Test LED is used to indicate that an error condition has been detected on the level control board during self test using the ADC to check the major functional blocks on the board. This LED is turned on and off by the processor.

ADC Control Latch L

A 74LS174 (U29) is used to latch six control signals off the data bus when the WADCC strobe (U29 pin 9) goes LOW. These signals are LOW CNVERT ALWAYS (U29 pin 2), LOW DON'T CNVERT (U29 pin 15), LOW AMUX0-2 (U29 pins 5, 12 & 7) and HIGH SRQ DISABLE (U29 pin 10).

ADC Clock/Control M

The clock for the ADC is generated by a schmidt trigger input NAND gate with RC feedback. The clock frequency is not critical and can vary by as much as 2:1 without causing any problems. This clock is controlled by several digital signals (U6B pins 10,12 & 13). Assume that one of the clock control signals is LOW thus disabling the clock and causing the output (U6B pin 8) to be HIGH. When the output of this circuit is HIGH, the feedback input (U6B pin 9) will also be HIGH after a period of time. If the clock circuit is enabled by all of the clock control signals going HIGH, the clock output (U6B pin 8) will immediately go LOW. The feedback input (U6B pin 9) will begin to head towards 0 volts at a rate determined by the RC time constant formed by R21 and C32. As soon as this voltage reaches the trigger threshold of the NAND gate, the clock output will go HIGH. The feedback input will head towards Vout at a rate determined by the RC time constant. As soon as this voltage reaches the trigger threshold of the NAND gate the clock output will again go LOW and the cycle will be repeated until one of the control lines (U6B pins 10,12 or 13) is pulled LOW.

Clock control enable U6B pin 10 is connected to LA-D SRQ so that the clock circuit is disabled whenever the ADC is being read. When the conversion is complete, the rising edge of the ADC clock (U6B pin 8) clocks the up/down counter (U1 pin 2 Block **Q**) which causes its RCO signal (U1 pin 15) to go HIGH. This clocks the conversion complete flip/flop (U21A pin 3 in Block **Q**) causing SRQ (U21A pin 5) to go LOW. The ADC clock must be disabled before the next falling edge of the clock to eliminate any partial clock pulses. Clock control enable U6B pin 13 is driven by the latched control line LOW DON'T CONVERT (U29 pin 15 in Block **L**). This signal allows the instrument processor to prevent the ADC clock from running when it is not being used. Clock control enable U6B pin 12 is driven by the output of a NAND gate (U26B pin 11) used as a dual negative input OR gate.

If either U26B input goes LOW, the clock circuit will be enabled. The first input (U26B pin 13) goes to L CNVERT ALWAYS. Any time this line is LOW, the clock will be enabled to run. The other input (U26B pin 12) is driven by a four input NAND gate (U6A pin 6). If LOW CNVERT ALWAYS is HIGH then the clock will be disabled when either input to U6A is LOW. The first input (U6A pins 1&2) are connected to the output of the conversion latch (U21B pin 9). The clock will be stopped when the conversion complete latch is reset which occurs at the end of a conversion cycle. The other inputs to this gate (U6A pins 4&5) are connected to HADCEN (XA27P1 pin 8) which goes to the ALC circuitry and is HIGH only when a valid voltage representing the detected output power is present on the DETLVL line (XA27P1 pin 29). HADCEN has a pullup resistor (R59) so the ADC will function normally if the ALC board is removed.

ADC Input Multiplexer N

The purpose of the ADC input multiplexer is to allow the processor to select which analog input line the ADC will convert to Digital information for use by the processor.

As discussed under Block **L**, AMUX0,1,2 are latched off the instrument data bus and determine which channel is selected. The output of the MUX (U25 pin 8) is connected to the summing node of an op amp. The buffer amp allows each channel to have a different gain and offset.

Channel 0 (U25 pin 4) is bipolar with a gain of 1 which will yield a full scale input range of $\pm$5.0 volts. Channel 0 is the DET LVL input from the Detector board and is corrected to accurately represent the actual output power of the 8340A when this voltage is valid. The scale factor of this voltage is -0.2 V/dB or $\pm$ 25 dB fullscale.

Channels 1 through 5 (U25 pins 5,6,7,12 & 11) are voltages that can be used by the processor to determine if major portions of the instrument are functioning correctly. Resistors R61 through R64 are used to sum an offset current into the buffer amplifier (U18A pin 2) to offset its output (U18A pin 1) to -5 volts. This allows the measured voltage to vary from 0 to -10 volts while the ADC sees -5 to +5 volts. Channel 6 (U25 pin 10) is scaled to allow -3.53 to +2.47 volts input. MOD LVL is connected to this input. If the SYTM is peaked by the processor so that more power is available, this voltage will change proportionately and if less power is available this voltage will change in the opposite direction. This input is required to provide feedback to the instrument processor for the auto-peaking and auto-tracking functions.

Channel 7 (U25 pin 9) will allow ±5 volt signals and is connected to TP 16 on the Level Control board. This input is used during testing of the ADC.

Test ADC O

The TEST ADC is essentially an internal voltmeter that measures the voltage of a pre-selected line and converts it into digital information. The processor reads the output of the TEST ADC, thus monitoring the voltage of the selected line. One example of how this circuit is used follows:

The 8340A normally places the user-selected power level in the Front Panel "ENTRY" an POWER dBm" displays. Under the conditions listed below the selected power level may not be the same as the actual power output.

- When the RF power output is unleveled.
- When the instrument is in the External Leveling mode.
- When AM is engaged (a dc voltage on the AM input will cause a change in the actual RF output power).

When any of the above conditions occur the TEST ADC monitors the DETLVL INPUT from the ALC circuitry and converts it into digital information. The processor reads this information and converts it into an equivalent power level in dBm. This value is displayed in the Front Panel "POWER dBm" display.

The Tracking Analog-to-Digital Converter (U11) contains a D-to-A converter and reference amplifier, an up/down counter, a window comparitor to control the up/down counter and data latches to store conversion data. A precision resistor (R17) is connected to the precision 10.00 V reference and to the converters Iref and Ref Amp + terminals (U11 pins 5 & 9). The Iref terminal connected to the reference current resistor (R17) is held at ground by the reference amplifiers input (U11 pin 5). The reference current is simply Vref/R17=1 mA. This reference current is multiplied by four in the DAC and then is divided appropriately according to the digital output of the internal 10-bit up/down counter. Iout of the DAC (U11 pin 10) is a current going into the A/D converter (U11 pin 11) and is summed into a 1 Kohm resistor along with an offset current of 2 mA through R18 (10.00V/R18) and the input current determined by R43 (Vin/ 2.5 Kohm). This summing node is connected to the comparitor input (U11 pin 11) which compares this voltage to reference ground. Since this summing node is held at ground (via digital feedback), the algebraic sum of the currents entering and leaving this node must equal zero. If the

currents entering this node are slightly greater than the currents leaving the node the internal window comparitor will signal the up/down counter to count up. This will in turn increase the current sinking output of the DAC (Iout U11 pin 10) until it sinks just enough extra current to compensate for the excess current entering the node. The reverse is also true. The window comparitor, up/down counter, and DAC will compensate for a deficiency of current at the summing node by decreasing the amount of current sunk by Iout. The digital value contained in the up/down counter, when the currents at the summing node are in equilibrium, is the digital representation of the current entering the node through R43. The offset current summed into the summing node through R18 forces the digital value to the DAC (and digital ouputs) to be mid range when no current is flowing in the input resistor (R43). This allows a bi-polar input voltage at R43 so that both positive and negative voltages can be digitized. The input voltage range at R43 is -5V to +5V. A -5 volt level will yield a digital value of 0; 0 volts will yield 512; and +5 (511/512) will yield 1023.

The digital outputs of the internal up/down counter go into transparent latched output buffers. Whenever the Data Hold line (U11 pin 28) is HIGH, the digital information appears at the outputs (U11 pins 18 through 27). If the Data Hold line is brought LOW, the information present at the DAC and up/down counters at that instant will be frozen in the output latch/buffers. Since the outputs are always enabled, the digital information appears directly at the inputs to two 74LS367 bus buffers (U12 & U15). When the main processor is ready for the ADC data it causes the RLEVEL strobe to go LOW which enables the outputs of these bus buffers (U12 & U15 pins 1 & 15) and places the ADC data on the instrument data bus to be read by the instrument processor. This RLEVEL strobe is also connected to the Data Hold on the ADC (U11 pin 28) so that the information in the ADC latches cannot be changed while it is being read. The ADC requires that the Data Hold line cannot be brought LOW for 150 nS after the rising edge of the ADC clock to allow for settling of the counter outputs. Due to the asyncronous nature of the ADC clock and the RLEVEL strobe, the above restriction means that the ADC clock cannot be allowed to run while the ADC is being read.

ATTENUATOR INSTALLED SENSING

A pulled up line that is grounded by the installation of the attenuator is connected to the input of DB 10 of the ADC data output buffers (U15 pin 10). This bit will be read any time the processor does a read level operation. This information is used to determine if the attenuator is installed only if the calibration data has been damaged and the default values must be used.

ADC Window Comparitor P

Since the ADC clock must not run when the voltage into the ADC is not changing, an external window comparitor (in addition to the window comparitor that resides inside the Test ADC) senses when the ADC clock should be turned on, allowing the ADC to function. The summing node of the current DAC inside the Test ADC and the input current through R43 is sensed by the widow comparitor circuit. Whenever the input current does not match the current output from the ADC, an offset voltage proportional to the error between the DAC current and the input current exists. Both the internal window comparitor and the external window comparitor sense this voltage. The external comparitor is set to trigger when this voltage exceeds approximately $\pm$1 LSB of the ADC. This window comparitor then starts a conversion. In this way the ADC clock can be turned off until the input voltage changes by more than approximately 2 LSB maximum.

U7 is an OP-07, a very low offset op-amp, which has been connected to provide a gain of approximately 19-20. Its purpose is to provide a larger voltage, representing one LSB to the comparitors. In order to provide a significant increase in resolution, U7 must have an input offset voltage which is much lower than the comparitor's.

The filter formed by R46 and C38 prevents transients or noise generated by the clock circuit from triggering the comparitors when the voltage is within the window.

U2 and U3 form the window comparitor. R47 and R48 set U2 output HIGH until the (-) input (U2 pin 3) exceeds 75 mV. R49 and R60 set U3 output HIGH (U3 pin 7) until the + input (U3 pin 2 is less than -75 mV. C39 and C40 provide noise filtering. Both U2 and U3 are open collector output comparitors so R50 is provided to pull up this signal to 5 volts. This open collector line is called LOW Outside Window (TP 5).

Conversion Complete Timer/SRQ Latch Q

The function of the conversion-complete timer is to allow the clock to run for 8 clock pulses after the widow comparitor has signaled that the ADC has converted the input voltage to within $\pm$1 LSB of the actual value. This will allow the ADC sufficient time to convert the input voltage down to within $\pm$0.5 LSB before its clock is stopped. (Assuming the input voltage is not changing.)

The output of the window comparitor (L OUTSIDE WINDOW) is inverted by U26C which drives LOW Enable of a LS169 counter (U1

pin 7). This counter is enabled to count up when the voltage being converted is inside the window. After 8 counts the carry out (U1 pin 15) goes LOW which does a parallel load (U1 pin 9) and clocks both the ADC clock control flip-flop (U21B in Block **M**) and the SRQ latch (U21A). The D input to the ADC clock control flip-flop (U21B in Block **M**) is grounded so it is reset which turns the clock off.

The D input to the SRQ flip-flop (U29A in Block **Q**) goes to H SRQ DISABLE (U29 pin 10 in Block **L**). If H SRQ DISABLE is LOW then U21A (Block **Q**) will be reset. The output of latch U21A goes to U22 in Block **R** to be read by the instrument processor and to a SRQ delay circuit. This SRQ circuit will allow only one ADC SRQ every 100 mS to limit the amount of main processor time devoted to servicing the ADC. LA-D SRQ also goes to U6B pin 10 (in Block **M**) which disables the ADC clock until the SRQ is cleared by the RLEVEL strobe.

In the delay circuit, Q2 will be conducting any time the ADC is not requesting service. As soon as ADC SRQ goes low, Q2 will be turned off and C53 will be charged up through R42. When C53 is sufficiently charged, the voltage at U19A pin 2 will cause its output (LCHNG) to go low. This signals the processor that a change has occurred. As soon as the processor reads the ADC, the SRQ flip-flop will be set so its output (U21A pin 5) will go HIGH, Q2 will turn on and pull the input to U19A LOW and therefore its output will go back HIGH. R40 provides base drive current for Q2 since the output current of U21 would not be sufficient. R39 limits the discharge current of C53 when Q2 turns on.

The Change Detectors U19B and U19D are designed to output a LOW going pulse onto the LCHNG line to the digital interface board to indicate that a change has occurred on the Unleveled or Overmod inputs to the Level Control board.

The inputs (LUNLVL and LOMD) also go to an output buffer (U22 pins 4 & 12 Block **R**) which can be read by the processor to determine what signal has changed state.

Assume that LUNLVL is HIGH initially; therefore both inputs to the LS266 open collector exclusive nor gate U19B will be HIGH. An exclusive nor gates output will go LOW when its inputs are at different logic levels, therefore for the above conditions its output will be HIGH. When LUNLVL goes LOW, one input (U19B pin 6) immediately goes LOW while the other (U19B pin 6) remains above the trigger threshold due to the limited discharge rate of C41 through R54. The output (U19B pin 4) will be LOW during this time. After some period of time, both inputs will be LOW. When LUNLVL goes HIGH, one input (U19B pin 6) will immediately go

HIGH, while the other input (U19B pin 5) will remain below the trigger threshold for some period of time due to the charge rate of C41 through R53 & 54. The output of the gate (U19B pin 4) will be LOW until the trigger threshold is reached.

The values of R54 and R52 were chosen so when LUNLVL or LOMD are LOW both inputs to U19 will be below the trigger threshold with worst case input currents to the gate. R53 and R51 then have been chosen so that the voltage divider formed with R52 and R53 will be above the trigger threshold under worst case conditions.

Status Buffer R

There are several bits of information about functions on the Level Control board that must be communicated back to the instrument processor and several ADC control lines that must be asserted by the instrument processor.

A 74LS367 bus buffer (U22 Block **R**) is used to put several bits of information onto the data bus when the RSTAT strobe is pulled LOW (U20 pin 7 in Block **B**). Four signals are communicated to the processor. They are LA-DSRQ (U22 pin 14 in Block **R**), LUNLVL (U22 pin 4), LOMD (U22 pin 12) and LOW BD INSTALLED (U22 pin 2).

Power Supplies S

Standard power supply filtering is provided for the +20V, +5V, -5V, -10V and -15V supplies. Low Q filters were used to help prevent resonances. A +15 V supply is provided using a 3 terminal adjustable regulator (Q3). In addition to all of the above supplies, a low current +10V supply is provided for the CMOS 7520 DACs U8, U9, and U10. The reliability of these CMOS DACs should increase as the voltage stress is decreased as far as practical. This 10V supply is tied to the +5.2 V supply to prevent the digital inputs to the DACs from being greater than the VDD supply when the instrument is turned on.

R57 is used to remove dc currents from the Reference Ground. These currents are injected by the DACs and other resistors connected to this ground.

Q1 is an AD581L 10.00V precision reference. This voltage (+10VR) is used as the reference voltage for the level DAC (U14 Block **H**) and to produce precision offsets (Block **C**, **D**, and **T**). The +20 volt supply is used as the input voltage (Q1 pin 1) to minimize the load on the +15V regulator (Q3).

Reference-Level Summing Amplifier T

The output from the Level DAC and the Level Sweep DAC are summed

together at unity gain by the summing op-amp (U18B). The +10.00 reference is also summed into this op-amp with a gain of 0.5 to provide a negative 5 volts offset at the level reference output (U18B pin 7). The output can be adjusted between approximately -5.12 and +5.11 volts by the main Level DAC. This voltage represents a change in output power of +25.55 dBm to -25.60 dBm and represents a slope of approximately -0.2 volts/dB. This is approximately because the exact slope and offset of the level reference is corrected in software by the instrument controller.

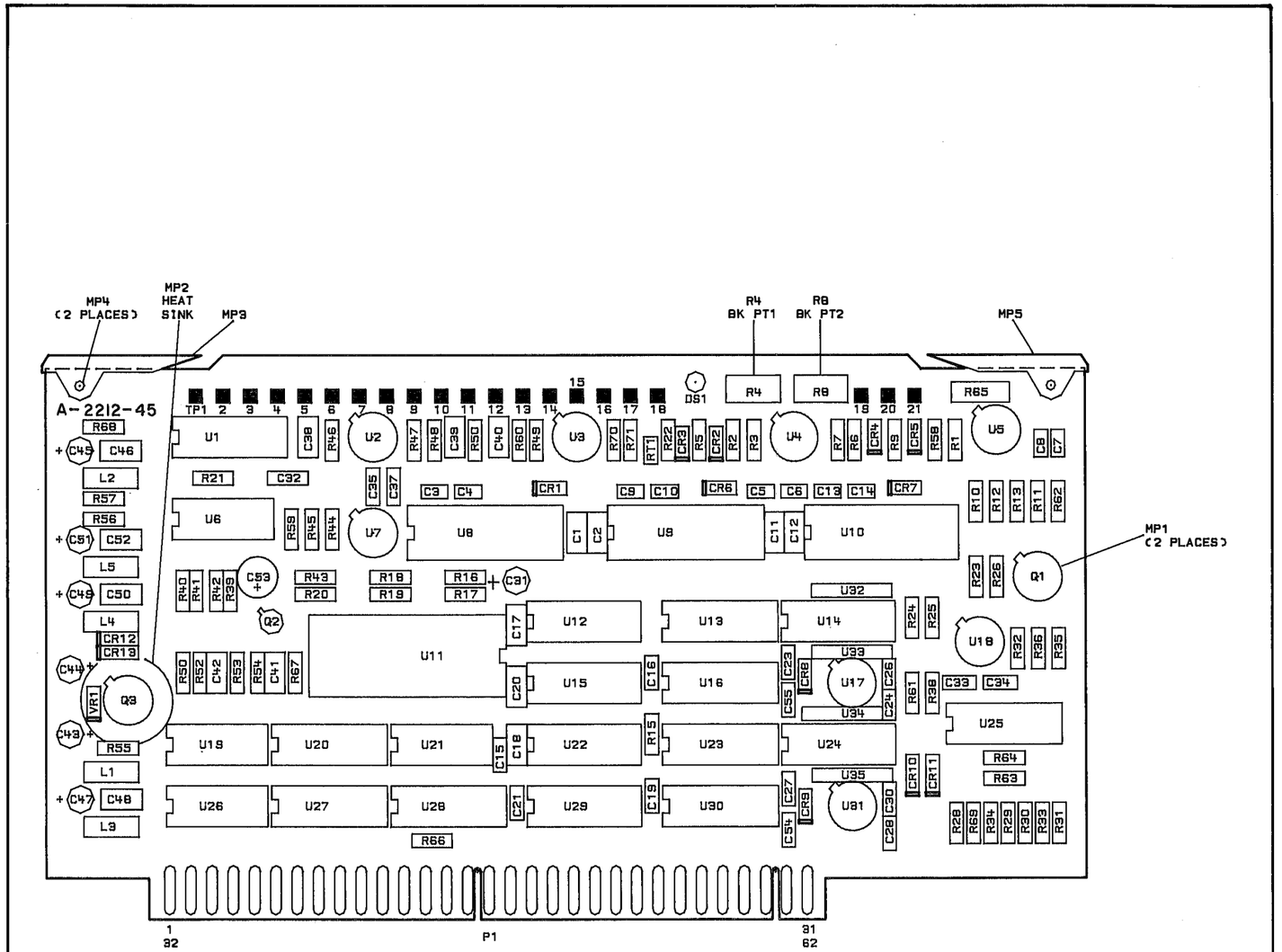


Figure 8I-38. A27 Level Control, Component Location Diagram

A27 Control P1 I/O (1 of 2)

A27

Pin	Mnemonic	Levels	Source	Destination
1 32	−5.2V −5.2V	−5.2V −5.2V	XA53P1-18, 36 XA53P1-18, 36	*S *S
2 33	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*S *S
3 34	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*S *S
4 35	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*S *S
5 36	−15V −15V	−15V −15V	XA56P1-15, 30 XA56P1-15, 30	*S *S
6 37	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*S *S
7 38	GND PLANE GND PLANE	0V 0V	IN GROUND IN GROUND	*S *S
8 39	HADCEN LATTN	TTL (HIGH TRUE) TTL (LOW TRUE)	XA21P1-1 A62J20-14	M 0
9 40	ADR0 ADR1	TTL TTL	XA60P1-17 XA60P1-73	*B *B
10 41	ADR2 ADR3	TTL TTL	XA60P1-18 XA60P1-74	*B *B
11 42	ADR4 SIOA	TTL TTL (LOW TRUE)	XA60P1-19 XA60P1-15	*B *B
12 43	WLEVEL WBAND	TTL (LOW TRUE) TTL (LOW TRUE)	B B	XA24P1-33 XA28P1-29
13 44	WYTMSLP	TTL (LOW TRUE)	B	XA28P1-30
14 45	WYTMCTL RSTAT	TTL (LOW TRUE) TTL (LOW TRUE)	B B	XA28P1-8 *
15 46	W11R2 HLB0	TTL (LOW TRUE) TTL (HIGH TRUE)	B A	XA23P1-15 *
16 47	HLB1 HLB2	TTL (HIGH TRUE) TTL (HIGH TRUE)	A A	* *

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A27 Control P1 I/O (2 of 2)

A27

Pin	Mnemonic	Levels	Source	Destination
17 48	RFSWP LOMD	10V/SWEEP TTL (LOW TRUE)	XA57P1-42 XA26P1-8	I Q R
18 49	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*S *S
19 50	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*S *S
20 51	LHET −.25V/GHZ	TTL (LOW TRUE) −.25V/GHZ	A XA28P1-40	* *
21 52	LCHNG LUNLVL	TTL (LOW TRUE) TTL (LOW TRUE)	* XA26P1-36	Q Q R
22 53	DB0 DB1	TTL TTL	*XA60P1-20 *XA60P1-76	*L *L
23 54	DB2 DB3	TTL TTL	*XA60P1-21 *XA60P1-77	*L *L
24 55	DB4 DB5	TTL TTL	*XA60P1-22 *XA60P1-78	*L *L
25 56	DB6 DB7	TTL TTL	*XA60P1-23 *XA60P1-79	*L *L
26 57	DB8 DB9	TTL TTL	*XA60P1-24 *XA60P1-80	*L *L
27 58	DB10 DB11	TTL TTL	*XA60P1-25 *XA60P1-81	*L *L
28 59	RGND WMOD	0V TTL (LOW TRUE)	STAR GND POINT B	*S *
29 60	DETLVL RGND	−0.2V/dB, 0V = 0dB 0V	XA25P1-33 STAR GND POINT	N *S
30 61	LVLREF MODLVL	0.2V/dB, 0V = 0dB 0 TO −3V LEVELED	T XA26P1-32	XA25P1-13 N
31 62	BVSWP LVLCOR	10V SWEEP 1.25 dB/V, 0V = 0dB	XA58P1-40 G	N XA25P1-14

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

TP1 TP6 TP8 TP20 TP21 TP19 TP17 TP2 TP16 TP7 TP3 TP5 TP16 TP10 TP9 TP8 TP18 TP13 TP4 TP12 TP11 TP14

FLATNESS COMPENSATION

POWER LEVEL REFERENCE

Ⓐ BAND SWITCH CONTROL

Ⓑ ADDRESS. DECODING

Ⓒ 20GHz BREAKPOINT SLOPE COMPENSATION

Ⓓ 9GHz BREAKPOINT SLOPE COMPENSATION

Ⓔ ATTENUATOR SLOPE COMPENSATION

COMPENSATION SUMMING AMPLIFIER

CABLE SLOPE COMPENSATION (NOTE 4)

Ⓗ ALC REFERENCE GENERATOR

Ⓘ POWER SWEEP GENERATOR

Ⓙ REFERENCE LEVEL SUMMING AMPLIFIER

Ⓚ FAIL TEST LED

CONTROL BUS

DATA BUS

Ⓛ ADC CONTROL LATCH

Ⓜ ADC CLOCK/CONTROL

Ⓝ CONVERSION COMPLETE TIMER/SRQ LATCH

Ⓡ STATUS BUFFER

Ⓢ POWER SUPPLIES

Ⓣ ADC INPUT MULTIPLEXER

Ⓤ TEST ADC

Ⓟ ADC WINDOW COMPARATOR

A-D CONVERTER

NOTES:
1. FOR OPTION 004 OR 008 (REAR PANEL OUTPUT) DELETE R79 AND REPLACE R76 WITH A JUMPER.

Figure 8I-39. A27 Level Control, Schematic Diagr

A28 SYTM DRIVER, CIRCUIT DESCRIPTION

Introduction

Refer to Figure 8A-41, "A28 SYTM Driver, Schematic Diagram".

The SYTM driver provides the correct amount of current to the SYTM coil for tuning the SYTM frequency under all conditions. Since the SYTM uses an open-loop tracking scheme, all differences in tracking conditions must be compensated for by the SYTM driver without the benefit of feedback. The SYTM driver also provides the rest of the instrument with voltages that are proportional to frequency (-0.25 V/GHz, +1.0/+0.5 V/GHz, +1.4 v/GHz).

Offset Compensation [A]

The offset compensation circuitry adds a correction current independent of frequency. The offset, adjusted by R1, affects the entire operating range of the SYTM and has a range of ±200 MHz. A separate offset adjusted by R113 is active only in band 1 (switched by Q4) and has a range of -125 to +75 MHz that is superimposed on the setting of R1.

Delay Compensation [B]

The SYTM magnet responds to any change in coil current, by setting up eddy currents to oppose the change. During a sweep, while the input current is ramping, the eddy currents set up a magnetic field that partially cancels the magnetic field required to tune the SYTM passband. A compensation current is added to the current driving the SYTM in order to offset the effects of the eddy currents. Since the eddy currents take time to set up, the start of the compensation ramp needs to be rounded. Although the transient response of the eddy currents do not follow an exponential function, using a low-pass filter on the delay compensation adequately accounts for the transient response.

The delay DAC (U3) gives the instrument processor control over the gain of the delay correction. When the processor writes to IO address 10,R2: a strobe (WBAND) is generated on the A27 Level Control Board. WBAND comes onto the SYTM driver through P1 Pin 29. When WBAND is pulsed, U14 latches the information on bits 3 through 10 of the Data Bus. The latched bits form the binary input to the delay DAC (U3). The reference input to the delay DAC is the sum of inputs. When Q10 is closed the voltage across C13 is self-adjusting to give 0V output from U5A. When Q10 is opened, the output of U5A is proportional to the -0.25 V/GHz line, offset by the voltage across C13. When the instrument is sweeping, this generates a ramp that is referenced to the frequency at the time Q10 was opened. Q10 is open when HSP (P1 Pin 26) is HIGH. The

output voltage at U5A is summed into U2A through R7 (DYS) for the delay compensation. The offset is adjusted through R6 (DYO) and summed into U2A as well. If the 8340A is sweeping 19.8 GHz to 26.5 GHz and if R6 (DYO) and R7 (DYS) are both turned fully counter-clockwise, then the output of U2A pin 1 will ramp up to about +12.7 V. R55 converts the output of U2A into the reference current (Iref) for the delay DAC (U3). Iref causes an equal current to flow from a series of binary weighted switches in U3. The binary switches are driven by the latched bits from U14. The internal binary weighted switches source the current from U3 pin 4 when the latched bits corresponding to the switches are HIGH. When the latched bits are LOW the current is sourced from U3 Pin 2. Thus when all of the latched bits are HIGH U3 Pin 4 will sink a current equal to Iref and U3 Pin 2 will not sink any current. When all of the bits are LOW U4 Pin 2 will sink a current equal to Iref and U3 Pin 4 will not sink any current. The amount of current sunk by U3 Pin 4 (I1) and U3 Pin 2 (I2) will vary between the two extremes in proportion to the latched binary code with the sum of I1 and I2 equal to Iref. The voltage present at U2C pin 8 is equal to I1*2K. In terms of the input current this becomes Iref*N*2K where N is the ratio of the binary input to the full scale binary input to the DAC. Q9 switches the delay compensation into the compensation summing amplifier at appropriate times. Q9 conducts when HSP (P1 Pin 26) is HIGH. Since HSP is also HIGH in CW the delay DAC (U3) is programmed to 0 by the processor because no delay compensation is required in CW operation. R46, R47 and C26 form a low-pass filter that rounds the first part of the delay compensation waveform.

Slope Compensation [C]

The slope compensation circuits generate a correction current proportional to frequency. The slope DAC (U4) provides microprocessor control over the slope correction and enables the 8340A to do the required self-peaking (see Block H description). When the processor writes to I/O address 11:R1 a strobe (WYTMSLP) is generated on the A27 Level Control Board. WYTMSLP comes onto the SYTM driver through P1 Pin 30 and causes U15 to latch the binary input for U4. The reference input for U4 is the PRETUNE signal that has been scaled and inverted by U2B to give +1.4 V/GHz +- 1%. This voltage is also output from P1 Pin 7 and is used for the ramp bias of the step recovery diode in the SYTM. The voltage present at U2D Pin 14 is equal to the combined effects of I1 (current sunk by U4 pin 4) and I2 (current sunk by U4 pin 2). The two current effects can be considered independently and then added for the final result. To consider the effects separately, set one equal to zero and look at the effects of the other. No current will flow through R57 due to I1 so the voltage at U2D Pin 14 due to I1 will be equal to -2K*I1. No current will flow through R58 due to I2 so the voltage at pin 14 due to I2 will be

2K*I2. The voltage at U2D Pin 14 due to both currents will be 2K*(I2-I1). I1+I2=Iref and I1=N*Iref (where N is the ratio of the binary input to the full scale binary input to the DAC). This gives a final result for the output voltage of U2D pin 14 to be (PRETUNE*4/8.9±1.3%)*(1-2*N). The output voltage of U2D pin 14 can vary by as much as ±8V which is summed into the compensation amplifier in Block **G** through R56. The output voltage on pins 2 and 4 of U4 can vary between -8V and 0V which is within the output voltage compliance of U4 (-8V and +21V). The DAC provides ±4% slope adjustment in band 1, ±2% in band 2, ±1.3% in band 3 and ±1% in band 4.

Since bits 0 through 2 are ignored when the data is latched into U15 from the data bus the binary pattern present at the input of the delay DAC increments once for every eight increments of the data on the Data Bus. Whenever the RPG is connected to U4 it will take eight pulses of the RPG to change the DAC by one bit. This will reduce the sensitivity of the RPG.

In addition to the correction provided by the slope DAC, three breakpoints are provided to correct for the non-linearities of the SYTM magnet. R20, R21, R22, R18 and R17 form a voltage divider used in conjunction with CR1 and CR2 to set fixed frequency breakpoints at 13.7 GHz (±2%) and 20 GHz (±2%). R2 and R3 vary the effect of the breakpoints adding as much as 3.1% and 3.2% respectively. R4, R5 and CR3 form a breakpoint that can be varied in frequency (anywhere above 23.2 GHz) as well as adjusted to add as much as 4.0% to the slope. All percentage increases in slope are referenced to the frequency where the breakpoint begins to take effect.

Programmable Voltage Divider [D]

The Pretune line comes to the SYTM driver board on P1 Pin 22. It is a voltage proportional to YO frequency and is adjusted to give -2.5 v/GHz with an accuracy of ±6.5mV ±7uV/C ±25ppm/C.

The programmable voltage divider uses a precision resistor array (U21) to attenuate the PRETUNE voltage giving a voltage that is proportional to SYTM frequency. The overall accuracy depends on the accuracy of the PRETUNE line as well as that of the resistor array. Hence, the specifications for the resistor array are important to the accuracy of the -0.25 V/GHz and +1.0/+0.5 V/GHz lines as well as to the tuning of the SYTM. The array consists of eight 2.5K resistors with a 5% absolute tolerance, 0.01% tracking tolerance relative to R1 (giving a worst case tolerance of 0.02% for any resistor ratio). The array also has a 2ppm/C tracking temperature coefficient between any two resistors.

The latched band information (P1 Pins 31, 32, and 33 in Block **I**)

is used as the input for a 3 by 8 decoder (U16). The outputs of the decoder are input into comparators (U19) that drive the gates of FETs to switch the appropriate node of the voltage divider.

-0.25V/GHz [E]

The -0.25 V/GHz line is the most widely used signal on the SYTM driver board. During Band 1-4 it is a buffered version of the voltage out of the programmable voltage divider. U6 has a low offset voltage (1.6 mV max over 0 deg. C.-70 deg. C.) and keeps the output within 1.6 mV (6.4 MHz) of the input signal. During Band 0, (Q11 closed and Q18 open) the instrument frequency is equal to the YO frequency offset by 3.7 GHz. The -0.25 V/GHz line uses the PRETUNE voltage, scales it down to -0.25 v/GHz and adds an offset voltage that equals 0.25 v/GHz*3.7 GHz or 0.925V. This signal is generated using the +10V reference, offset R68, R69, and R70, and PRETUNE. When the Band 0 signal is adjusted at 10 MHz by trimming the +10V reference with R85 (Block **K**) the -0.25 V/GHz line will be accurate within 10 MHz of the ideal value at 2.2 GHz.

Q11 and Q18 switch between the Band 0 and Band 1-4 conditions. A sample and hold circuit (Q5 and U5B) is used to remove the discontinuities that are present due to changing the band number and PRETUNE at different times.

Q6 is capable of sourcing 2 mA and sinking 40 mA. The normal load requires sourcing 0.5 mA and sinking 7 mA. R65 limits the amount of output current to protect Q6 in the event the output is shorted. R27 along with the +20V supply provide the sourcing capability. C16 is required to stabilize the loop during the sample mode. The holding capacitor (C14) is a mylar capacitor with an insulation resistance of 15,000 megohms. U5B has a maximum input bias current of 8 nA over 0 deg. C. to 70 deg. C. (100 pA @ 25 deg. C.). Q5 has a maximum drain cutoff current of 0.1 nA at 25 deg. centigrade. The maximum droop is 260 mV/sec. A normal holding interval is about 5 msec resulting in a maximum droop of 1.3 mV during the holding interval. This value drops substantially at instrument temperatures lower than 70 deg. C. The maximum droop at room temperature is 20 mV/sec or 0.1 mV during a holding interval of 5 msec. When the circuit is in the hold mode (Q5 open) R32 and diodes CR4 and CR5 keep U6 from saturation and making the output of U6 a buffered version of the input to U6. The output of U6 is used as a pullup voltage for the comparators driving the FET's in blocks **D** (programmable voltage divider) and **E** (-0.25 V/GHz). The output of U6 also drives the guard trace described in Block **H** description (current driver).

Without the clamping provided in the hold mode, the input diode protection internal to U6 would shunt current from the input

disturbing the desired SYTM tuning. Because U6 doesn't saturate, the transition from hold to sample occurs with a minimal perturbation. R33 attenuates the amplitude of the hold-to-sample perturbation. R30 adds a zero to the transfer function that eliminates the ringing of the perturbation.

+1.0/+0.5 V/GHz [F]

This block provides a voltage proportional to instrument frequency that is sent to the rear panel. The standard configuration has a sensitivity of +1.0 v/GHz. This limits at around +19V (+20V supply tolerance and 0.4V saturation across Q7). The +1.0 v/GHz sensitivity was necessary to interface with 8410B/C Series Network Analyzer. The limit of +19V doesn't matter in this case because the 8410B/C only covers up to 18.6 GHz. For applications involving the entire frequency range, 2 jumpers (W1 and W2) on the SYTM driver board can be cut to change the sensitivity to +0.5 v/GHz. Q8 and R37 provide a current source that limits around +19.7 volts. The current is on the order of 1.2 mA (not exact because the transistor parameters of each half will differ due to the difference in their power dissipation). This current in conjunction with R41 will give about a +5 volt offset from the output of U10. This removes the effect of op amp limiting which happens as low as +17V for U10. C19 insures that the 0 dB gain crossover for the loop has a slope of --6 dB/octave. Q7 is a dual NPN transistor, one side Q7B is used as a drive transistor for the output, the other side is used in conjunction with R38 to limit the output current to 7.8 mA. CR6 and CR7 protect the circuitry from voltages that may inadvertently be applied to the output. R73 and the -10V supply provide pull-down capabilities for the output. R75, R40 and R39 cause the output to be referenced to ground potential at the rear panel. R42, R43, C20 and C21 are used for high frequency noise rejection of the power supplies.

Compensation Summing Amplifier [G]

The currents that are generated by the slope, offset and delay compensation circuitry are amplified by a factor of 25 by U1 and injected into the collector of the drive transistor A47Q2. The R13 is effectively in parallel across the sense resistors on the A47 assembly with an additional current equal to the voltage at the emitter of Q1 divided by R13. Q1 is used to buffer the output of U1 allowing the amplifier to have a higher output voltage capability. R11 and the -10 volt supply provide a sink capability. The compensation summing amplifier U1 is able to pull the passband of the SYTM over the range of -220 MHz to +625 MHz. Q3 is a P-channel FET used to switch the compensation out during kick pulses (see Block **J** description). Q2, R116 and R117 drive the gate of Q3 to +20 volts to turn it off and to 0 volts to turn it on.

Current Driver [H]

When considering the errors of the current driver, only the temperature effects need be considered since the steady-state errors are adjusted out when the instrument is calibrated. The temperature errors indicate the need for a self-peaking routine for the 8340A. The 1 dB passband is on the order of 25-30 MHz in band 4 (assuming the instrument is calibrated to center the tracking in the middle of the passband), the errors that could result from a temperature drift would cause power losses greater than any tolerable level.

The sensitivity of the input node of the current driver is 4 MHz/mV. The impedance of the line can be as much as 2.6K ohms. In order to keep the errors due to leakage currents less than 1 MHz, the leakage currents must be kept below 100 nA. When leakage currents exist at frequencies greater than 1 MHz, potential problems could exist. To avoid the problems, guard traces are placed around the sensitive traces. The guard traces are driven by a buffered version of the same voltage.

A triple darlington configuration (Q26, Q27, and drive transistor A47Q2) is used to remove the effects of the variation of the beta of the drive transistor due to temperature. With this configuration, the base current into the OP-07 (U22) is less than 15uA so any variations in this current due to temperature would influence the tracking by less than 1 MHz. R110 and R100 are used to keep a small amount of current flowing through Q26 and Q27.

Q22 keeps U22 from saturating during the kick pulses. Q21 and Q25 are used in the generation of the kick pulses and are discussed in the Block **J** description.

Due to the inductance of the SYTM coil, a voltage spike is generated when the current ramp is reset. The zener diode, VR2 prevents this voltage kick from exceeding the breakdown voltage for the transistors by controlling the maximum allowed rate of change of current from the driver. CR10 protects the base-emitter junction of Q26 from large voltages that could cause a breakdown. CR11 is a low capacitance diode that is placed in series with VR2 to reduce the effect of the zener diode's junction capacitance. R111 is added to eliminate the ringing that would otherwise be present at retrace. There is also a zener diode protection circuit on the SYTM bias board. This circuit clamps the inductive voltage at a higher voltage (about 140V) than the one on the driver board (about 125V). The primary purpose for this circuit is to protect the drive transistor located on the sense resistor assembly (A47) in the event that the SYTM driver board is pulled out while the instrument is under power. The breakdown voltage of

the drive transistor is 400V. Q26 and Q27 have breakdown voltages of 160V so the clamping circuit on the bias board would also protect them if the clamping circuit on the driver board fails. Due to the method employed by the clamping circuit on the SYTM driver, the sense resistors always give an indication of the amount of current flowing through the coil. This voltage is used by the kick pulse comparators to sense the amount of current in the coil. If the clamping circuit on the driver board fails, there would be no negative (in frequency) kick pulse and the delay compensation wouldn't be as effective. However the rest of the circuit would work because the clamping circuit on the SYTM bias board would protect the transistors.

C39, C40, and R101 are used to match the frequency response of the SYTM coil to the frequency response of the YO coil. The sweep output on the front and rear panels is also matched.

During a bandswitch the -0.25 V/GHz voltage is more accurate for holding the SYTM at the desired current than is the normal attenuated PRETUNE voltage (see Block H). At these times the -0.25 V/GHz line is gated by Q12 to override the attenuated PRETUNE voltage to hold the SYTM and avoid the undesired kick pulses that would be present due to the discontinuities on the attenuated PRETUNE line. When the instrument is in the Band 0 the SYTM magnet is tuned to about 4 GHz to keep the YIG sphere from interferring with the output. Tuning the SYTM to 4 GHz is accomplished by closing Q17. R109, Q21, and Q25 will be discussed in the Block J description (kick pulses).

Digital Control [I]

The following digital control signals are used on the SYTM driver board:

HSP: (P1 Pin 26) A signal from the A59 Digital Interface board that is HIGH when the instrument is sweeping and LOW at bandcrossings and retrace. HSP is used to generate the DELAY and DLY RES signals which control Q10 and Q9 in Block **B**.

WBAND: (P1 Pin 29) (10:R2) Block **B** - A strobe from the A27 Level Control board used by U14 to latch data from the Data Bus for U3 (delay DAC).

WYTMSLP: (P1 Pin 30) (11:R1) Block **C** - A strobe from the A27 Control board used by U15 to latch data from the data bus for U4 (slope DAC).

WYTMCTL: (P1 Pin 8) (11:R3) Block **I** - A strobe from the A27 Level Control board used by U13 to latch S/H from Data Bit 3, SYTMSEL from Data Bit 4, KICK TRIGGER from Data Bit 5.

KICK TRIGGER: (U13 Pin 7 Block **I**) Initiates the SYTM kick pulse in Block **J** when set momentarily HIGH. KICK TRIGGER is a pulse that is about 20 usec wide.

SYTMSEL: (U17B Pin 1) controls the gate signal for Q12 in Block **H**.

S/H (DB3), LYTMKICK, and LYOKICK (P1 Pin 41) are used by U12A (Block **I**) to generate the sample signal which controls Q5 in Block **E**.

HLB0: (P1 Pin 31), HLB1 (P1 Pin 32) and HLB2 (P1 Pin 33) give latched band information decoded by U16 to control Q13, Q14, Q15, and Q16 in Block **D**, to generate the HET signal which controls Q17 in Block **H**, and to generate the Band 0 and Band 1-4 signals which control Q11 and Q18 in Block **E**.

HENDKICK: (U12B Pin 6 Block **I**) A signal that is HIGH when both the SYTM and YO kick pulses are off and it is routed to the A24 Attenuator Driver board to be read by the processor. If HENDKICK remains LOW for more than 90 msec the processor ignores it and activates the fault light indicating a KICK error.

U17, U18, and U19 are open collector quad comparators used to drive all of the FET switches on the board (except Q3, Q21 and Q25). The inputs to the FETs are TTL level signals. The outputs are pulled to -15V for LOW output and pulled up to the level set

by the pull-up resistor connected to the individual comparators. R93 and R94 set the switching threshold of 1.3V for the comparators.

Kick Pulses [J]

In order to set up a uniform past history for each sweep and to force the SYTM to settle faster, a sequence of kick pulses is used at the end of each sweep with a start frequency less than 22.5 GHz. Sweeps with start frequencies greater than 22.5 GHz are not kicked. When kicked, the STYM is kicked positive in frequency until a predetermined current is reached, then the SYTM is kicked negative in frequency until a second predetermined current is reached, it then is allowed to settle from that point. The kick pulses minimize the differences between the various sweep conditions (continuous, line, external, single, and alternate). They are not needed at bandcrossings because the SYTM's past history at bandcrossings is similar to that provided by the kick pulses.

When Q21 and Q25 in Block H are both open, the base current to the triple darlington is removed and the drive current decays to zero. This results in a negative (frequency) kick pulse. With Q25 open and Q21 closed the driver saturates and the current heads towards its maximum steady-state value giving a positive kick pulse. R133 and CR4 will cause Q25 to be open whenever Q21 is closed. This is accomplished by allowing the output of U7 enable U23 whenever U7 is LOW.

The frequency to which the SYTM is tuned is proportional to the current through the SYTM coil. The current through the coil is sensed by measuring the voltage on the sense resistor (at P1 Pin 44). This voltage is compared with adjustable preset levels by the two comparators (U7, U23) that drive Q21 and Q25.

It is necessary to deactivate the comparators when kick pulses are not desired so they don't interfere with the normal tuning of the SYTM. LM311's were chosen for the comparators because of the strobe pin that allows them to be deactivated. The deactivated state of the comparators will have a HIGH output. Normal operation of the current driver requires Q25 to be an N-channel FET (normally on) and Q21 to be a P-channel FET (normally off). The outputs of the comparators are used in the control of the strobe. The comparators are deactivated when 3 to 5 mA of current is drawn out of pin 6. Hence, U23 is deactivated when Q24A is turned on. Likewise, U7 is deactivated when Q19A is turned on. Q19B and Q24B are used as current mirrors with the necessary gain to insure that Q19A and Q24A have 3 to 5 mA in the off state. R114 and R82 set the current ratio between Q19A and Q19B. R115 and R108 set the ratio between Q24A and Q24B.

Q21 is turned off when the gate voltage is more positive than -11V. When the comparator is in the HIGH state R81 pulls the comparator output up to +5.2V. R83 feeds this level into the base of Q19A to latch the comparator into the HIGH state. In order for the comparator to become active Q19A must be turned off. This is accomplished by pulling the base voltage down below 0.6V. When the kick pulse is desired, Q20 is momentarily turned on which pulls the voltage down at the base of Q19A turning Q19A off and thus activating the comparator. If the voltage on the sense resistor is more positive than the voltage set by R10, the output of comparator U7 will go LOW (-15V) turning Q21 on and keeping Q19A OFF. CR8 keeps the output of U7 from pulling the base of Q19A below -0.4V. The comparator remains in this state until the voltage on the sense resistor reaches the threshold set by R10. The output of the comparator then switches to +5.2V turning Q21 off and Q19A on. This latches the comparator into the HIGH state until Q20 is again pulsed on.

Q25 is turned off when the gate voltage goes to -15V and turned on when the voltage is pulled up to the level of Q25's source voltage. U23 has an open collector output so the gate of Q25 is pulled up to the same voltage as the source by R103 in Block H. Again the the output of the comparator (U23) is used to latch itself into its HIGH state. In order to activate U23, Q24A must be turned off. This is accomplished when Q23 is pulsed on or whenever the output of U7 is LOW. The comparator then switches to its active mode if the voltage sensed at the sense resistor is more negative than the level set by R9. The output of the comparator goes to -15V which turns Q25 off. CR9 keeps Q22 from pulling the base of Q24A below -0.4V. U23 latches itself in its HIGH state in the same way U7 latches itself. R126 provides hysteresis around U7 while R128 and R134 provide hysteresis around U23. The hysteresis around each comparator ensures that the comparators will deactivate themselves once the appropriate conditions are met. CR12 keeps the output of U23 from disturbing the SYTM tuning when U23 is deactivated.

Thus, when a kick pulse trigger (KICK T) is sent by the microprocessor (by setting the common point of R107 and R104 to a HIGH TTL logic level) both comparators are activated and Q25 is turned off while Q21 is turned on (R9 and R10 are adjusted to levels out of the normal SYTM operating range). Q21 remains on causing the current to the coil to increase until the threshold set by R10 is reached. U7 then turns Q21 off and latches in this state. The coil current then decreases until the threshold set by R9 is reached. U23 then turns Q25 on and latches in this state. Both comparators remain in their latched state until another trigger pulse is sent. U23 is in it's active mode during both kick pulses. LYTMKICK is a TTL level signal that is LOW when Q24A

is off indicating when the kick pulses are active. LYTMKICK (offset by a diode drop) is also used to switch out the compensation during the kick pulses (see Block **G** description). If the compensation were left in it would be able to interfere with the current sense level to the extent that the negative kick pulse wouldn't shut off.

Voltage Reference [K]

The +10 VREF and -10 VREF are generated for cases where accurate supply voltages are needed. The +10V reference is adjusted by R85 to null the offset error in Band 0 of the +1.0/+0.5 V/GHz lines (see Block **F** description). It has a maximum temperature drift of 25 ppm/C. R84 is used to reduce the loading on the +10V reference (U5). U13, R86, R87 and R88 form a voltage inverter creating a -10V reference supply.

Power Supplies [L]

The power supplies coming to the board are: the +20V supply (P1 Pins 1,23), the +5.2V supply (P1 Pins 2,24), the -10V supply (P1 Pins 3,25), the -15V supply (P1 Pin 4) and the -40V supply (P1 Pins 5,27). All supplies coming onto the board (except the -40V supply) are filtered by low-pass filters consisting of a 4.7uH inductor in series with the supply followed by a 1 uF capacitor shunting across the supply to power ground. The -40V supply is used as a reference voltage in Block **H** (current driver) and is not shown in Block **L** of the schematic.

U11 regulates the +20V supply and provides a +15V supply to the rest of the board.

TROUBLESHOOTING PROCEDURE

NOTE:

Perform the following tests shown in Roman numerals. If one of the steps fail, perform the associated substeps shown in uppercase alpha characters. If one of the steps in uppercase alpha characters fail, perform the associated substeps shown in numeric characters.

I. Check the voltages on the power supplies. P1 Pins 1,23 should be +20V ±0.2V, P1 Pins 2,24 should be +5.2V ±0.05V, P1 Pins 3,25 should be -10V ±0.1V, P1 Pin 4 should be -15V ±0.2V, P1 Pins 5,27 should be -40V +0.7V, U9 Pin 6 should about +10V adjustable by R85 and U10 pin 6 should be the negative of U9 Pin 6 ±1.3 mV.

II. Set 8340A to CW 10MHz and adjust R85 (Block **K**) until the voltage out of the +1.0 V/GHz rear panel connector reads 10 mV ±1.5 mV.

A. If +1.0 V/GHz line won't adjust to 10 mV at 10 MHz, then check U9 pin 6. Output should vary around +10V as R85 is varied.

B. Check the -0.25 V/GHz line, R85 should be able to adjust it to 2.5 mV ±0.05 mV. If OK then check P1 Pin 17, it should read 10 mV ±1.5 mV when adjusted by R85. If it is correct at P1 Pin 17 then the rear panel BNC isn't connected to the +1.0 V/GHz line.

1. R41 (Block **F**) should have about 5V across it.

2. U8 (Block **F**) shouldn't be saturated.

3. R38 should have less than 0.4V across it. If R38 has 0.4V or more, check the +1.0 V/GHz line for an output short.

C. Check PRETUNE line at P1 Pin 22. It should read -9.25V ±5 mV.

1. Pull out A28 SYTM driver board (Refer to Repair Procedures in the beginning of the RF functional group) and verify that the PRETUNE line is valid on the A54 YO Pretune board (TP3).

Troubleshoot or adjust as necessary. Refer to the Sweep Generator - YO Loop functional group.

D. The gate of Q11 should have the same voltage as U6 pin 6 and the gate of Q18 should be about -15V.

1. U16 Pin 13 (Block **I**) should be LOW. U16 Pins 12, 11, and 10 should be HIGH.

a. U16 pins 1 and 3 should be LOW. U16 Pin 2 should be HIGH.

If not, pull out SYTM driver board and verify the latched band information on the A27 Level Control board; otherwise replace U16.

E. The gate of Q5 should have the same voltage as measured at U6 pin 6.

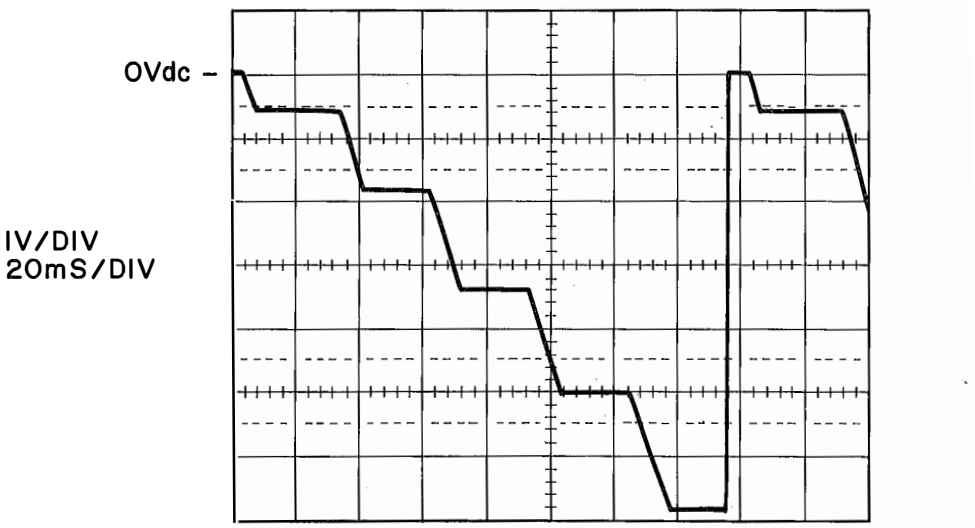
1. U12 Pin 1 should be LOW, it is an input to a three input and gate whose output U12 Pin 12 should also be LOW.

a. If U12 Pin 1 (Block **I**) isn't LOW check latch U13 for correct operation by using the signature analyzer test described in the troubleshooting section of the A60 Processor Assembly. I/O channel 11 subchannel 3 is the address of the strobe used with U13. This test may also be done by entering **[SHIFT] [GHz] [1] [1] [Hz]**, **[SHIFT] [MHz] [3] [Hz]**, **[SHIFT] [KHz] [8] [Hz]**. U13 Pin 2 should be HIGH. Then enter **[6] [5] [5] [2] [7] [Hz]**. U13 Pin 2 should now be LOW. If either condition fails, it indicates a problem with either the Data Bus or U13.

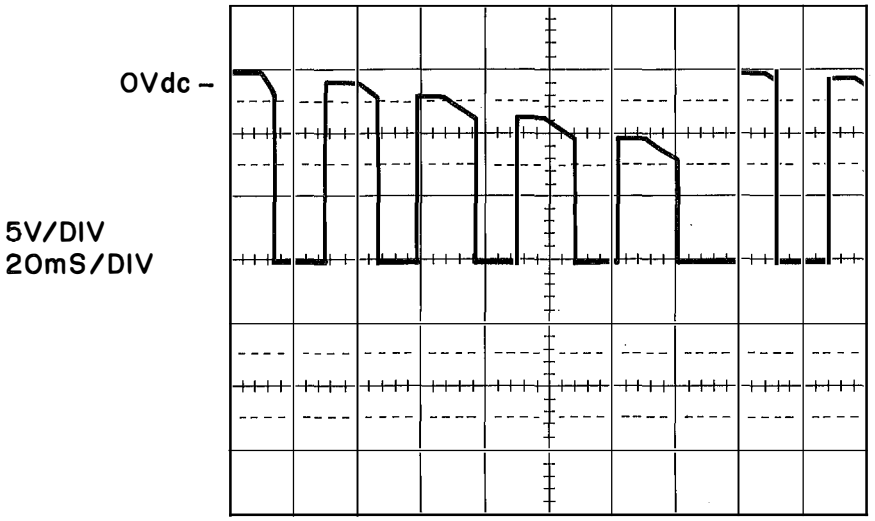
III. Connect voltmeter rear panel to +1.0 V/GHz BNC. It should vary with the instrument frequency up to at least 19V. Check test point A28 TP4 labeled V/GHz to verify correct operation. The voltage at TP4 should read -0.25 v/GHz times the instrument frequency. The voltage readings should be within the following limits at room temperature:

Frequency	-0.25 V/GHz	+1.0 V/GHz
2.2 GHz	± 5 mV	±25 mV
5 GHz	± 5 mV	±25 mV
10 GHz	± 5 mV	±35 mV
15 GHz	± 5 mV	±55 mV
18 GHz	± 5 mV	±60 mV
22 GHz	±10 mV	
26 GHz	±10 mV	

Check the waveform at TP4 (V/GHz) during a full-band sweep. There should be no discontinuities during a bandswitch. It should look like:



A. Check the voltage at the gate of Q5 during the sweep, it should have the the following waveform:



B. Check PRETUNE line at P1 Pin 22. It should read -2.5 v/GHz (relative to YO frequency).

1. Pull out A28 SYTM driver board and verify that the PRETUNE line is valid on the A54 YO Pretune board (TP3). Troubleshoot or align where necessary.

C. In CW operation, the gate of Q12 (Block H) should be at -15V. In band 0, Q11 should be at the same level as U6 pin 6 while Q13, Q14, Q15, Q16 and Q18 should be at -15V. In band 1, Q15 and Q18 should be at the same level as U6 pin 6 while Q11, Q13, Q14 and Q16 should be at -15V. In band 2, Q16 and Q18 should be at the same level as U6 pin 6 while Q11, Q13, Q14 and Q15 should be at -15V. In band 3, Q13 and Q18 should be at the same level as U6 pin 6 while Q11, Q14, Q15 and Q16 are at -15V. In band 4, Q14 and Q18 should be at the same level as U6 pin 6 while Q11, Q13, Q15 and Q16 are at -15V.

1. Check latched band information on U16 (Block I) Pins 1, 2 and 3 (P1 Pins 31, 32 and 33). Pin 1 should be HIGH in bands 0, 2 and 4 and LOW in bands 1 and 3. Pin 2 should be HIGH in bands 1 and 2 and LOW in the other bands. Pin 3 should be HIGH in bands 3 and 4 and LOW in the other bands.

2. Pull out SYTM driver board and verify the latched band information on the A27 Level Control board.

3. Verify U16, all outputs should be HIGH except for pin 14 in band 0, pin 13 in band 1, pin 12 in band 2, pin 11 in band 3 and pin 10 in band 4.

D. Check U22 (Block H) to see if it is saturated. If saturated the voltages on pins 2 and 3 will differ. Since U22 has internal input diode protection, current will shunt along the input path through the programmable voltage divider causing an error voltage to be added to the V/GHz lines.

1. Measure the voltage at A28TP5 labeled "SRS" to determine the current flowing through the SYTM coil. If the voltage is around 8V or more, the SYTM output current drive is saturated. Check for collector to emitter shorts in Q26, Q27 and the drive transistor A47Q2 on the sense resistor bracket. If the drive transistor is shorted the same voltage that appeared on the "SRS" test point should appear on A62XA28 Pin 20 with the A28 SYTM driver removed. Also verify that the gate of Q21 is at +5V in CW operation.

2. If the output of U22 is against the negative supply rail check to make sure that Q25 is conducting during CW operation.

   a. Measure the base-emitter voltages of Q26, Q27 and the drive transistor. Replace the transistors that have abnormal base-emitter voltages. Normal base-emitter voltages should be about -0.6V.

E. Check U6 (Block **E**), U5B and Q6 if still having problems with the -0.25 V/GHz line.

IV. Look at the waveform at TP5 labeled "SRS" during a sweep. R9 (Block **J**) should adjust the height of the low frequency kick pulse (about 0V), R10 should adjust the depth of the high frequency kick pulse (about 0V), and R8 (Block **H**) should adjust the overall amplitude of the waveform.

A. Check the emitters of Q24A and Q19A to verify that the pulse trigger is reaching that point.

   1. If no kick pulses are present check pin 7 of U13 (Block **I**) for a positive trigger pulse.

B. Check the inputs and ouputs of U23 and U7 to see if they become active at all.

C. If only a positive kick pulse is present, check P1 Pin 42 (SYTM COIL+). The voltage should drop to -125V $\pm$7V. If it drops to about -140V it means that the diode on the SYTM bias board is clamping the coil voltage. Check VR2 and CR11 in Block **H**. If it drops less, the zener diode on the SYTM bias board may be breaking down at too low a voltage.

V. Look at TP1 "CMP" (Block **G**) and verify that R1 (Block **A**), R2, R3, R4 and R5 (Block **C**) can affect output at 26.5 GHz. Verify that U4 (Block **C**) and R1 (Block **A**) can both increase and decrease the compensation.

VI. Look at the voltage across C26 (TP2 Block **B**) during sweep. It should look like a ramp with an offset. The knee should be rounded. This waveform should restart at each bandcrossing. The overall amplitude should vary with sweep time. R6 (DVO) should vary the height of the knee and R7 (DVS Block **B**) should vary the slope of the ramp.

A. If there is no signal check Q9, it should be gated by HSP via U18 pin 14. Check U2 pin 10 and U2A pin 1.

B. If there is no slope, or if the slope doesn't reset at bandcrossings, check Q10 (gated by HSP via U18 pin 1). Also check U5A pin 1.

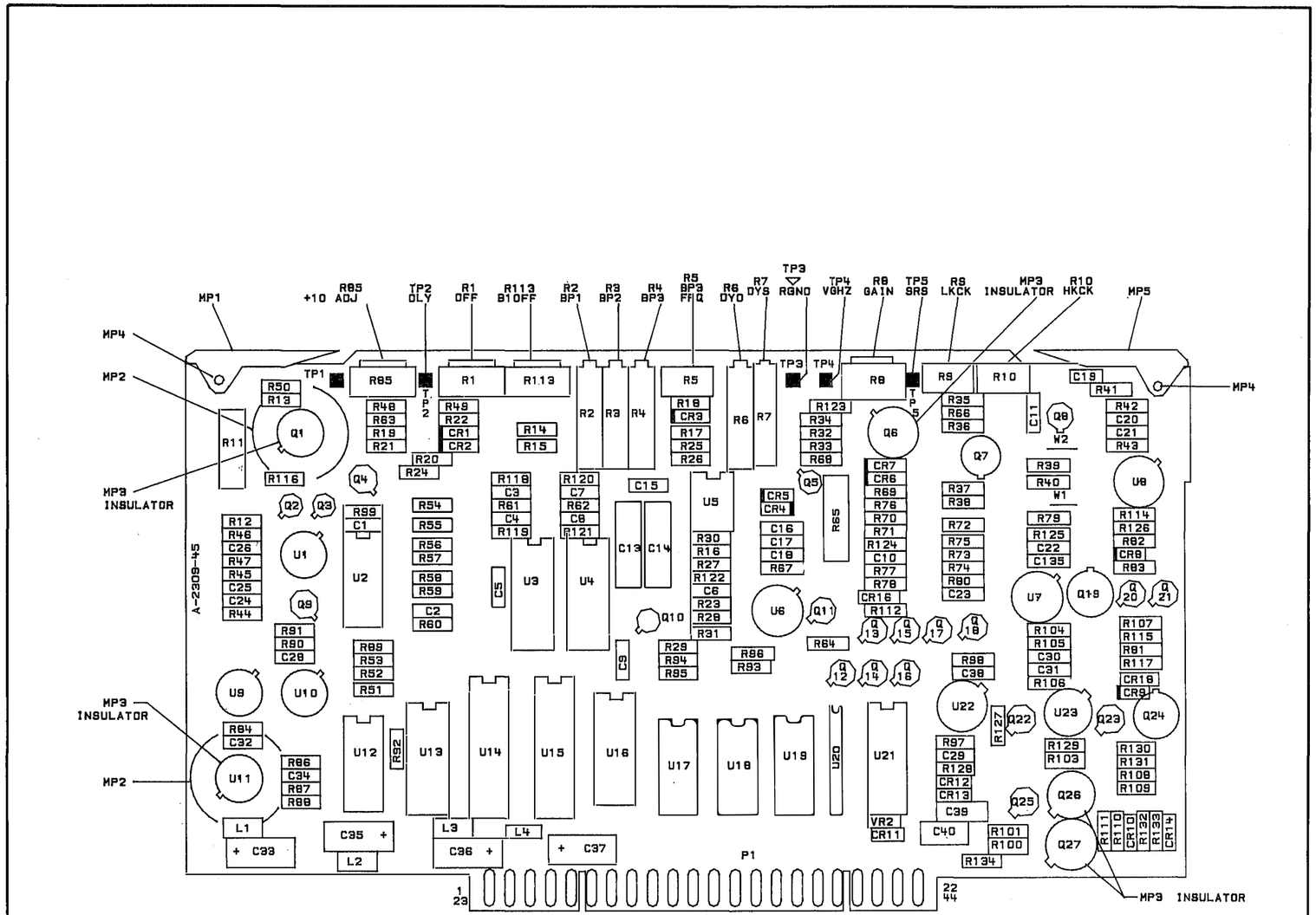


Figure 8I-40. A28 SYTM Driver, Component Location Diagram

A28 SYTM Driver P1 Pin I/O

A28

Pin	Mnemonic	Levels	Source	Destination
1 23	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*L *L
2 24	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*L *L
3 25	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*L *L
4 26	−15V HSP	−15V TTL (HIGH TRUE)	XA56P1-15, 30 XA57P1-13	*L *I
5 27	SYTM COIL −/−40V SYTM COIL −/−40V	−40V/−40V −40V/−40V	A62J18-12/XA53P1-11, 30 A62J18-12/XA53P1-11, 30	H H
6 28	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*L *L
7 29	1.4V/GHZ WBAND	+1.4V/GHZ TTL (LOW TRUE)	C XA27P1-43	XA24P1-6 B
8 30	WYTMCTL WYTMSLP	TTL (LOW TRUE) TTL (LOW TRUE)	XA27P1-14 XA27P1-44	I C
9 31	HLB0	TTL (HIGH TRUE)	XA27P1-46	*I
10 32	RSTAT HLB1	TTL (LOW TRUE) TTL (HIGH TRUE)	XA27P1-45 XA27P1-16	NOT USED *I
11 33	DB0 HLB2	TTL TTL (HIGH TRUE)	*XA60P1-20 XA27P1-47	*NOT USED *I
12 34	DB2 DB1	TTL TTL	*XA60P1-21 *XA60P1-76	*NOT USED *NOT USED
13 35	DB4 DB3	TTL TTL	*XA60P1-22 *XA60P1-77	*B C I *B C I
14 36	DB6 DB5	TTL TTL	*XA60P1-23 *XA60P1-78	*B C *B C I
15 37	DB8 DB7	TTL TTL	*XA60P1-24 *XA60P1-79	*B C *B C
16 38	DB10 DB9	TTL TTL	*XA60P1-25 *XA60P1-80	*B C *B C
17 39	+1.0V/GHZ +1.0V/GHZ RTN	1.0V/GHZ 0V	F F	A62J31-27 A62J31-13
18 40	HENDKICK −.25V/GHZ	TTL (HIGH TRUE) −.25V/GHZ	I E	XA24P1-31 *B C F H
19 41	SYTMDB YOKICK	−22V TO −39V TTL (HIGH TRUE)	H XA54P1-21	A62J32-2 I
20 42	SYTMDC SYTM COIL +	−.6V TO −6V −40V TO −25V	H H	A62J32-4 *
21 43	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*L *L
22 44	PRETUNE SYTMRES	−2.5V/GHZ 0V ≃ 2 GHZ −.9V LOW BAND CW	XA54P1-24 H	*C D E J A62J32-5

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

A28 SYTM DRIVER
(08340-60159)

NOTES:

1. REFER TO THE BEGINNING OF SECTION VIII FOR DETAILED SCHEMATIC LOGIC SYMBOLOGY NOTES.
2. RESISTANCE VALUES ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. THE A47 SENSE RESISTOR ASSEMBLY IS CONNECTED TO GROUND ON THE A2E MAIN MICROWAVE ASSEMBLY BY ITS MOUNTING HARDWARE.
4. THE VOLTAGE SENSITIVITY OF THIS LINE IS PRESET TO +5.0V/GHz, LIMITING AT 8V VOLTS. IN ORDER TO COVER THE ENTIRE FREQUENCY RANGE OF THE 8340, JUMPERS W1 AND W2 MAY BE CUT. THAT WILL CHANGE THE SENSITIVITY TO +5V/8Hz.

Figure 8I-41. A28 SYTM Driver, Schematic Diagram

(NOTE 6)

FUNCTION	LIMITS MIN	MAX
FREQUENCY(GHz)	2.3	2.7
POWER * (dBm)	+9	+16
* WITH +10 TO +16 dBm INPUT		

(NOTE 6)

FUNCTION	LIMITS MIN	MAX
FREQUENCY(GHz)	2.3	7.0
POWER * (dBm)	-4.0	--
* WITH +9dBm INPUT		

(NOTE 6)

FUNCTION	LIMITS MIN	MAX
FREQUENCY(GHz)	3.71	6.1
POWER *(dBm)	8.0	--
*WITH +9dBm INPUT AND BAND 1-4 MOD CURRENT AT A16J5=25mA		

(NOTE 6)

FUNCTION	LIMITS MIN	MAX
FREQUENCY(GHz)	2.3	7.0
POWER * (dBm)	9.5	--
* WITH +9dBm INPUT		

(NOTE 6)

FREQUENCY (GHz)	POWER LIMITS*(dBm) MIN.	MAX.
2.3 TO 3.45	+24.0	—
3.45 TO 5.75	+26.5	—
5.75 TO 6.57	+27.2	—
6.67 TO 6.75	+26.5	—
6.75 TO 7.0	+25.0	—
*WITH +9.5dBm INPUT		

(NOTE 6)

FREQUENCY (GHz)	POWER LIMITS* (dBm) MIN	MAX
0.01 TO 2.4	11.9	—
2.4 TO 7.0	16.5	—
7.0 TO 13.5	14.6	—
13.5 TO 18.6	15.0	—
18.6 TO 20.0	13.3	—
20.0 TO 23.0	11.2	—
23.0 TO 26.5	9.7	—
*WITH MINIMUM INPUT POWER OF 25.5 dBm FROM 2.3 TO 7.0 GHz AT A13J1		

(NOTE 6)

FREQUENCY (GHz)	POWER LIMITS* (dBm) MIN	MAX
0.01 TO 2.4	11.0	—
2.4 TO 7.0	15.6	—
7.0 TO 13.5	13.7	—
13.5 TO 18.6	14.1	—
18.6 TO 20.0	12.0	—
20.0 TO 23.0	9.9	—
23.0 TO 26.50	8.4	—
*WITH INPUT POWER AS SHOWN FOR A10J1		

(NOTE 6)

FUNCTION	LIMITS MIN	MAX
FREQUENCY(GHz)	3.69	3.71
POWER* (dBm)	-6.5	—
*WITH -1 dBm INPUT POWER		

(NOTE 6)

FUNCTION	LIMITS MIN	MAX
FREQUENCY(GHz)	3.69	3.71
POWER* (dBm)	-7.1	—
*WITH -6.5dBm INPUT POWER		

(NOTE 6)

FUNCTION	LIMITS MIN	MAX
FREQUENCY(GHz)	0.01	2.4
POWER* (dBm)	-20.6	-20.0
*WITH A17J1 INPUT=-7.1dBm AND A17J2 INPUT=+8 TO +18dBm		

(NOTE 6)

FUNCTION	LIMITS MIN	MAX
FREQUENCY (GHZ)	0.01	2.4
POWER* (DBM)	+18.4	—
*WITH -25 TO -20.6 dBm INPUT		

(NOTE 6)

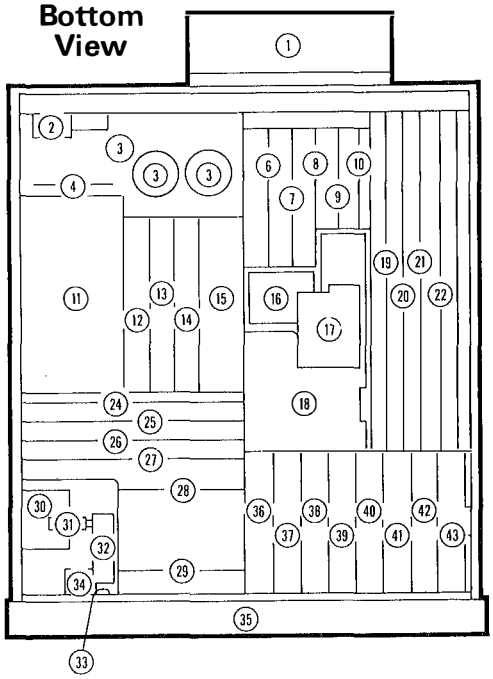
FUNCTION	LIMITS MIN	MAX
FREQUENCY (GHz)	.01	2.4
POWER* (dBm)	-12.8	—
*WITH 18.4 dBm INPUT		

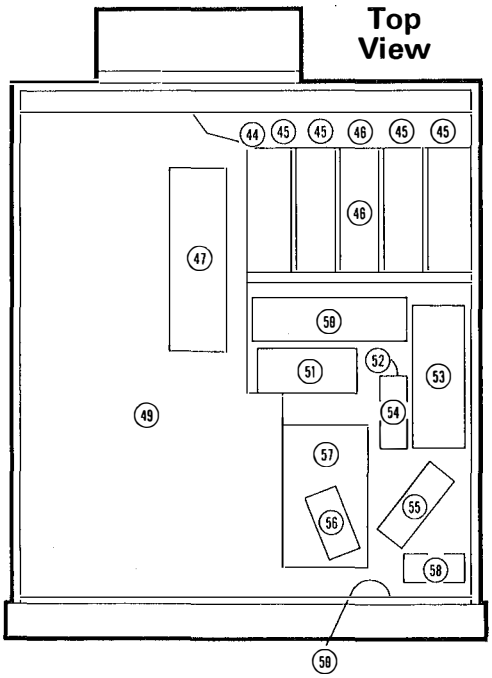
(NOTE 6)

FUNCTION	LIMITS MIN	MAX
FREQUENCY(GHz)	3.69	3.71
POWER* (dBm)	-1.0	--

Figure 8I-42. RF Section Schematic Diagram; A8 - A18, A20, A63, AT1

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 3					Volume 4		
			Ref.-M/N Loops	20-30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	33					•			
A2	Display Driver	33					•			
A3	Display Processor	33					•			
A4	Not Assigned	-								
A5	Keyboard	35					•			
A6	Keyboard Interface	35					•			
A7	Lower Keyboard	35					•			
A8	3.7 GHz Oscillator	57						•		
A9	Band 0 Pulse Modulator	56						•		
A10	Directional Coupler	32						•		
A11	Band 1-4 Detector	31						•		
A12	Band 0 Splitter/Detector	34						•		
A13	SYTM (Switched YIG Tuned Multiplier)	30						•		
A14	Band 1-4 Power Amplifier	53						•		
A15	Band 0 Low Pass Filter	52						•		
A16	Band 1-4 Modulator/Splitter	51						•		
A17	Band 0 Mixer	54						•		
A18	Band 0 Power Amplifier	55						•		
		60						•		
A19	Capacitor Assembly	48								•
A20	RF Section Filter	50						•		
A21	Pulse Modulator Driver	29						•		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						•		
A25	ALC Detector	27						•		
A26	Linear Modulator	26						•		
A27	Level Control	25						•		
A28	SYTM Driver	24						•		
A29	Reference Phase Detector	12	•							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	•							
A31	M/N Phase Detector	14	•							
A32	M/N VCO (Voltage Controlled Osc.)	15	•							
A33	M/N Output	15	•							
A34	Reference-M/N Motherboard	5	•							
A35	Rectifier	4								•
A36	PLL1 VCO (Voltage Controlled Osc.)	36		•						
A37	PLL1 Divider	37		•						
A38	PLL1 IF	38		•						
A39	PLL3 Upconverter	39		•						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		•						
A41	PLL2 Phase Detector	41		•						
A42	PLL2 Divider	42		•						
A43	PLL2 Discriminator	43		•						
A44	YIG Oscillator (YO)	18			•					
A45	Directional Coupler	18			•					
A46	7 GHz Low Pass Filter	18			•					
A47	Sense Resistor Assembly (YO circuit)	47			•					
	(SYTM circuit)	47						•		
A48	YO Loop Sampler	18			•					
A49	YO Loop Phase/Detector	18			•					
A50	YO Loop Interconnect	17			•					
A51	Reference Oscillator	16	•							
A52	Positive Regulator	6								•
A53	Negative Regulator	7								•
A54	YO Pretune/Delay Compensation	8			•					
A55	YO Driver	9			•					
A56	-15V Regulator	10								•
A57	Marker/Bandcross	19					•			
A58	Sweep Generator	20			•					
A59	Digital Interface	21					•			
A60	Processor	22					•			
A61	Not Assigned	23					•			
A62	Motherboard	49				•				
A63	90 dB RF Attenuator	59						•		
AT1	Peripheral Mode Isolator	58						•		
AT2	15 dB Attenuator	18			•					
B1	Fan Assembly	1								•
A62C1-3	Power Supply Filter Capacitors	3								•
FL1	AC Line Module	2								•
A62Q1-4	Power Supply Regulating Transistors	45								•
A62S1	Power Supply Thermal Switch	44								•
T1	Power Supply Transformer	11								•
A62U1	Power Supply Regulator	46								•

POWER SUPPLIES — FAN J

INTRODUCTION

This **POWER SUPPLIES - FAN** section provides information and instructions for troubleshooting, repairing, or replacing the 8340A Power Supply, transformer, line filter module, or fan assemblies. Information includes circuit descriptions, troubleshooting procedures, block diagrams, schematics, and component location diagrams for each printed circuit board assembly.

The **POWER SUPPLIES - FAN** functional group is made up of the following sections:

- **THEORY OF OPERATION**

  This section provides a general description of how the 8340A power supplies and rectifiers operate, which assemblies they are on, and how the power supplies are interdependent. A simplified block diagram also shows this information. This section also describes ac mains requirements, line module operation, microprocessor protection and supply failure monitoring circuitry.

- **POWER SUPPLY - TROUBLESHOOTING TO ASSEMBLY LEVEL**

  This section explains how to determine which power supply or rectifier assembly is causing the line fuse to blow or power supplies to fail. Because of the interdependency of many of the power supplies, several power supplies may be down when a single supply is causing the problem. In order to quickly find which assembly has failed, Figure 8J-3, a troubleshooting to assembly level flow chart, and Figure 8J-4, block diagram have been provided. This section also provides line module troubleshooting information.

- **REPAIR PROCEDURES**

  Specific information pertaining to personal and instrument safety are presented in this section. Replacement procedures for the transformer, line module, and fan assemblies are also presented.

- **INDIVIDUAL ASSEMBLY SERVICE SECTIONS**

  - **A19 CAPACITOR ASSEMBLY - A35 RECTIFIER ASSEMBLY - TRANSFORMER - FAN Service Section**

    This section contains the following information: circuit

descriptions, troubleshooting and repair procedures for the A19 and A35 assemblies. The circuit descriptions for each assembly are given first, then both troubleshooting guides. These are followed by the fan troubleshooting procedure. The A19 and A35 Repair procedures are located near the end of the section followed by the component location and schematic diagrams for each assembly.

- **A52 POSITIVE REGULATOR Service Section**

  Contains the circuit description, troubleshooting, and repair procedures for the A52 Positive Regulator assembly. The component and schematic diagrams are at the end of the section.

- **A53 NEGATIVE REGULATOR/A56 -15V REGULATOR Service Section**

  Contains the circuit descriptions for both assemblies followed by each troubleshooting and repair procedure. Component and schematic diagrams are at the end of the section.

POWER SUPPLIES - FAN THEORY OF OPERATION

INTRODUCTION

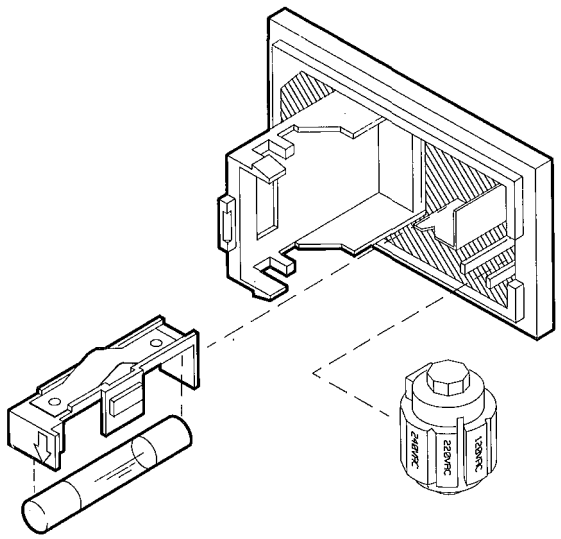
This section supplies the operator with a general knowledge of how the 8340A rectifier and regulators operate and interact with one onother. This section also specifies the ac mains voltages and frequencies the 8340A is designed to accept and describes the operation of the line module, A60 Microprocessor protection circuitry, and supply failure monitoring circuits.

AC MAINS REQUIREMENTS

The 8340A (not Option 003) can be operated at an ac mains voltage of 100, 120, 200, or 240 Vac (+10% -10%) at 47.5 to 66 Hz. Instruments equipped as Option 003 operate at 100 or 120 Vac (+10% -10%) at 360 to 440 Hz. The line filter module configures the primary inputs to the power transformer for the appropriate operating voltage. The cooling fan operates from the primary input to the power transformer. The four secondary windings provide unrectified voltages for the +22, +20, +5, -10, and -40 volt rectifiers.

LINE MODULE

The line module performs several functions. The main line fuse protects the instrument from line voltage surges, incorrect line voltage applied, internal damage due to a short in the line module, transformer, motherboard, or a rectifier board. The line module suppresses power line transients. The line voltage selector cam allows the user to easily configure the 8340A for operation at different line voltages. The selected voltage is visible through a small window (see Figure 8J-1).



CAUTION:

Do not attempt to rotate the voltage selector cam while it is installed in the line module or non-repairable damage will result. The cam must be completely removed from the line module, rotated to the proper position, and reinstalled. Refer to the instructions below.

Replacement of fuse

1. Pry open line module cover door.
2. Pull out fuse carrier.
3. Insert fuse of proper rating.
4. Place carrier back into line module

Selection of Operating Voltage

1. Pry open line module cover door.
2. **REMOVE CAM FROM THE LINE MODULE.**
3. Rotate the cam to the desired voltage. (When the line module cover is closed, the selected voltage will be visible through a small window.)
4. Insert the cam back into the line module.
5. Close the line module cover door.

Figure 8J-1. Line Module

POWER SUPPLY OPERATION

The 8340A is equipped with the following power supply assemblies: The A19 Capacitor Assembly, the A35 Rectifier Assembly, the A52 Positive Regulator Assembly, the A53 Negative Regulator Assembly, the A56 -15V Regulator Assembly, and several A62 Motherboard mounted components.

NOTE

The components mounted on the A62 Motherboard include series pass elements for the majority of the instrument power supplies.

- A19 CAPACITOR ASSEMBLY provides +20V unregulated and -10V unregulated.
- A35 RECTIFIER ASSEMBLY provides -40V unregulated, +5v unregulated, and +22V regulated.
- A52 POSITIVE REGULATOR provides +20V regulated, +12V regulated, and +5.2V regulated. This assembly also supplies REFERENCE OSCILLATOR SUPPLY, which is the +20V supply switched on or off by HIGH INTERNAL 10 MHz STANDARD ENABLE (HSTD).

- A53 NEGATIVE REGULATOR provides -5.2V regulated, -10V regulated and -40V regulated.

- A56 -15V REGULATOR uses the -40V regulated output to develop a -15V supply.

The 20 volt secondary is rectified and used by both the +20V and +22V regulators. The +22V supply is used for functions that require power when the instrument is in STANDBY mode (e.g. the oven for the 10 MHz standard, standby relay, and memory backup).

The +20V is used throughout the rest of the instrument. +20V is used to power the REFERENCE OSCILLATOR SUPPLY, the +12V supply, and also provides a reference voltage for the +5.2, -10, and -40 volt supplies. The -10V and -40V supplies power the -5.2V and -15V supplies, respectively. None of the instrument power supplies (except the +22V supply) will operate if the +20V supply fails. The +20V supply is energized with a "start-up" current source until it reaches the voltage required to power the precision +10V reference. This +10V reference serves as a voltage reference for the +20V supply. If the instrument is turned off, or if the temperature threshold of the thermal switch is exceeded, the +20V supply is shut down and all other supplies (except the +22V supply) stop functioning (all other supplies are either directly or indirectly dependent on +20V). The REFERENCE OSCILLATOR SUPPLY is provided so the internal 10 MHz reference oscillator can be turned off when an external 10 MHz reference is used.

The 5V secondary output is rectified and regulated to generate the +5.2V regulated supply.

The 10V secondary and 40V secondary outputs are rectified and regulated to power the -10V and -40V supplies. Regulation in these two supplies is accomplished by placing the series pass element in the rectifier ground return path. The return current is regulated to hold the voltage of the supply at the appropriate level.

MICROPROCESSOR PROTECTION CIRCUITRY

The +12V supply is powered by the +20V supply and is not allowed to operate until the +5.2V and -5.2V supplies are present. This circuit protects 08340-60018 processors from excessive power dissipation caused by a 5.2V supply failure. The 08340-60018 was used only in instruments with a serial prefix number of 2447A and below. Newer version(s) of this assembly do not require this protection circuit.

SUPPLY FAILURE MONITORING CIRCUITRY

HIGH POWER UP (HPUP) indicates whether or not all of the instrument power supply voltages are in the correct operating range. If the supplies are out of tolerance, HPUP will be low and LIPS (LOW INSTRUMENT PRESET) will be pulled low. Pulling LIPS low causes the A60 Microprocessor to reset, protects the instruments memory, resets the A3 Display Microprocessor and turns on all of the front panel LED's. LIPS can also be pulled low by pressing the front panel Instrument Preset button.

SIMPLIFIED BLOCK DIAGRAM

Figure 8J-2, Simplified Block Diagram, provides an overview of power supply assemblies and how they interrelate.

WARNING

Although the +22V REGULATOR is the only operational supply in STANDBY mode, all rectifiers are operational and the filter capacitors are fully charged. With the instrument connected to ac mains, there are voltages present at points inside the instrument that can cause personal injury or even death. Any servicing of this instrument with protective covers removed should be performed only by trained personnel who are aware of the hazard involved.

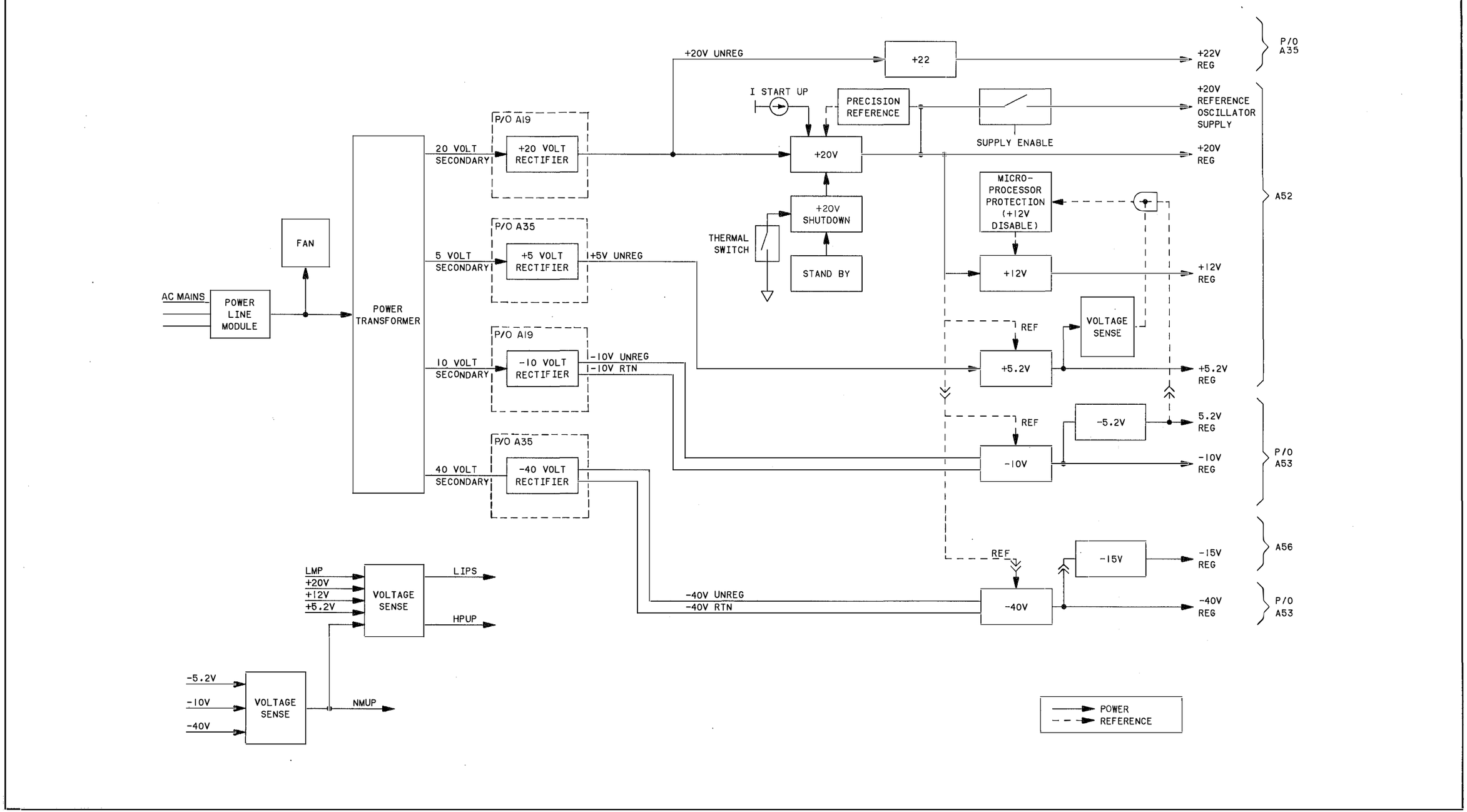


Figure 8J-2. Simplified Block Diagram

POWER SUPPLIES - FAN
TROUBLESHOOTING TO ASSEMBLY LEVEL

INTRODUCTION

This section contains information necessary to determine which rectifier or regulator assembly to troubleshoot if the instrument is blowing line fuses, if the line module is bad, or if more than one power supply is down, which supply is actually causing the problem. If more than one regulator is not operating, refer to the flowchart below.

WARNING

When connected to ac mains, there are voltages at points inside the instrument that can cause personal injury or even death. Any servicing of this instrument with protective covers removed should be performed only by trained personnel who are aware of the hazard involved.

WARNING

If the A19 POWER-ON SAFETY INDICATOR LED is on there are voltages present inside the instrument (the A62 Motherboard, the A35 and A19 Rectifier Assemblies, line filter module/transformer wiring, etc.) that can cause personal injury or even death.

CAUTION

The assemblies mentioned below contain static sensitive components. Troubleshoot these assemblies only at a work station that is equipped with an anti-static surface. Any persons working on this instrument should wear a grounding strap that provides a path to ground of no less than 1 Megohms and no more than 2.5 Megohms. All anti-static safeguards must conform to state and federal safety standards and statutes. When handling a printed circuit board, always hold it by the edges. Never touch the finger contacts.

INSTRUMENT BLOWS LINE FUSE

Initial checks:

Make sure that the line voltage selector cam is installed in the line filter module (FL1) with the proper voltage selected. Make sure ac mains voltage is nominal. Check to see if the proper value fuse is installed for the line voltage selected.

Regulator Checks

Remove ac mains and wait for the A19 POWER-ON SAFETY INDICATOR to go out. Remove the A52 Regulator Assembly. Reconnect ac mains and turn the instrument on. If the fuse blows repeat the above procedure and remove the A53 Assembly, A35 Assembly, and A19 assembly, one at a time, until the instrument stops blowing fuses. If the fuse still blows after removing all of these assemblies, suspect the A62 Motherboard, a transformer to motherboard wiring error, an FL1 wiring error, or the transformer itself.

If the line fuse stops blowing after the removing one of the above assemblies, troubleshoot that assembly. Refer to the appropriate service section.

LINE MODULE TROUBLESHOOTING

Refer to Figure 8J-8, A19 Capacitor Assembly, A35 Rectifier Assembly, Transformer, Fan, Schematic Diagram.

Make sure the main line fuse is good. Be sure to install the correct fuse for the selected line voltage (refer to the Fuse Rating Guide, located on the rear panel near the line module).

Refer to Figure 8J-5, Transformer - Line Module - Fan Replacement. Perform steps 1 and 2 of the **"Line Filter Module Replacement"** procedure. Reconnect ac mains, if the line voltage selector cam is set to 120 or 240 Vac, measure across output pins C and E. Likewise measure across output pins D and F. The voltage across each of these should be equal to the line voltage. If no voltage is present, replace the line module.

If the line voltage selector cam is set to 100 or 220 Vac, measure across output pins A and F. The voltage across these pins should be equal to the line voltage. If no voltage is present, replace the line module.

The +22V supply is the only one that is completely indendent of any other supplies. Furthermore, no other supply relies on it. The +20V supply also requires no other supplies to operate. However, all other supplies (except the +22V supply) depend either directly or indirectly on the +20V supply. There are other supply interrelationships as well. The +12V supply requires both the +5.2V and -5.2V supplies to operate (this was once needed to protect the A60 Microprocessor). The -5.2V and -15V supplies are powered directly by the -10V and -40V supplies, respectively.

In order to determine which rectifier or regulator is at fault when multiple supplies are down, or to determine if a single supply failure is being caused by the rectifier or regulator, refer to Figure 8J-3, Power Supply-Troubleshooting to Assembly Level, Flowchart. All supply interrelationships have been taken into account in this flowchart.

To determine which assembly is at fault, begin with the "START" position on the flowchart. Follow the flowchart instructions until a "TROUBLESHOOT" box is reached.

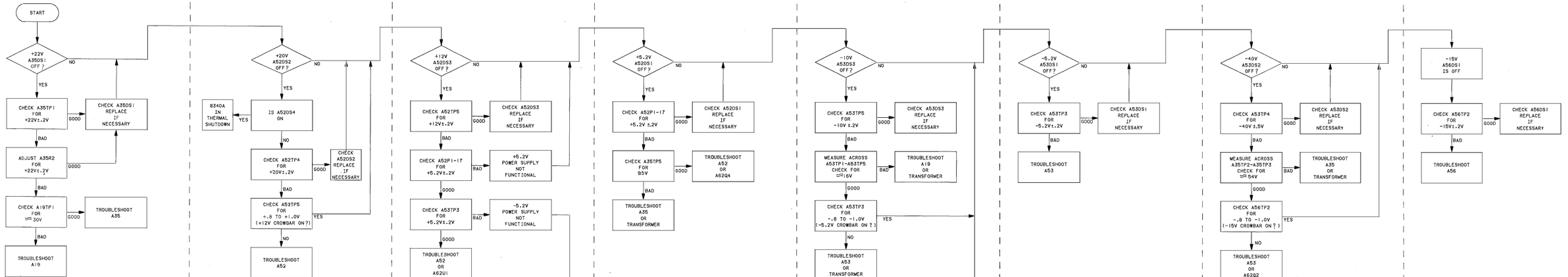


Figure 8J-3. Power Supply — Troubleshooting to Assembly Level, Flow Chart

A62J30 TO B1W1P1 PIN I/O

Pin	Mnemonic	B1W1P1	Levels
1 2	FAN 2	PIN 1	110 VAC
3	FAN 1	PIN 3	110 VAC

Note: Refer to A19 Capacitor Assembly, A35 Rectifier, and Line Power Circuits Schematic Diagram and A62 Motherboard Wiring List for signal source and destination information.

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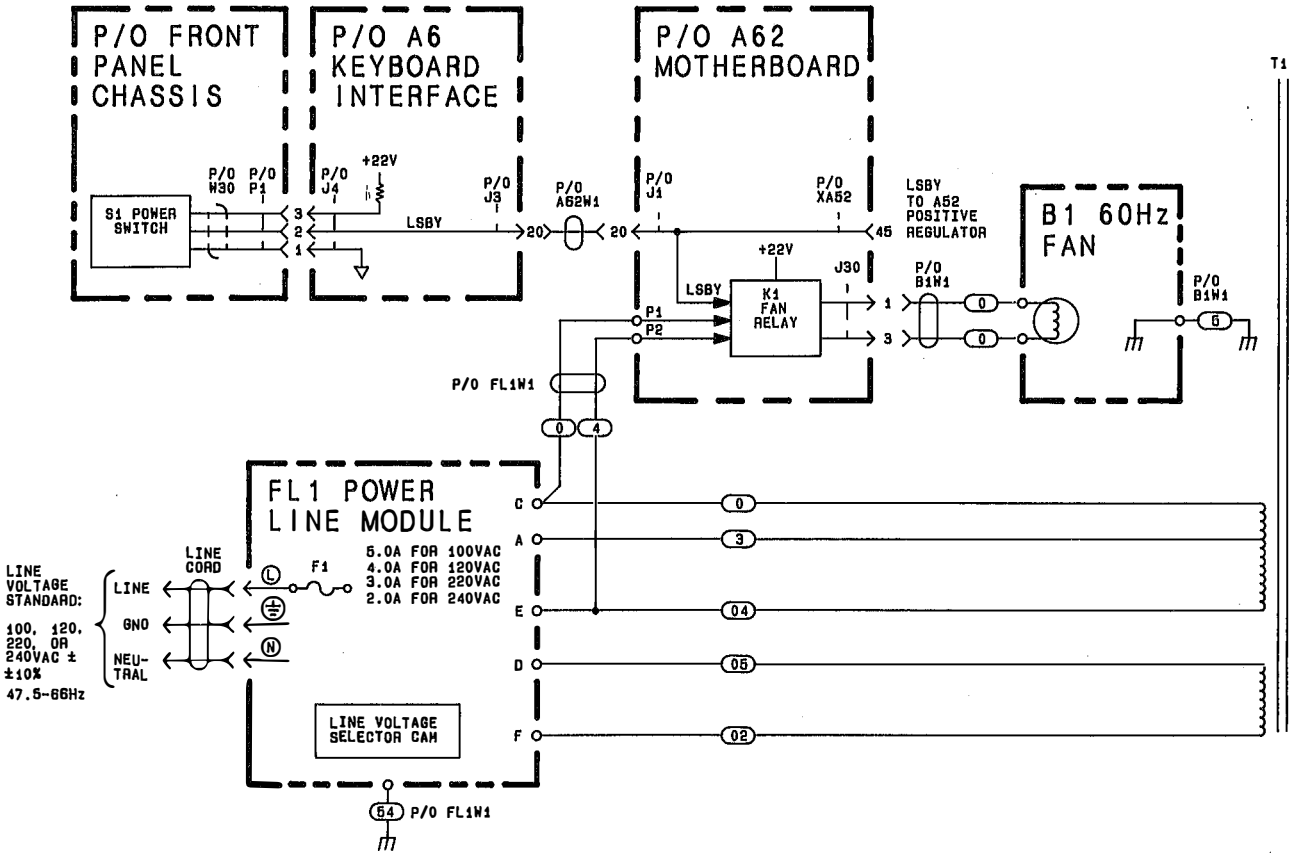


P/O Figure 8J-4. Power Supply — Troubleshooting Block Diagram

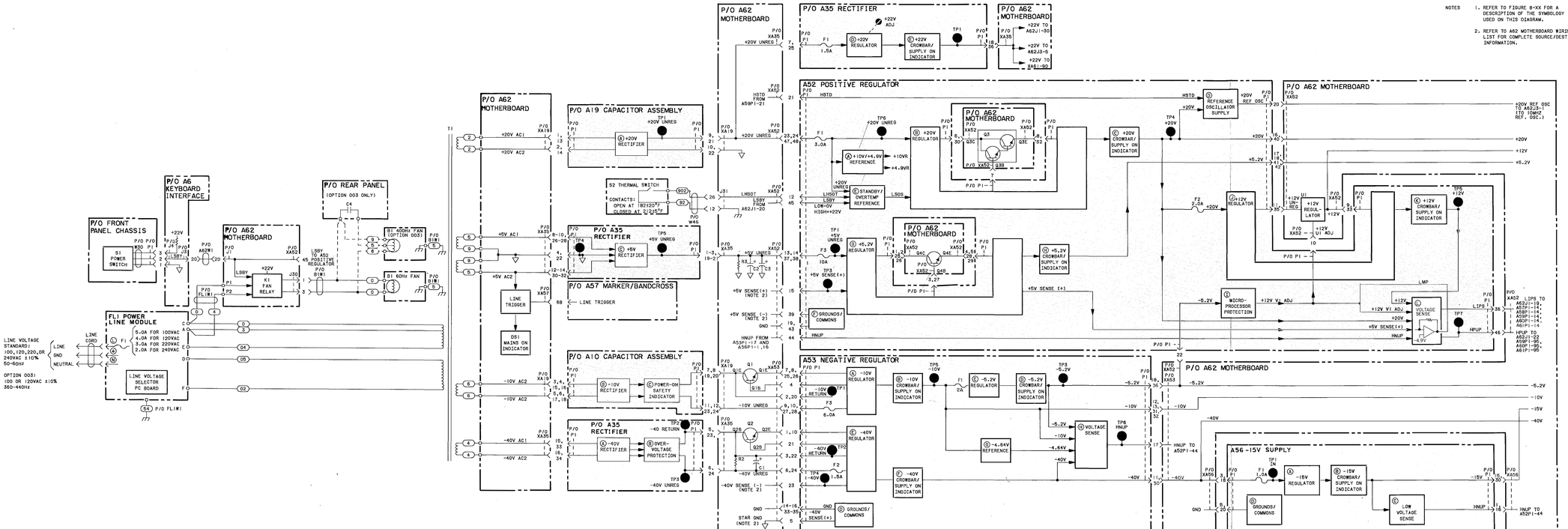


Figure 8J-4. Power Supply — Troubleshooting Block Diagram

POWER SUPPLIES — FAN REPAIR PROCEDURES

INTRODUCTION

This section contains information and/or procedures for the following:

- **SAFETY INSTRUCTIONS**
- **TRANSFORMER REPLACEMENT**
- **LINE FILTER MODULE REPLACEMENT**
- **FAN REPLACEMENT**

SAFETY INSTRUCTIONS

Read the "**SAFETY CONSIDERATIONS**" section located near the front of Volume 3. this is extremely important. The "**SAFETY CONSIDERATIONS**" section contains information vital to personal safety.

WARNING

When connected to ac mains, there are voltages at points inside the instrument that can cause personal injury or even death. Any servicing of this instrument with protective covers removed should be performed only by trained personnel who are aware of the hazard involved.

WARNING

If the A19 POWER-ON SAFETY INDICATOR LED is on there are voltages present inside the instrument (the A62 Motherboard, the A35 and A19 Rectifier Assemblies, Line Module/transformer wiring, etc.) that can cause personal injury or even death.

CAUTION

In the following procedures handling assemblies that contain static sensitive components is necessary. Handle any printed circuit board by the edges and never touch finger contacts. Execute these procedures only at a work station that is equipped with an anti-static surface. Any persons working on this instrument should wear a grounding strap that provides a path to ground of no less than 1 Megohms and no more than 2.5 Megohms. All anti-static safeguards must conform to state and federal safety standards and statutes.

Do not re-install the A19 Capacitor, A35 Rectifier, A52 Positive Regulator or A53 Negative Regulator assemblies unless ac mains has been disconnected from the instrument. Failure to observe this precaution will likely result in non-repairable damage to these assemblies.

TRANSFORMER REPLACEMENT

Recommended Special Equipment

Screwdriver, Posidriv Offset HP Part Number 8710-0949 CD1.

Removal Procedure

Refer to Figure 8J-5, Transformer-Line Module-Fan Replacement, located after the Line Module replacement procedure.

1. Disconnect the instrument from ac mains. Remove instrument top and bottom covers. The screws that hold them in place are accessible through holes in the fan housing. Remove the side panel on the transformer side of the instrument. Wait for the A19 POWER-ON SAFETY INDICATOR to go out before proceeding.

2. Remove the A19 CAPACITOR Assembly:
   a. Remove two flange screws **1**.
   b. Remove two side panel screws **2**.

3. Disconnect transformer wires from A62 Motherboard:
   a. Remove the seven screws **3** that connect the transformer secondary wires to the A62 Motherboard.
   b. Remove wire clamp screw **4** from side panel.
   c. Remove the two screws **5** that hold the blue transformer secondary wires to the bottom of the A62 Motherboard.

4. Mechanically disconnect the rear panel Assembly **6**.
   a. Invert the instrument and remove three rear panel screws **7** located on the bottom of the instrument. When these screws are removed the A35 Rectifier protective cover will come off.
   b. Remove three rear panel screws **8** located on the rear panel itself.
   c. Reach into the side of the instrument and push the rear panel out. Pull the rear panel out and away from the fan housing.

5. Desolder all transformer primary wires from Line Module, FL1.

6. Remove the four 1/4 in. screws, **9a**, and the four 3/8 in. screws, **9b**, from the side panel.

CAUTION

On some instruments with a serial prefix number of 2305A or below, the four 9a screws are too long (3/8 in). Ensure that the four 9a screws are 1/4 in. long, if

not, replace with 1/4 in. screws (HP Part Number 2360-0193). This is necessary to avoid shorting the transformer windings.

7. Remove the last two screws as follows:
   a. Remove the cables from A25J1 and A25J2.
   b. Remove the A24, A25, A26, A27, and A28 Assemblies.
   c. Remove two transformer screws, located on the side of the transformer enclosure closest to the front panel (made accessible by removing A24 through A28), with offset posidriv.
   d. Turn the instrument on its side and remove the transformer by carefully pulling out one end a little, then the other. Proceed in this way until the transformer is out.
   e. Remove the metal plate from the side of the transformer and place it on the new transformer.

New transformer Installation

1. To install the new transformer reverse steps 1 through 7 above.

NOTE

Do not allow the transformer secondary wires touch adjacent A62 Motherboard lugs when reversing step 3a. Also, make sure that the white transformer secondary wire pair is reattached to the A62 Motherboard lug labeled (9). Do not attach it to the taller unmarked lug nearby.

NOTE

Make sure the blue transformer secondary wires are all the way inside the plastic clamp when reversing step 3b. If plastic clamp hardware is mounted in the wrong side panel hole, the A19 Assembly will not go back into place.

NOTE

Reinstall the A19 CAPACITOR Assembly as follows: Lift the two grey cables out of the way, lower the A19 assembly flange end first until the finger contact end drops into place. Then lift up slightly on the flange end and push down on the finger connector side until the fingers are fully seated.

LINE MODULE REPLACEMENT

Please read this entire procedure once before proceeding.

Removal Procedure

Refer to figure 8J-5, Transformer – Line – Fan Replacement, located after this procedure.

1. Disconnect the instrument from ac mains. Remove instrument top and bottom covers. The screws that hold them in place are accessible through holes in the fan housing. Wait for the A19 Power-on Safety Indicator to go out before proceeding.
2. Remove the portion of the rear panel that holds the line module as follows (Refer to Figure 8J-5):
   a. With the instrument setting in its normal operating position, remove the two screws (**12**).
   b. Invert the instrument and remove the three rear panel screws (**7**). the protective cover for the A35 Rectifier will now come off.
   c. Remove the three rear panel screws (**13**). The fan assembly can now be moved to provide clearance for removal of the rear panel (**6**).
   d. Remove three screws (**8**) located on the rear panel itself. Reach into the instrument and push the rear panel out.
3. Desolder all wires from the line module.
4. The line module is held in by four plastic retainers and two metal clips. The metal clips are not part of the line module itself and **must** be removed before the line module will come out (see the following instructions).

   Note that the plastic retainers hold the metal clips in place. The plastic retainers must be cut off with wire cutters before the metal clips will come off. **It is important to cut the plastic away at the base of the plastic retainer completely, flush with the body of the line module and well away from the tops of the metal clips.** The metal clips will not come off easily if any of this plastic remains.

   Now, take a flat head screwdriver and pry the metal clips away from the line module. Lay them down as far as possible. They should now come free, allowing the removal of the line module.

Installation of New Line Module

1. Look on the fuse selection chart on the back of the instrument. Select the proper fuse and install it in the fuse holder (refer to the instructions in *Figure 8J-1. Line Module.* Select the proper line voltage by removing the line voltage selection cam, turning it to the proper position, and reinstalling it into the line module. Again, refer to *Figure 8J-1. Line Module* for instructions.
2. Place the metal retainers, HP Part Number 02932-00038, onto the line module. The portion of the clip that is bent 90 degrees (at each end of the clip) should fit under the plastic retainers on the line module.
3. When inserting the line module into the rear panel, make sure the line cord receptacle is on the side farthest away from the instrument's fan. Push the line module in firmly until all clips have engaged on the inside of the rear panel.
4. Wire the new line module as shown in *Figure 8J-8. A19 Capacitor Assembly, A35 Rectifier Assembly, Schematic Diagram.* Reinstall the rear panel by reversing step 2 in the removal procedure.

FAN REPLACEMENT PROCEDURE

Fan Removal

Refer to Figure 8J-5, Transformer-Line Module-Fan Replacement.

1. Disconnect the instrument from ac mains. Remove instrument top and bottom covers. Wait for the A19 POWER-ON SAFETY INDICATOR to go out before proceeding.

2. Remove two screws **12** from the rear panel frame (top of instrument).

3. Remove three screws **13** from the rear panel frame (bottom of instrument).

4. Remove the A35 protective cover **10**, A35 RECTIFIER Assembly, and the nearby capacitor cover **11**.

5. When the A35 Assembly is removed the fan cable may be disconnected from J30.

6. Remove four screws from each side of the fan housing. These screws must be discarded and replaced with new screws (HP Part Number 2200-60055, CD7).

7. Remove four screws that hold the fan filter assembly to the front of the fan.

8. Remove the two screws now accessible on the front of the fan housing. These screws must be discarded and replaced with new screws (HP Part Number 2200-60055, CD7).

9. Separate the fan housing.

10. Remove the two screws that hold the fan to the base plate. Note carefully the position of the two washers located between the fan and the base plate. Be careful to place these washers properly when reassebling the fan assembly or the fan may be permanently warped.

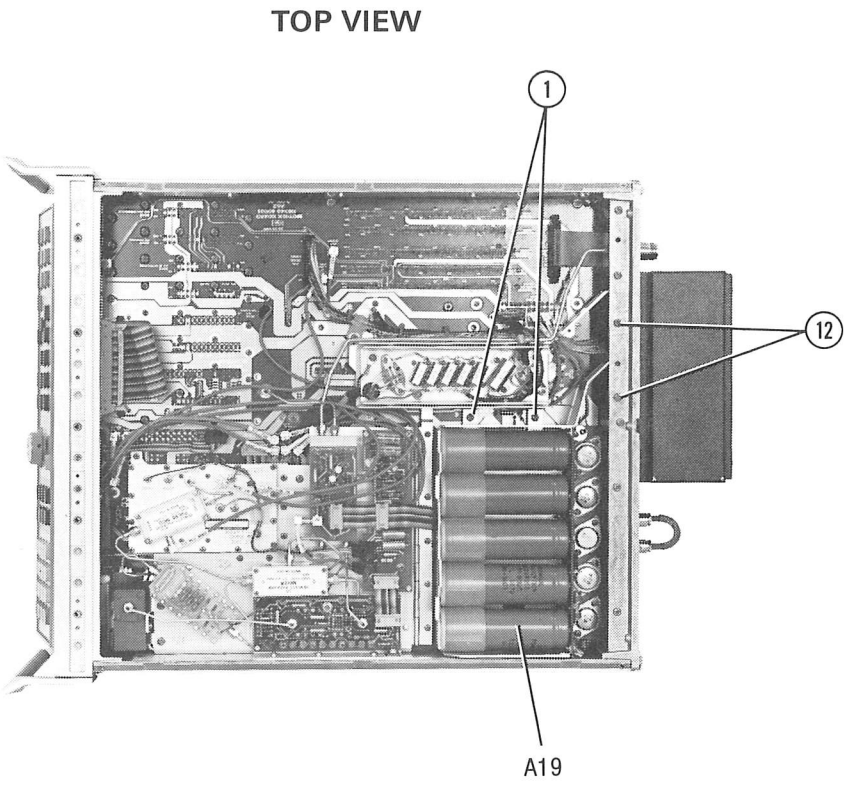
Fan Housing Assembly

To reassemble the fan housing reverse steps 1 through 10 above.

NOTE

The fan housing top (HP Part Number 08340-00012) and fan housing bottom (HP

Part Number 08340-00013) are the two parts that connect directly to the fan base plate. If instruments with a serial prefix number of 2303 or lower must have either the fan housing top or fan housing bottom replaced, both parts must be replaced.



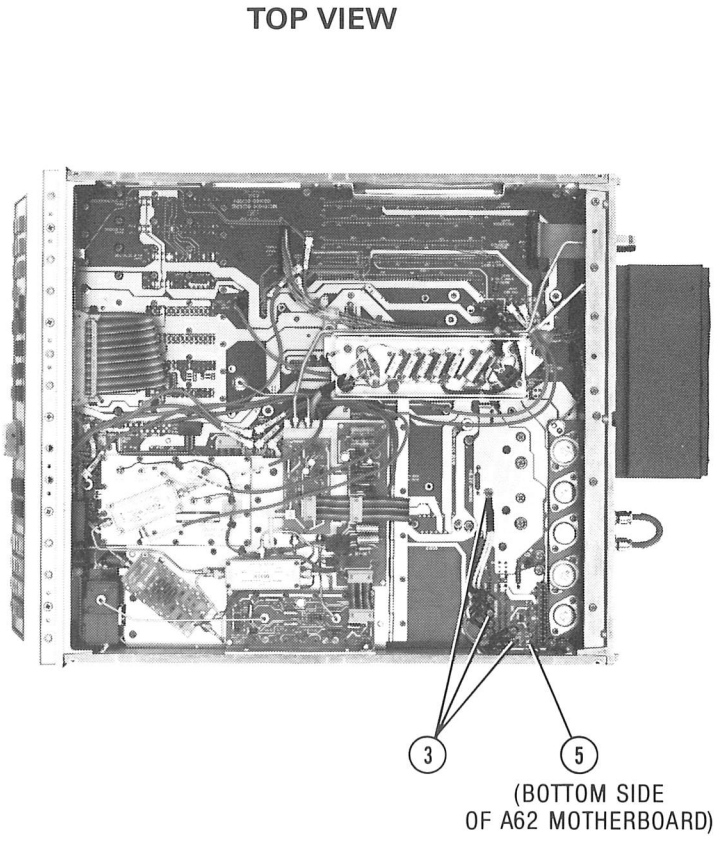


Figure 8J-5. Transformer-Line Module-Fan Replacement (1 of 2)

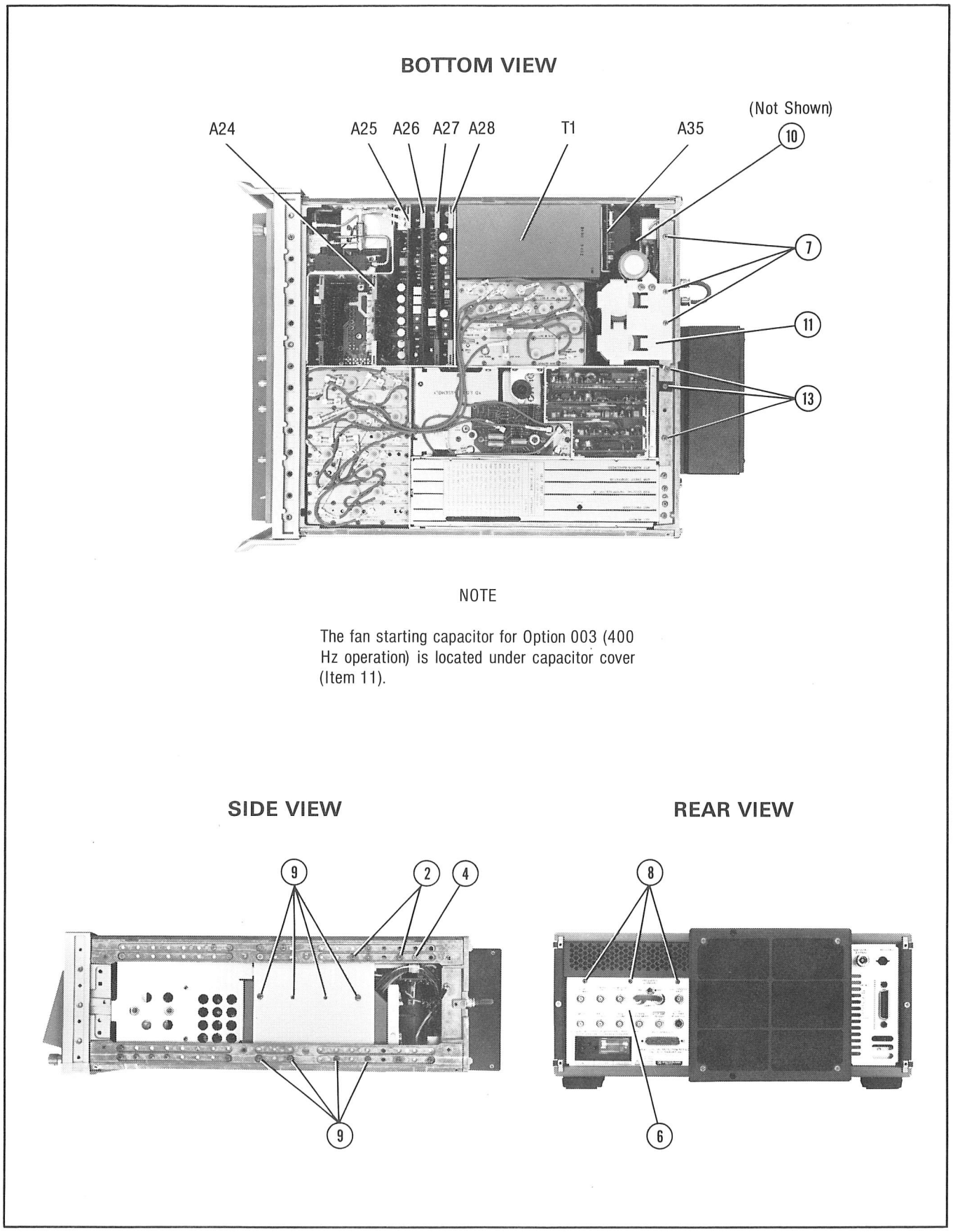


Figure 8J-5. Transformer-Line Module-Fan Replacement (2 of 2)

A19 CAPACITOR ASSEMBLY - A35 RECTIFIER ASSEMBLY TRANSFORMER - FAN

INTRODUCTION

The power supply includes the following:

- The A19 CAPACITOR Assembly.
- The A35 RECTIFIER Assembly.
- The A52 Positive Regulator Assembly.
- The A53 Negative Regulator Assembly.
- The A56 -15V Regulator Assembly.
- Several A62 Motherboard components.

Figure 8J-2 is a simplified block diagram of the power supplies. The +12V, +5.2V, -10V, and -40V power supplies are dependent upon the +20V supply. The -5.2V and -15V supplies are dependent upon the -10V and -40V supplies, respectively.

The function of the power supplies is to produce the voltages required for the 8340A. The circuit also generates the power-up flag HPUP (HIGH POWER UP). This flag is used by the microprocessor and several other circuits to control instrument activity and to ensure proper initialization.

PRIMARY POWER

Primary power is supplied to the primary of T1 through line filter module FL1, which includes a line voltage selector cam. C1 filters noise. The voltage selector cam is positioned to provide correct power connections to T1 for operation with line voltages of 100 Vac, 120 Vac, 220 Vac, or 240 Vac. Refer to **POWER SUPPLIES-FAN THEORY OF OPERATION**, for complete instructions on the correct installation of the line voltage selection cam.

STANDBY MODE

With ac mains connected and the front panel LINE switch in STANDBY, the following occurs. Power is supplied to the rectifiers on the A19 CAPACITOR and A35 RECTIFIER Assemblies. The +22V REGULATOR, located on the A35 RECTIFIER Assembly, is powered by the output of the +20V RECTIFIER (+20V UNREG). The anode of DS1 (front panel STANDBY LED) is grounded, lighting DS1. A62K1 switches (closes) into STANDBY (fan B1 remains OFF) and LOW STANDBY (LSBY) disables the +20V REGULATOR. A62CR2 is placed across the coil of the A62K1 relay to remove the inductive kickback that would occur when the 8340 is switched from STANDBY

to ON. The A62K1 relay is connected so that power is normally supplied to the fan (B1). Switching to STANDBY grounds A62K1 pin 1 and energizes the relay, removing power from the fan (B1). When the +20V supply is disabled, all other supplies (except the +22V supply) are disabled. Other LEDs that are ON are A62DS1 (MAINS-ON indicator), A19DS1 (POWER-ON SAFETY INDICATOR) and A35DS1 (+22V supply operational indicator).

WARNING

Although the +22V REGULATOR is the only operational supply, ac mains are present, the rectifiers are fully operational and the filter capacitors are fully charged.

When the LINE switch is moved from STANDBY to ON, A62K1 pin 1 is disconnected from ground, allowing power to go to the fan (B1). Simultaneously, LSBY goes from 0V to +22V which allows the +20V supply and other supplies to become operational.

A19 CAPACITOR ASSEMBLY, CIRCUIT DESCRIPTION

Introduction

The A19 CAPACITOR Assembly contains the full-wave bridge rectifiers and line filters for the +20V, and the -10V power supplies. Also located on the board is a POWER-ON SAFETY INDICATOR for the safety of the service technician. If the POWER-ON SAFETY INDICATOR is illuminated (See **"POWER-ON SAFETY INDICATOR Circuit C"**, below), there will be hazardous voltages present directly beneath the A19 assembly on the A62 Motherboard.

All components referenced below are on the A19 Assembly unless otherwise noted.

+20V RECTIFIER Circuit A

The +20V full-wave bridge rectifier consists of CR1 through CR4. C3 and C10 form a high frequency filter that suppresses conducted line emissions by attenuating diode reverse recovery transients. C1 decreases the high frequency currents on the +20V UNREG line. C5 and C6 are the main filter capacitors; R1 and R4 form a bleeder resistor.

-10V RECTIFIER Circuit B

The -10V full-wave bridge rectifier includes CR5 through CR8; these are schottky barrier power rectifiers and are used here to increase the efficiency of the low voltage power supplies. C4 is a high frequency filter to suppress conducted line emissions. C7, C8, and C9 are the line filter capacitors and R2 is a bleeder resistor. C2 decreases the high frequency currents on the -10V UNREG line.

POWER-ON SAFETY INDICATOR Circuit C

The POWER-ON LED (DS1) should be ON whenever the unregulated supply filter capacitors still store enough energy to present a potential safety hazard. Since the 8340A has no ON/OFF line power switch, if ac mains are connected, the unregulated supplies and +22V regulated supply are active.

A35 RECTIFIER ASSEMBLY, CIRCUIT DESCRIPTION

Introduction

The A35 Rectifier Assembly consists of the following:

- **-40V RECTIFIER Circuit.**
- **OVERVOLTAGE PROTECTION Circuit.**
- **+5V RECTIFIER Circuit.**
- **+22V REGULATOR Circuit.**

All components referenced below are on the A35 Assembly unless otherwise noted.

-40V RECTIFIER Circuit A

The -40V RECTIFIER consists of CR1 through CR4. C1 is the high frequency filter that decreases conducted line emissions. C5 decreases the high frequency currents on the -40V UNREG line.

OVERVOLTAGE PROTECTION Circuit B

The OVERVOLTAGE PROTECTION circuitry is a simple crowbar circuit that is fired in the event that the line voltage selector printed circuit board is set to a low line voltage and the instrument is mistakenly plugged into a high voltage outlet. VR1 starts to conduct as the voltage across it reaches 82.5V, biasing crowbar SCR Q1 on and shorting the 40V transformer winding during each positive half-cycle of the ac mains. This blows the main fuse in the line module.

+5V RECTIFIER Circuit C

The +5V RECTIFIER is arranged in a full-wave, center-tapped configuration for efficiency (e.g. only one rectifier in series with the load at any time, as opposed to two for a bridge configuration). Power rectifier U1 is a single-chip dual schottky barrier rectifier in a TO-3 package. C2 and C3 are the high frequency filters that decrease conducted line emissions. C7 decreases the high frequency currents on the +5V UNREG line.

+22V REGULATOR Circuit D

The +22V REGULATOR consists of U2 (a three terminal adjustable regulator), the adjustment circuitry (R1, R2, and R3), and ripple rejection capacitors C8 and C10. CR7 prevents C8 and C10 from discharging into U2 if the input to U2 is shorted or when line power is removed. CR5 and CR6 protect the +22V loads from damage due to reverse polarity power supply voltages in the event of

some instrument fault. For example, without CR5 and CR6 a direct short between the +22V and -10V power supplies occured, the -10V supply would overpower the +22V standby supply and reverse its polarity.

NOTE

This supply is continuously active as long as the instrument is connected to ac mains.

+22V CROWBAR/SUPPLY-ON INDICATOR Circuit E

In the event of an overvoltage condition on the +22V regulated output, VR2 will conduct, biasing crowbar SCR Q2 on and shorting the +22V supply to ground. This protects the instrument +22V loads from damage due to an overvoltage condition. C9 filters transients to prevent premature firing of Q2. The POWER-ON SAFETY INDICATOR consists of DS1, R4, and VR3. DS1 will begin to light when the regulator supply voltage reaches +17V.

+22V Supply Tolerance

The tolerance of the +22V supply is +22V $\pm$5% (1.1V).

P/O A62 MOTHERBOARD ASSEMBLY CIRCUIT DESCRIPTION

The A62 Motherboard distributes all secondary ac and unregulated dc power to those printed circuit boards requiring these voltages. The MAINS-ON indicator (consisting of DS1, R1, and CR1) is active whenever the instrument is plugged into the ac mains. It's function is to warn the service technician that hazardous voltages are present on the Motherboard in the power supply area. (The same circuit is used to generate the 60 Hz LINE TRIGGER signal for the internal sweep circuitry). If DS1 fails to light when ac mains are connected, suspect a DS1 failure. A failure of DS1 should not cause failure of the LINE TRIGGER function.

The instrument power supply heat sink is located on the rear panel. It is the primary cooling system for the +20, +12, +5.2, -10, and -40 Volt power supply series pass elements. Figure 8J-14. Power Supplies Major Assembly Location Diagram, illustrates the placement and identity of these series pass elements on the A63 Motherboard/Heatsink.

A19 CAPACITOR ASSEMBLY, TROUBLESHOOTING

WARNING

When connected to ac mains, there are voltages at points inside the instrument that can cause personal injury or even death. Any servicing of this instrument with protective covers removed should be performed only by trained personnel who are aware of the hazard involved.

WARNING

If the A19 POWER-ON SAFETY INDICATOR LED is on there are voltages present inside the instrument (the A62 Motherboard, the A35 and A19 Rectifier Assemblies, line filter module/transformer wiring, etc.) that can cause personal injury or even death.

CAUTION

Do not remove the crowbar and operate the supply without it. This could cause severe damage to the instrument if the supply is faulty and the crowbar has engaged to protect the instrument.

CAUTION

The A19 Assembly contains static sensitive components. Troubleshoot this assembly only at a work station that is equipped with an anti-static surface. Any persons working on this instrument should wear a grounding strap that provides a path to ground of no less than 1 Megohms and no more than 2.5 Megohms. All anti-static safeguards must conform to state and federal safety standards and statutes. When handling a printed circuit board, always hold it by the edges. Never touch the finger contacts.

Introduction

When POWER-ON SAFETY INDICATOR LED DS1 is on, it is warning the service technician that hazardous voltages exist on the A62

Motherboard, beneath the A19 CAPACITOR Assembly. Wait for this LED to go out before removing the A19 Capacitor Assembly to place it on an extender board. This extender board is designed assuming the instrument is on its left side (ON/STANDBY switch down, output connector up), with the A19 Capacitor Assembly resting on the side rail.

Main Line Fuse Blows

If the instrument blows the line fuse, refer to the **"INSTRUMENT BLOWS LINE FUSE"** section of the **"POWER SUPPLY - TROUBLESHOOTING TO ASSEMBLY LEVEL"** functional group. If the tests contained in the above functional group indicate that this assembly is at fault, proceed as follows:

Remove aluminum electrolytic capacitors C5 through C9. If the problem dissappears, one of these capacitors is shorted. Use a process of elimination to discover which capacitor is defective. If the problem persists, try to isolate the cause to one of the two rectifier circuits as follows: The transformer secondary windings that power the rectifiers first go to the A62 Motherboard where they are attached with screws. Remove ac mains from the instrument, wait for the POWER-ON SAFETY INDICATOR to go out. Remove the A19 Assemby (to make the screws accessable) and remove one of the red secondary wires that power the +20V RECTIFIER (be careful to isolate the exposed wire from all other circuits on the motherboard). Reinstall the A19 Assembly and reconnect ac mains. Repeat this procedure to disconnect the -10V secondary if necessary. If either rectifier circuit is at fault, suspect a shorted component. If the problem persists, suspect an A62 Motherboard short.

+20V Rectifier Output Voltage Incorrect

Make sure the instrument is in STANDBY and ac mains are nominal (120V in the 120V line option, etc.). Ensure that the line voltage selector printed circuit board is installed properly. Measure A19TP1 (or directly across C5 or C6) for +35V. If the voltage is low disconnect ac mains and wait for the POWER-ON SAFETY INDICATOR to go out. Remove the A35 and A52 assemblies. Connect ac mains and measure TP1 again. If the voltage at TP1 is now approximately +35VDC, proceed as follows: While observing all safety precautions mentioned above, reinstall A35 and A52 one at a time to determine which one is at fault. Refer to the appropriate troubleshooting guide.

If the problem persists after the A35 and A52 are both removed, suspect an open rectifier diode. If these are funtional, suspect the transformer.

-10V RECTIFIER Output Voltage Incorrect

Troubleshooting is similar to the **"+20V RECTIFIER Output Voltage Incorrect"** troubleshooting section, above. Check for +18VDC directly across C7, C8, or C9. Any **"+20V RECTIFIER Output Voltage Incorrect"** instructions that pertain to the A35 and A52 assemblies pertain to the A53 assembly when troubleshooting the -10V RECTIFIER. If DS1 is out, but the -10V UNREG voltage level appears correct, check DS1 and R3.

A35 RECTIFIER ASSEMBLY, TROUBLESHOOTING

WARNING

When connected to ac mains, there are voltages at points inside the instrument that can cause personal injury or even death. Any servicing of this instrument with protective covers removed should be performed only by trained personnel who are aware of the hazard involved.

WARNING

If the A19 POWER-ON SAFETY INDICATOR LED is on there are voltages present inside the instrument (the A62 Motherboard, the A35 and A19 Rectifier Assemblies, line filter module/transformer wiring, etc.) that can cause personal injury or even death.

CAUTION

The A35 Assembly contains static sensitive components. Troubleshoot this assembly only at a work station that is equipped with an anti-static surface. Any persons working on this instrument should wear a grounding strap that provides a path to ground of no less than 1 Megohms and no more than 2.5 Megohms. All anti-static safeguards must conform to state and federal safety standards and statutes. When handling a printed circuit board, always hold it by the edges. Never touch the finger contacts.

CAUTION

Do not remove the crowbar and operate the supply without it. This could cause severe damage to the instrument if the supply is faulty and the crowbar has engaged to protect the instrument.

Since the A35 Rectifier Assembly contains three separate and isolated power circuits, each circuit can be considered separately.

-40V RECTIFIER Troubleshooting

The -40V RECTIFIER is straightforward, and troubleshooting follows the same logic as pointed out in troubleshooting the A19 Capacitor Assembly. When a crowbar SCR fails, it will usually short. If the instrument blows line fuses and the problem is traced to the A35 Rectifier Assembly, check Q1 for a short (this could also be due to a shorted VR1). If the overvoltage protection circuit does not work, it is probably due to an open VR1.

+5V RECTIFIER Troubleshooting

The +5V RECTIFIER has only two diodes which are both in one TO-3 package. If this unregulated supply malfunctions, check the diodes for open or shorted condition failures.

+22V REGULATOR Troubleshooting

The +22V REGULATOR source is the +20V UNREG line. the A19 Capacitor Assembly must therefore be present to test this regulator. The tolerance of this supply is +22V $\pm$5% (1.1V).

SUPPLY/LOAD FAILURE DETERMINATION

Disconnect the instrument from ac mains. After the POWER-ON SAFETY INDICATOR goes out remove the A35 Assembly and place it on an extender board. Apply thin, colored, non-conductive tape to the extender board +22V output pins (use of colored tape is recommended because transparent tape may be forgotten and left on the extender board, causing unnecessary troubleshooting). Do not apply tape to A35 printed circuit board fingers. Re-install the A35 Assembly and connect ac mains to the instrument. If the power supply now operates properly suspect a short on one of the instrument assemblies that use +22V. Refer to Table 8J-11, Power Supply Destination Chart at the end of the **"POWER SUPPLY - FAN"** functional group, for a list of these assemblies. After removing tape from extender board fingers clean fingers according to the following instructions:

CAUTION

Cleaning P.C. Board fingers by any other method than the one described below may cause serious reliability problems. NEVER clean fingers with any kind of eraser. NEVER use tap water in the cleaning solution described below. Tap water contains chlorine. Chloride contamination from tap water, salt (from skin contact),

or any other source may cause serious reliability problems. Always wear a ground strap when handling any 8340 internal component or assembly.

Printed Circuit Board Finger Cleaning Procedure

Mix one part deionized water with two parts isopropyl alcohol. Apply this solution to a clean, lint free, cloth (HP Part Number 9310-0039 CD3). Rub the fingers carefully and then dry with a clean part of the cloth.

Refer to the appropriate section below:

- +22V Load Failure
- +22V Power Supply Failure

+22V Load Failure

If the problem is load related repeat the above procedure for safe removal of the A35 Assembly, remove the tape from the extender board's +22V output pins, clean the fingers as described above, and reinstall the A35 assembly. It will be necessary to remove each assembly that uses +22V, one at a time, to determine which one is faulty. Likewise remove any cables listed that carry the affected supply. Refer to Table 8J-11, Power Supply Destination Chart, located at the end of the **"POWER SUPPLY - FAN"** functional group, for a list of these assemblies. Always remove ac mains and wait for the POWER-ON SAFETY INDICATOR to go out before removing or installing any assembly or cable.

+22V Power Supply Failure

If the power supply output does not return to normal after the extender board +22V output pins are taped off, refer to the appropriate sections below:

- +22V output voltage approximately .8V to 1.0V.
- +22V output voltage approximately 0V.
- +22V output voltage incorrect. Tolerance is +22V $\pm$5% (1.1V).

+22V output voltage approximately .8V to 1.0V.

Crowbar circuit verification - If the output voltage is approximately .8V to 1.0V the crowbar circuit is engaged. Connect the instrument to an auto-transformer set for 0V output. While monitoring the supply output voltage slowly

increase the auto-transformer output voltage. If the crowbar fires before the supply output reaches +22V suspect A35VR2.

Regulator verification - If the power supply output reaches +22V stop increasing auto-transformer voltage. Measure the voltage across pin 1 and the case of U2 (regulator). If the voltage is not approximately 1.25V suspect U2. Measure the voltage from the input and the output of U2. If there is little or no voltage U2 is probably shorted.

+22V output voltage approximately 0V.

Initial checks - Ensure that ac mains voltage is nominal and that the line voltage selector PC Board is installed properly in the line filter module, FL1. Make sure the proper fuse value is installed. If the above is correct and the power supply input fuse (F1) is blown, suspect regulator A35U2.

Regulator verification - Measure across pin 1 and the case of U2. If the voltage is not approximately 1.25V suspect U2.

Measure the +20V UNREG (P1-7). If this voltage is less than approximately +30V, troubleshoot the +20V Rectifier. Refer to the A19 troubleshooting guide.

Examine the +22V supply for burnt or discolored components. Suspect a shorted capacitor, diode, or crowbar SCR if the above mentioned procedures to not isolate the problem.

+22V output voltage incorrect. Tolerance is +22V $\pm$5% (1.1V).

Ensure that ac mains voltage is nominal and that the line voltage selector PC Board is installed with the proper line voltage selected.

Measure the +20V UNREG input with respect to ground. If the voltage is less than approximately +30V troubleshoot the +20V Rectifier. Refer to the A19 Troubleshooting Guide.

Measure the output voltage with an HP 1740A or similar Oscilloscope. Make sure the supply is not oscillating.

If the output is approximately 1.25V C10 is probably shorted.

FAN TROUBLESHOOTING PROCEDURES

WARNING

When connected to ac mains, there are voltages at points inside the instrument that can cause personal injury or even death. Any servicing of this instrument with protective covers removed should be performed only by trained personnel who are aware of the hazard involved.

WARNING

If the A19 POWER-ON SAFETY INDICATOR LED is on there are voltages present inside the instrument (the A62 Motherboard, the A35 and A19 Rectifier Assemblies, line filter module/transformer wiring, etc.) that can cause personal injury or even death.

Fan Inoperative/Slow

Make sure ac mains are nominal and that the line voltage selector PC Board in the line filter module is set to the correct voltage. Disconnect ac mains from the instrument. Remove the instruments top and bottom covers. The screws that hold them in place are accessible through holes in the fan housing. Wait for A19 POWER-ON SAFETY INDICATOR to go out. Remove the A35 RECTIFIER Assembly. Disconnect the fan power cord from A62J30 (located under the A35 Assembly). Connect ac mains, turn the Line switch on, and measure the voltage at A62J30. Make sure the voltage is approximately 120V. If it is not troubleshoot the K1 relay or the line filter module. If the voltage is correct disassemble the fan housing assembly as follows:

Disconnect ac mains. Turn the instrument on its side and Remove the four screws on each side of the fan housing. These screws must be discarded and replaced with new screws (HP Part Number 2200-60055, CD7). Remove the four screws that hold on the fan filter assembly. Remove the two screws now accessible on the front of the fan housing. The latter two screws must be discarded and replaced with new screws (HP Part Number 2200-60055, CD7). Separate fan housing.

Reconnect the fan power cord to A62J30. Remove the access plate on the fan where the power cord is attached. Connect ac mains and turn the Line switch on. Measure the voltage across the power terminals. If the voltage is not approximately 120V suspect the

fan power cable. It the voltage is correct, suspect the starting capacitor (on Option 400 units only), or the fan itself. Refer to the **"FAN REPLACEMENT PROCEDURE"** in the **"REPAIR PROCEDURES"** section for complete fan replacement instructions.

A19 REPAIR PROCEDURES

CAUTION

Never short a capacitor with a screwdriver or similar tool.

Capacitor Replacement

When installing a replacement electrolytic capacitor, make sure the capacitor's pressure relief valve is directly over the hole in the PC Board. This ensures that capacitor polarity is correct.

A35 REPAIR PROCEDURES

See all warnings and cautions mentioned above in the **"A19 REPAIR PROCEDURES"** section.

CAUTION

The thermal connection between the voltage regulator A35U2, the full wave rectifier A35U1, and the A35 heat sink is the dominant factor in the two device's long term reliability. Be sure to properly apply thermal compound (HP Part Number 6040-0454 CD0) when installing or replacing either of these parts.

CAUTION

Use only oil based thermal compound. The use of silicone based thermal compound may cause serious reliability problems. Silicone based oil migrates to pass element sockets, switch contacts, or printed circuit board edge connectors. The compound then tends to raise contact resistance or electrically isolate the contacts. Silicone based thermal compounds disperse into the air and deposit themselves anywhere in the instrument. Applying this material to a warm component (e.g. a heat sink or pass element) increases the rate of dispersion.

Thermal Compound Application

When installing or replacing a pass transistor or voltage regulator make sure thermal compound is applied as described below:

Apply a thin coating of thermal compound (HP Part Number 6040-0454 CD0) to both sides of the insulating washer. The coating should be just thick enough to provide a thin but continuous layer of compound from component-to-washer and washer-to-heat sink. An excessive amount of heat sink compound impairs its ability to transfer heat. The pass element mounting screws should be tightened with seven inch-pounds of force. Tightening with less force diminishes the heat transfer capability of the thermal compound. Tightening with greater force may damage the mounting hardware.

TRANSFORMER REPLACEMENT PROCEDURE

For transformer replacement instructions refer to **"TRANSFORMER REPLACEMENT"** in the **"REPAIR PROCEDURES"** section of this functional group.

FAN REPLACEMENT PROCEDURE

Refer to the **"FAN REPLACEMENT PROCEDURE"** in the **"REPAIR PROCEDURES"** section of this functional group.

Table 8J-1. A35 Rectifier, Regulated Supply Limit

Power Supply	DMM Probe	Ground	Limit
+22V	A35TP1	A35TP4	+20.90V to +23.10V

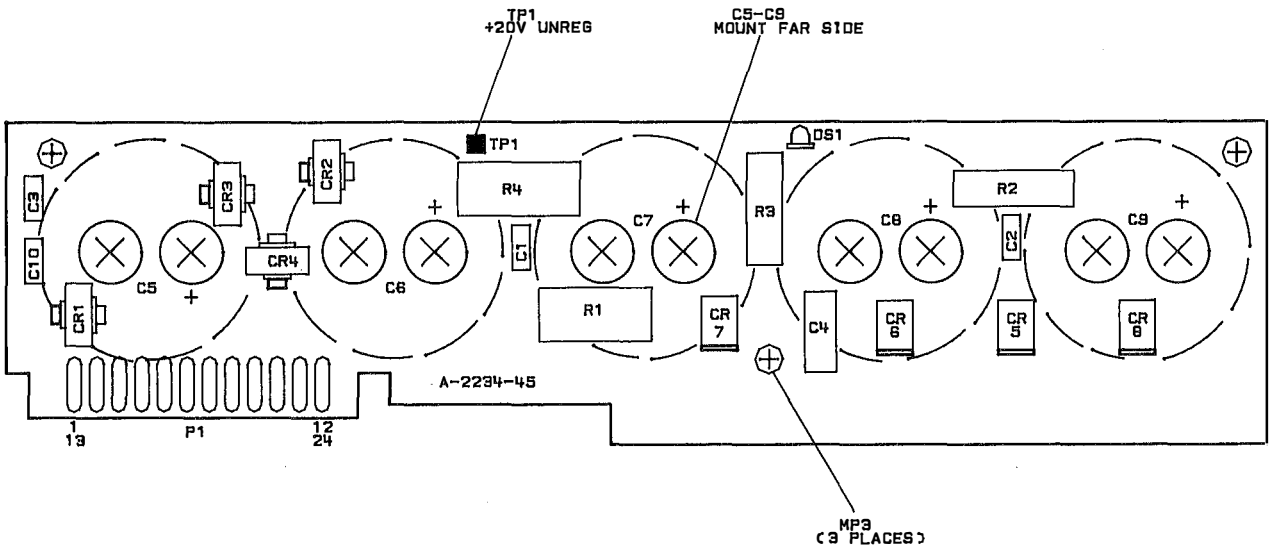


Figure 8J-6. A19 Capacitor Assembly, Component Location Diagram

A19 Capacitor Assembly P1 Pin I/O

A19

Pin	Mnemonic	Levels	Source	Destination
1	+20V AC1	+20 VAC	A62 LUG (2)	*A
13	+20V AC1	+20 VAC	A62 LUG (2)	*A
2	+20V AC2	+20 VAC	A62 LUG (2)	*A
14	+20V AC2	+20 VAC	A62 LUG (2)	*A
3	−10V AC1	−10 VAC	A62 LUG (6)	*B
15	−10V AC1	−10 VAC	A62 LUG (6)	*B
4	−10V AC1	−10 VAC	A62 LUG (6)	*B
16	−10V AC1	−10 VAC	A62 LUG (6)	*B
5	−10V AC2	−10 VAC	A62 LUG (6)	*B
17	−10V AC2	−10 VAC	A62 LUG (6)	*B
6	−10V AC2	−10 VAC	A62 LUG (6)	*B
18	−10V AC2	−10 VAC	A62 LUG (6)	*B
7	−10V RETURN	+6.4V AT 13.3 GHZ	XA53P1-2, 20	B C
19	−10V RETURN	+6.4V AT 13.3 GHZ	XA53P1-2, 20	B C
8	−10V RETURN	+6.4V AT 13.3 GHZ	XA53P1-2, 20	B C
20	−10V RETURN	+6.4V AT 13.3 GHZ	XA53P1-2, 20	B C
9	+20V UNREG	+31.2V	XA35P1-7, 25	*A
21	+20V UNREG	+31.2V	XA35P1-7, 25	*A
10	GND	0V	A62 STAR GND	*A
22	GND	0V	A62 STAR GND	*A
11	−10V UNREG	−10V	B C	XA53P1-27, 28
23	−10V UNREG	−10V	B C	XA53P1-27, 28
12	−10V UNREG	−10V	B C	XA53P1-27, 28
24	−10V UNREG	−10V	B C	XA53P1-27, 28

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

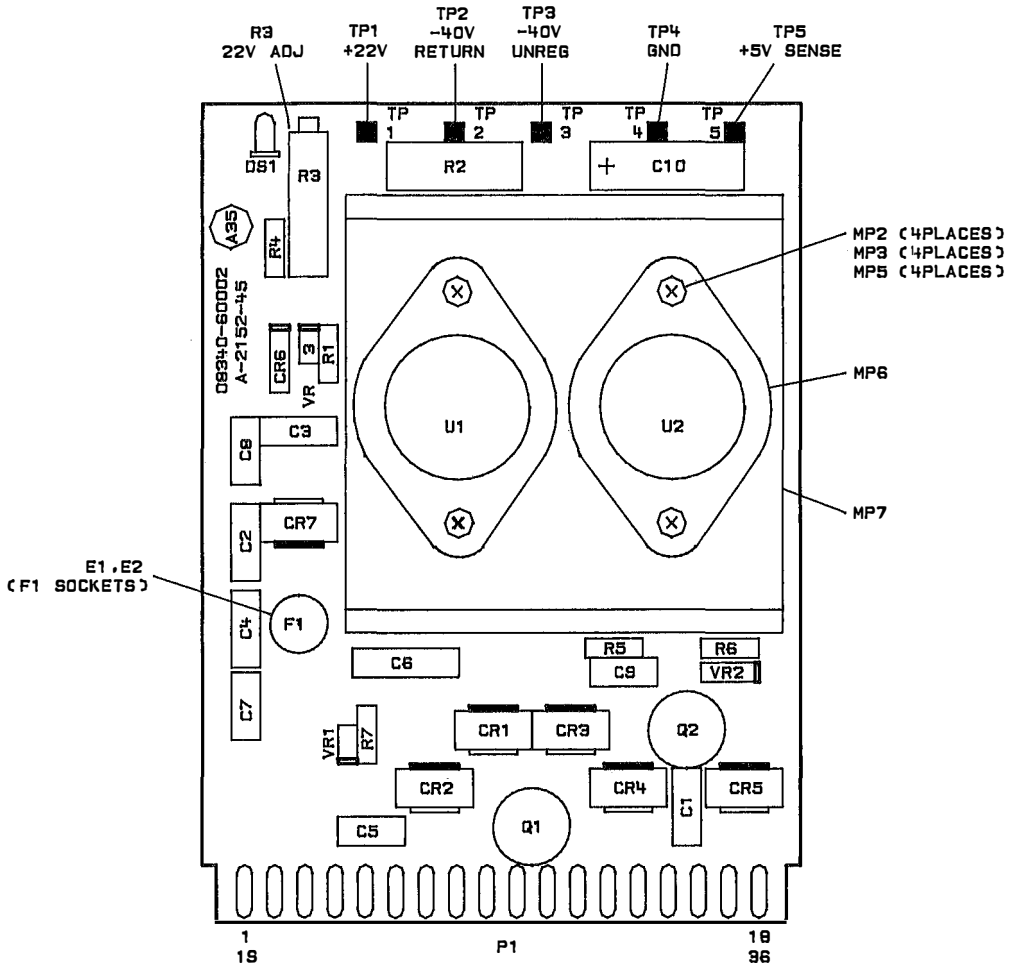


Figure 8J-7. A35 Rectifier, Component Location Diagram

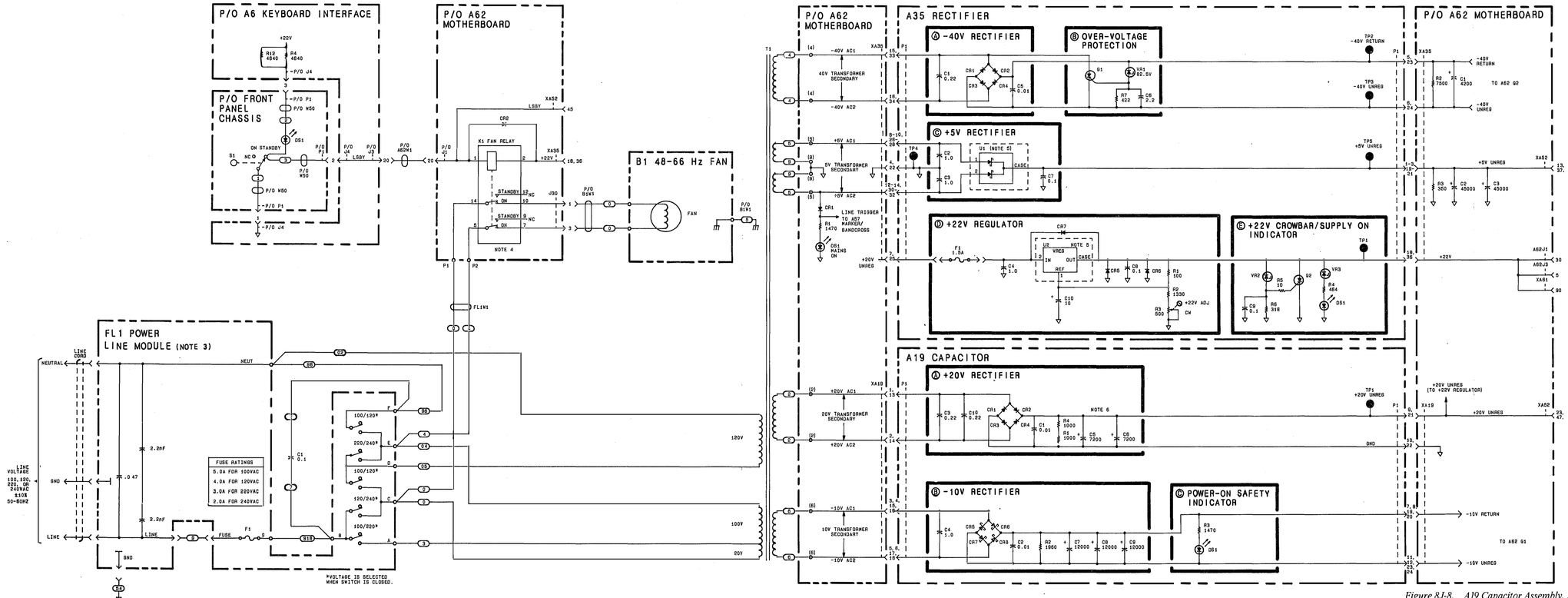
A35 Rectifier P1 Pin I/O

A35

Pin	Mnemonic	Levels	Source	Destination
1 19	+5V UNREG +5V UNREG	+7 TO +9V +7 TO +9V	C C	* *
2 20	+5V UNREG +5V UNREG	+7 TO +9V +7 TO +9V	C C	* *
3 21	+5V UNREG +5V UNREG	+7 TO +9V +7 TO +9V	C C	* *
4 22	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*C *C
5 23				
6 24	−40V UNREG −40V UNREG	−40V −40V	A B A B	* *
7 25	+20V UNREG +20V UNREG	+31.2V +31.2V	D D	* *
8 26	+5V AC1 +5V AC1	7V AC 7V AC	A62 LUG (5) A62 LUG (5)	*C *C
9 27	+5V AC1 +5V AC1	7V AC 7V AC	A62 LUG (5) A62 LUG (5)	*C *C
10 28	+5V AC1 +5V AC1	7V AC 7V AC	A62 LUG (5) A62 LUG (5)	*C *C
11 29				
12 30	+5V AC2 +5V AC2	7V AC 7V AC	A62 LUG (5) A62 LUG (5)	*C *C
13 31	+5V AC2 +5V AC2	7V AC 7V AC	A62 LUG (5) A62 LUG (5)	*C *C
14 32	+5V AC2 +5V AC2	7V AC 7V AC	A62 LUG (5) A62 LUG (5)	*C *C
15 33	−40V AC1 −40V AC1	−40V AC −40V AC	A62 LUG (4) A62 LUG (4)	*A *A
16 34	−40V AC2 −40V AC2	−40V AC −40V AC	A62 LUG (4) A62 LUG (4)	*A *A
17 35				
18 36	+22V +22V	22V 22V	D E D E	* *

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.



NOTES:

1. REFER TO THE SERVICE SECTION INTRODUCTION FOR DETAILED SCHEMATIC DIAGRAM NOTES.
2. RESISTANCE VALUES SHOWN ARE IN OHMS. CAPACITANCE IN MICROFARADS. AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. LINE MODULE PIN OUT DIAGRAM AS SEEN FROM ASSEMBLY CONNECTION SIDE:

4. BOTTOM VIEW OF A62K1:

5. BOTTOM VIEW OF A35U1, U2:

6. CAPACITORS A19C5-8 ARE LARGE ELECTROLYTICS MOUNTED TO THE A19 ASSEMBLY BY SCREWS.
7. C4 IS MOUNTED TO THE REAR PANEL ASSEMBLY IN OPTION 003 (400HZ LINE) INSTRUMENTS ONLY.

Figure 8J-8. A19 Capacitor Assembly, A35 Rectifier Assembly, Schematic Diagram

A52 POSITIVE REGULATOR

INTRODUCTION

This service section pertains to the following assemblies:

- The A52 Assembly.
- Parts of the A62 Motherboard Assembly.

A52 POSITIVE REGULATOR CIRCUIT DESCRIPTION

Introduction

The A52 Positive Regulator contains circuitry for the +20V supply, the +12V supply, the +5.2V, voltage accuracy sensing circuitry for these supplies, and ON/STANDBY and SHUTDOWN functions. The +20V supply is a self-starting regulator having a precision reference to accurately set the output potential. With the exception of the independent +22V standby supply (described in the A35 theory of operation), all supplies are slaved to the +20V output. The +12V, +5.2V, -10V and -40V supplies are directly slaved while the -5.2V and -15V supplies are indirectly slaved (refer to Figure 8J-2, Simplified Block Diagram).

NOTE

The +20V and +5.2V supplies are critical, low noise supplies with a specified periodic and random deviation (PARD) less than 100 microvolts peak. The +12V supply is non-critical with a specified PARD less than 5mV peak.

All components referenced below are on the A52 Assembly unless otherwise noted.

+10V/+4.9V REFERENCE Circuit A

The zener regulator VR5 creates a stable +10V reference (+10VR) for use in the +20V REGULATOR (Block **B**), Standby/Overtemperature Shutdown (Block **E**), and voltage sense circuitry on the A52 Positive Regulator Assembly. VR5 bias is supplied through R26 by +20V UNREG. The accuracy and stability of VR5 is not critical; however, a large error in the voltage across VR5 can cause problems with the power Up/Down circuitry. If +10VR is incorrect, check for excessive supply loading. Trouble is indicated if the value of +10V REF changes significantly as the LINE switch is cycled. The +4.9V reference (+4.9VR) is generated by divider network R39 and R40. This signal is used as a reference for the

comparators in the STANDBY/OVERTEMP SHUTDOWN (Block **E**) and VOLTAGE SENSE (Block **L**) circuits on the A52 Positive Regulator Assembly.

+20V REGULATOR Circuit B

The +20V REGULATOR is the master regulator for the 8340A power supply system. Except for the +22V standby supply (which is ON continuously), all instrument supplies are dependent on the +20V supply. The +12V supply and the REFERENCE OSCILLATOR SUPPLY are powered directly from the +20V regulator. The +5.2V, -10V, and the -40V supplies use the +20V supply as a reference (see Figure 8J-2). The -5.2V and -15V supplies are powered by the -10V and -40V supplies respectively, and are functionally dependent on the +20V supply.

The +20V startup current source is composed of Q12, Q13, and Q14. Q12 and R14, driven from the Internal +10V REFERENCE (Block **A**) form a 6mA (nominal) current sink. C19 damps out Q12 oscillations due to excessive line length. Q13 and Q14 are connected as a Wilson current mirror with local feedback (R6 and R7) to ensure current sharing. Output current from the collector of Q14 is 6mA.

In standby, the output of U4D pin 13 (Standby/Overtemp Shutdown) is LOW, and current from Q14 is shorted to ground. When the instrument is ON, both U4D pin 13 and U4C pin 14 are open (they have open collector outputs) and current from Q14 is delivered to the base of the darlington pass transistor A62Q3, acting as an emitter follower. This causes the +20V output to begin increasing.

When +20V output exceeds +10V, precision +10.00V reference U2 goes into regulation, and U1 begins to function. TP3, aside from allowing a check of U2, provides a very accurate +10.00V reference for instrument troubleshooting.

The DC feedback loop (error correction circuit) receives the +20V output through voltage divider R13 and R15 and compares it to the output of U2 by U1. The voltage generated on the output of U1 (pin 6) is fed through CR5 and R11 to the base of emitter follower pass transistor A62Q3, completing the loop. Due to the placement of CR5, U1 cannot source current to A62Q3. U1 therefore, sinks base current as +20V out exceeds 20 Volts, acting as negative feedback to regulate the output voltage.

R16 and C5 form a noise filter to clean up broadband noise on integrated reference voltage source U2. They also slow down the startup transient, acting as a "soft-start" circuit. C4 (in conjunction with R13), C3, R12 and C2, R10 and C1, R18 and C6, are loop frequency compensation components.

R1 and R2 form the current sense resistor for the foldback current limit circuit consisting of R82, R8, CR4, R9, and Q8. As the current from A62Q3 (Darlington pass transistors) exceeds 2.4 Amps, the voltage at the emitter of Q8 decreases sufficiently to turn Q8 on. This allows current to flow through Q8, sinking base current from A62Q3, and reducing the current from A62Q3. R8, R9, and CR4 sets the voltage at which Q8 turns on. CR10 protects instrument loads from reverse polarity power in the event of a short between the +20V output and some negative polarity power supply. R82 prevents Q8 from sinking all of the base current when the instrument (+20V supply) is turned on.

Foldback current limit is used on all critical supplies for several reasons. First, a high current supply (such as the +5.2V supply capable of delivering 10 Amps) is easily capable of damaging a printed circuit board if a short develops. Foldback current limit reduces this output current capability of the supply as its output voltage drops (as in driving a dead short). A second and equally important consideration is power dissipation in the pass transistor for a critical supply. The purpose of the foldback circuit is to have power dissipation less with the supply shorted, than with the supply in normal operation. Table 8J-2 lists the maximum output current capability of each supply, and short circuit output current in foldback.

Table 8J-2. Power Supply Output Current Capability

SUPPLY	MAXIMUM OUT	SHORT CIRCUIT CURRENT
+20	2.4A	< .5 A
+12	1.8A	NO FOLDBacK (>2A)
+5	10 A	< 3 A
-5	1.8A	NO FOLDBacK (>2A)
-10	6.0A	< 3 A
-15	1.8A	NO FOLDBacK (>2A)
-40	1.7A	< .5 A

+20V CROWBAR/SUPPLY ON INDICATOR Circuit C

VR1 and R20 monitor the +20V regulator output. When this voltage exceeds approximately 23V, the drop across R20 is large enough to bias crowbar SCR Q1 ON and short the supply output to ground. This circuit is useful for protecting instrument loads in many fault conditions. C21 prevents very short transients from firing SCR Q1.

Yellow LED DS2, mounted close to TP4, and current limit resistor R21 give a visual indication of the status of the +20V power supply. By observing this indicator along with the indicators for the other supplies, the status of all the instrument power supplies can be easily determined.

+20V Supply Tolerance

The tolerance of the +20V supply is +20V ±5% (1.0V).

REFERENCE OSCILLATOR SUPPLY Circuit D

When HIGH INTERNAL 10 MHz STANDARD ENABLE (HSTD) is set HIGH by the microprocessor, Q4 conducts, turning series switch Q5 ON. This brings the +20V Reference Oscillator Supply output up to power the A51 10 MHz Reference Oscillator.

STANDBY/OVERTEMP SHUTDOWN Circuit E

In STANDBY mode LSBY is pulled LOW by the front panel ON/STANDBY switch. This drives U4D pin 13 (the open collector output of quad comparator U4, Standby/Overtemp Shutdown Block **E**) LOW which in turn, through CR7, pulls the base of chassis mounted +20V pass transistor Q3 to ground. The +20V supply is shut down, along with all other supplies that are slaved to it. Also, CR13 pulls the CLK input to D-type flip flop U5B LOW (U5 is a positive edge triggered CMOS D-type flip flop).

When the ON/STANDBY switch is flipped to the ON position, LSBY rises to +22V, reverse biasing CR6. The voltage across C9 rises exponentially toward 5V. When it passes 4.9V, U4D pin 13 goes HIGH (open) and the base of chassis mounted Q3 is released. The +20V supply starts itself. CR13 now causes the CLK input to U5B to go HIGH (but not to exceed the 10V Vcc). This transition clocks a zero into the flip flop (due to the D input, which is tied low), resetting any overtemperature condition that may have occured. During initial power-up, C10 and R53 reset U5B to ensure that the instrument is always in operational status (with overtemp flag cleared) when initially energized.

The main heat sink temperature sensor is a normally open bi-metallic switch that closes when the heat sink reaches 100 degrees C. The sensor is tied from LOW HEAT SINK OVERTEMPERATURE SENSOR (LHSOT) to ground. A switch closure pulls LHSOT LOW and forces U4A pin 1 HIGH, which in turn sets flip flop U5B Q output (pin 13) HIGH. This forces U4B output (pin 2) HIGH and turns ON red overtemp indicator LED DS4. U5B Q NOT output (pin 12) goes LOW forcing U4C pin 14 LOW which in turn pulls the base of A62Q3 to ground, shutting all instrument power supplies down except the

+22V supply. U5B has now latched this overtemp condition, and subsequent removal of LHSOT (as when the heat sink cools back down) does not cause the instrument to restart. The only way to clear this overtemp condition is to turn the ON/STANDBY switch to STANDBY, and then back to ON.

This overtemp protocol was specifically chosen for several reasons. First of all, a fault condition that allows the main heat sink to reach 100 degrees C indicates that a failure has probably occurred (e.g. the fan has stopped, etc.). To ensure that the operator is aware of a potentially hazardous condition it takes specific operator intervention before the instrument will restart. Because the over temperature detector latches when overtemp is detected, the 8340A will not cycle ON and OFF repetedly if there is a condition that causes overheating. This improves instrument reliability by eliminating cycling at excessively high temperatures.

GROUNDS and COMMONS F

Ground distribution is very critical on this board to achieve the PARD (Periodic and Random Deviation) specification for the +20V and +5.2V regulators. Right at the edge connector fingers power ground (plain ground), sense ground (ground 1), and +20V ground (ground 2) are separated. This is to isolate power ground currents from sensitive circuitry in the regulators. The sense ground for the +5.2V supply (ground 3) is taken from +5.2V sense (-), P1-39.

+5.2V REGULATOR Circuit G

+20V provides the reference voltage, and powers the loop error correction amplifier U3. R67 and R68 drop +20 Volts to 4.0 Volts. C14 is a noise filter, and also acts as a "soft-start" element (it slows down the power supply turn-on transient). +5.2V out is sensed remotely on the A62 Motherboard at the main 5V power distribution point. +5.2V SENSE(+) comes back onto the board, into voltage divider R65, R66, and is compared to the generated 4V reference by error amp U3. The output voltage of U3 is fed to emitter follower Q7, then to darlington driver Q10, and then to the transistor, A62Q4. The +5.2V SENSE(-) comes from the central ground distribution point (STAR ground) on the A62 Motherboard to provide ground reference (ground 3).

Loop frequency compensation is provided by C13 (in parallel with R65) C16, R63, R64 and C12. R69 and C15 lower output impedance and provide a minimum load capacitance. Foldback current limit operates in essentially the same manner as in the +20V supply. The current sense resistor is the parallel combination of R3, R4, and R5. Foldback is accomplished with pre-bias from R61 and R62,

and Q6 is the active element. R83 prevents Q6 from sinking all of the base current to Q7 when the +5.2V supply is active.

+5.2V CROWBAR/PROTECTION Circuit H

When +5.2V OUT exceeds approximately 6.2V, VR3 conducts, biasing crowbar SCR Q11 on and shorting the +5.2V output to ground. This protects load circuits from an overvoltage condition. C20 prevents very short transients from firing SCR Q11. CR12 protects against reverse polarity applied to the load due to some instrument fault, and yellow LED, DS1, provides a visual indication of the operational status of the +5.2V supply.

+5.2V Supply Tolerance

The tolerance of the +5.2V supply is +5.2V +-5% (0.26V).

MICROPROCESSOR PROTECTION Circuit I

VR4 senses the -5.2V supply. If the -5.2V supply level is more positive than -4.5V, Q3 is turned ON. This shorts the adjustment terminal of A62U1 (the +12V regulator in +12V REGULATOR Block **E**) to ground, pulling +12V output down to +1.3V. This circuit prevents the 08340-60018 version microprocessor from being damaged by excessive power dissipation. If repairs have been done to either the +12V or -5V supplies, it is critical that the operation of this circuit be checked prior to turning the instrument ON with a 08340-60018 microprocessor board installed.

+12V REGULATOR Circuit J

A62U1 is an adjustable three-terminal regulator. Output voltage is adjusted by the selection of the feedback resistors R29, R30 and A62R14. R30 and A62R14 are fixed values while R29 is a factory select. Through proper selection of R29, compensation for variations in regulator characteristics is obtained. The nominal value of R29 is 3.83K and is appropriate for most of the regulators. However, it may be necessary to substitute an alternate value. Increasing R29 increases the +12V output. A62R14 is mounted on the A62 Motherboard in parallel to R29 to ensure that the regulator has a ground reference path before its feedback is connected (as in accidentally inserting the A52 Positive Regulator Assembly with the power ON).

Input capacitor A62C7 is required for stability of the regulator. A62C6 is a noise filter and increases the ripple rejection of the regulator and lowers its output impedance. A62CR3 is required to protect the regulator from damage due to charge stored on A62C6 in the event of a short from the +12V output to ground. CR11

protects the +12V power supply's loads from reverse polarity power in the event of a short between +12V and some negatine power supply. R31 and C17 reduce the output impedance of the supply, and provide a minimum capacitive load to guarantee stability regardless of load configuration.

+12V CROWBAR/POWER ON INDICATOR Circuit K

When +12V OUT exceeds approximately 13.5 Volts, VR2 conducts, providing gate current for crowbar SCR Q2, biasing it on and shorting the supply output to ground. This protects load circuits from damage due to the overvoltage condition. C22 prevents very short transients from firing SCR Q2. Yellow LED, DS3 gives a visual indication of the status of the +12V power supply. It will begin to light when the output of A62U1 is approximately +7.6V.

+12V Supply Tolerance

The tolerance of the +12V supply is +12V $\pm$5% (0.6V).

VOLTAGE SENSE Circuit L

U6A, U6D, and U6B sense the level of the +5.2V, +12V and +20V power supplies. When one of these supplies goes out of regulation its comparator output goes LOW, shorting delay capacitor C8 to ground. This forces HPUP (HIGH POWER UP) LOW, pulling LIPS (LOW INSTRUMENT PRESET) LOW. CR9, CR14 and CR15 are provided to easily isolate which supply caused the low voltage indication.

The cathode of CR8, HIGH NEGATIVE UP (HNUP) is connected to the A53 Negative Regulator and the A56 -15V Supply boards. This line is pulled LOW in the event any of these supplies go out of regulation.

When all supplies come into regulation, C8 is released and its voltage increases as it is charged by R49. After some 300mS its level passes VREF at 4.9 volts and U6C pin 14 goes LOW. This sets HPUP (via Q16) and LIPS (via Q15) HIGH. These signals are used by the processor (and several other circuits) to control instrument activity and to ensure proper initialization.

A52 POSITIVE REGULATOR, TROUBLESHOOTING

WARNING

When connected to ac mains, there are voltages at points inside the instrument that can cause personal injury or even death. Any servicing of this instrument with protective covers removed should be performed only by trained personnel who are aware of the hazard involved.

CAUTION

Do not remove the crowbar and operate the supply without it. This could cause severe damage to the instrument if the supply is faulty and the crowbar has engaged to protect the instrument.

WARNING

If the A19 POWER-ON SAFETY INDICATOR LED is on there are voltages present inside the instrument (the A62 Motherboard, the A35 and A19 Rectifier Assemblies, line filter module/transformer wiring, etc.) that can cause personal injury or even death.

CAUTION

The A52 Assembly contains static sensitive components. Troubleshoot this assembly only at a work station that is equipped with an anti-static surface. Any persons working on this instrument should wear a grounding strap that provides a path to ground of no less than 1 Megohms and no more than 2.5 Megohms. All anti-static safeguards must conform to state and federal safety standards and statutes. When handling a printed circuit board always hold it by the edges. Never touch the finger contacts.

+20V REGULATOR Troubleshooting

If all supplies appear to be down, the first priority is to troubleshoot the +20V Regulator (Block B). If this supply is down

the rest of the instrument supplies, except the +22V supply, will be shut down.

If more than one supply has failed, and the +20V supply is not one of them, refer to the **"POWER SUPPLY TO ASSEMBLY LEVEL"** Flow Chart.

The +20V supply tolerance is +20V ±5% (1.0V).

SUPPLY/LOAD FAILURE DETERMINATION

Disconnect the instrument from ac mains. After the POWER-ON SAFETY INDICATOR goes out remove the A52 Assembly and place it on an extender board. Apply thin, colored, non-conductive tape to the extender board +20V output pins (use of a colored tape is recommended because transparent tape may be forgotten and left on the extender board, causing unnecessary troubleshooting). Do not apply tape to A52 printed circuit board edge fingers. Re-install the A52 Assembly and connect ac mains to the instrument. If the power supply now operates properly suspect a short on one of the instrument assemblies that use +20V. After removing tape from extender board fingers clean fingers according to the following instructions:

CAUTION

Cleaning P.C. Board fingers by any other method than the one described below may cause serious reliability problems. NEVER clean fingers with any kind of eraser. NEVER use tap water in the cleaning solution described below. Tap water contains chlorine. Chloride contamination from tap water, salt (from skin contact), or any other source may cause serious reliability problems. Always wear a ground strap when handling any internal 8340 component or assembly. Always hold printed circuit boards by the edges.

Printed Circuit Board Finger Cleaning Procedure

Mix one part deionized water with two parts isopropyl alcohol. Apply this solution to a clean, lint free, cloth (HP Part Number 9310-0039 CD3). Rub the fingers carefully and then dry with a clean part of the cloth.

- +20V Load Failure
- +20V Power Supply Failure

+20V Load Failure

If the problem is load related repeat the above procedure for safe removal of the A52 Assembly, remove the tape from the extender board's +20V output pins, clean the extender boards fingers as described above, and re-install the A52 Assembly. It will be necessary to remove each assembly that uses +20V, one at a time, to determine which one is faulty. Likewise remove any cables listed that carry the affected supply. Refer to Table 8J-11, Power Supply Destination Chart at the end of the **"POWER SUPPLY - FAN"** functional group, for a list of these assemblies. Always remove ac mains and wait for the POWER-ON SAFETY INDICATOR to go out before removing or installing any assembly or cable.

+20V Power Supply Failure

If the power supply output does not return to normal after the extender board +20V output pins are taped off, refer to the appropriate section below:

- +20V output voltage approximately .8V to 1.0V.
- +20V output voltage approximately 0V.
- +20V output voltage incorrect. Tolerance is +20V ±5% (1.0V).

+20V output voltage approximately .8V to 1.0V.

Crowbar circuit verification - If the output voltage is approximately .8V to 1.0V the crowbar circuit is engaged. Connect the instrument to an auto-transformer set for 0V output. While monitoring the supply output voltage slowly increase the auto-transformer output voltage. If the crowbar fires before the supply output reaches +20V suspect VR1.

Regulator and error amp verification - If the power supply output reaches +20V stop increasing auto-transformer voltage. Verify a 6 mA current flow through Q14 (measure .6V across R7). If the voltage across R7 is wrong check for 6 mA through Q13 (.6V across R6). Check the current through Q12, it should also be 6ma. Check for +10V at the base of Q12. If Q12, Q13, and Q14 are operating correctly check the operation of precision +10V reference device U2 and operational amplifier U1.

Check the voltage across CR7 (Block E). If the voltage is .6V the base current of A62Q3 is being drawn away by U4D.

Check U4D (Block E) input pins. Pin 11 should be approximately +20V and pin 10 should be +4.9V. If these are correct suspect a U4 failure. It is possible that a failure of U4C (Block E) is drawing A62Q3 base current. However this can only be verified by changing U4.

Measure the voltage across the base (P1-7) and the emitter (P1-8) of darlington transistor A62Q3. If the voltage is not approximately 1.25V suspect A62Q3. Measure the voltage between the collector and the emitter of A62Q3. If there is little or no voltage A62Q3 is probably shorted.

+20V output voltage approximately 0V.

Initial checks - Ensure that ac mains voltage is nominal and that the line voltage selector printed circuit board is installed properly in the line filter module, FL1. Make sure the proper fuse value is installed. If the above is correct and the power supply input fuse (F1) is blown, suspect darlington transistor A62Q3.

Measure the +20V UNREG (P1-23) with respect to ground. If this voltage is less than approximately +30V, troubleshoot the +20V Rectifier. Refer to the A19 troubleshooting guide.

Regulator verification - Measure across the base (P1-7) and emitter (P1-32) of A62Q3. If the voltage is not approximately 1.25V suspect A62Q3.

Current limit checks - Check for .6V across the emitter - base junction of Q8. This condition indicates that the current foldback circuit is engaged and that it is shutting down the pass transistor A62Q3.

Measure Q8 emitter to collector. If the voltage is approximately .2V or less, Q8 may be shorted.

Examine the +20V supply for burnt or discolored components.

Suspect a shorted capacitor, diode, or crowbar SCR if the above mentioned procedures to not isolate the problem.

+20V output voltage incorrect. Tolerance is +20V $\pm$5% (1.0V).

Ensure that ac mains voltage is nominal and that the line voltage selector printed circuit board is installed with the proper line voltage selected. Measure the +20V UNREG input

with respect to ground. If the voltage is less than Approximately +30V troubleshoot the +20V Rectifier. Refer to the A19 Troubleshooting Guide.

Measure the output voltage with an HP 1740A or similar Oscilloscope to make sure the supply is not oscillating. If the supply is oscillating check the precision 10V reference for oscillations. Check loop frequency compensation capacitors C1, C2, C4, and C5.

Check the voltage output of the precision reference U2 and the values of divider resistors R13 and R15. Make sure the feedback path to U1 is not open.

Check C4 and C5 by removing them from the circuit. C4 and C5 are likely to cause supply noise or temperature instability if bad (current leakage). The voltage at pin 2 of U1 must be 1/2 of the supply output voltage.

+12V REGULATOR Troubleshooting

The +12V supply tolerance is +12V ±5% (0.6V). If the +12V regulator is down, remember that this supply comes up only when the +5.2V and -5.2V supplies are both operating properly. If the A53 Negative Regulator board is not installed, the +12V supply will not function. The best way to tell which circuit caused the shutdown is to measure the base of Q3 in the MICROPROCESSOR PROTECTION circuit (Block I). If it is turned ON (.6V or greater), then VR4 is open or the -5.2V supply is down. If it is OFF, then U6B pin 1 in Voltage Sense (Block L) has caused the problem. Trace backwards to find out why.

Determine if the +12V supply has failed or is being forced into current limit by a short elsewhere in the instrument. Refer to "SUPPLY/LOAD FAILURE DETERMINATION" in the above +20V troubleshooting section. If the problem is load related, troubleshooting is similar to the +20V "Load Failure" section. If the +12V supply is at fault, proceed as follows:

+12V Power Supply Failure

If the power supply output does not return to normal after the extender board +12V output pins are taped off, refer to the appropriate section below:

NOTE

After repairing the +12V supply make sure its output is +12.00V ±.6V. Change factory select resistor R29 if necessary. Increasing R29 Increases the +12V output.

- +12V output voltage approximately .8V to 1.0V.
- +12V output voltage approximately 0V.
- +12V output voltage incorrect. Tolerance is +12V ±5% (0.6V).

+12V output voltage approximately .8V to 1.0V.

Crowbar circuit verification - If the output voltage is approximately .8V to 1.0V the crowbar circuit is engaged. Connect the instrument to a auto-transformer set for 0V output. While monitoring the supply output voltage slowly increase the auto-transformer output voltage. If the crowbar fires before the supply output reaches +12V suspect VR2.

Regulator verification - If the power supply output reaches +12V stop increasing auto-transformer voltage. Measure the voltage across pin 1 and the case of A62U1 (regulator). If the voltage is not approximately 1.25V suspect A62U1. Measure the voltage from the input and the output of A62U1. If there is little or no voltage A62U1 is probably shorted.

+12V output voltage approximately 0V.

Initial checks - Ensure that ac mains voltage is nominal and that the line voltage selector printed circuit board is installed properly in the line filter module, FL1. Make sure the proper fuse value is installed.

If the above is correct and the power supply input fuse (F2) is blown, suspect regulator A62U1.

Measure the +20V REGULATOR output (TP4). If this voltage is incorrect, troubleshoot the +20V power supply. Refer to the **"+20V REGULATOR Troubleshooting"** section, above.

Regulator verification - Measure across pin 1 and the case of A62U1. If the voltage is not approximately 1.25V suspect A62U1.

Examine the +12V supply for burnt or discolored components. Suspect a shorted capacitor, diode, or crowbar SCR if the above mentioned procedures to not isolate the problem.

+12V output voltage incorrect. Tolerance is +12V ±5% (0.6V).

Ensure that ac mains voltage is nominal and that the line voltage selector printed circuit board is installed with the

proper line voltage selected.

Measure the +20V REGULATOR output (TP4). If the voltage is incorrect, troubleshoot the +20V power supply. Refer to the **"+20V REGULATOR Troubleshooting"** section, above.

Measure the +12V output voltage with an HP 1740A or similar Oscilloscope to make sure the supply is not oscillating.

If the output is approximately 1.25V either A62C6 or A62C7 are probably shorted.

CAUTION

After repairing the +12V supply the operation of the MICROPROCESSOR PROTECTION Circuit must be checked prior to turning the instrument on with the A60 Microprocessor board in the instrument.

REFERENCE OSCILLATOR SUPPLY Troubleshooting

If the +20V switched supply does not come up (or will not shut down), check driver Q4 and pass element Q5 in Reference Oscillator Supply (Block D).

Ensure that the INTERNAL 10 MHz STANDARD ENABLE (HSTD) signal is getting to the board properly.

+5.2V REGULATOR Troubleshooting

The +5.2V supply tolerance is +5.2V ±5% (0.26V). The +5.2V supply and the +20V supply are similar in design. Therefore, troubleshooting techniques are similar. Refer to the +20V "SUPPLY/LOAD FAILURE DETERMINATION" section, above, to determine if the failure is caused by a supply failure or a shorted assembly elsewhere in the 8340A. Refer to the +20V "Load Failure" section if the cause is load related. If the supply has failed, proceed as follows:

+5.2V Power Supply Failure

If the power supply output does not return to normal after the extender board +5.2V output pins are taped off, refer to the appropriate sections below:

- +5.2V output voltage approximately .8V to 1.0V.

- +5.2V output voltage approximately 0V.

- +5.2V output voltage incorrect. Tolerance is +5.2V ±5% (0.26V).

+5.2V output voltage approximately .8V to 1.0V.

Crowbar circuit verification - If the output voltage is approximately .8V to 1.0V the crowbar circuit is engaged. Connect the instrument to an auto-transformer set for 0V output. While monitoring the supply output voltage slowly increase the auto-transformer output voltage. If the crowbar fires before the supply output reaches +5.2V suspect VR3.

Regulator and error amp verification - If the power supply output reaches +5.2V stop increasing auto-transformer voltage. Check the operation of transistors Q7, Q10, and A62Q4. The emitter-base voltage across each of these transistors should be approximately .6v. Check for emitter-collector shorts. Measure the voltage across the collector and emitter of A62Q4. If there is little or no voltage A62Q4 is probably shorted.

+5.2V output voltage approximately 0V.

Initial checks - Ensure that ac mains voltage is nominal and that the line voltage selector printed circuit board is installed properly in the line filter module, FL1. Make sure the proper fuse value is installed. If the above is correct and the power supply input fuse (F3) is blown, suspect transistor A62Q4.

Measure the +5V UNREG (P1-13). If this voltage is less than approximately +9.5V, troubleshoot the +5V Rectifier. Refer to the A35 troubleshooting guide.

Regulator verification - Check transistors Q7, Q10, and A62Q4 for proper operation. The base-emitter voltage across each of these transistors should be approximately .6V.

Current limit checks - Check for .6V across the emitter-base junction of Q6. This condition indicates that the current foldback circuit is engaged and that it is shutting down the pass transistor A62Q4. Measure Q6 emitter to collector. If the voltage is approximately .2V or less, Q6 may be shorted.

Examine the +5.2V supply for burnt or discolored components. Suspect a shorted capacitor, diode, or crowbar SCR if the above mentioned procedures to not isolate the problem.

+5.2V output voltage incorrect. Tolerance is +5.2V ±5% (0.26V).

Ensure that ac mains voltage is nominal and that the line voltage selector printed circuit board is installed with the proper line voltage selected.

Measure the +5V UNREG. If the voltage is less than Approximately +9.5V troubleshoot the +5V Rectifier. Refer to the A35 Troubleshooting Guide.

Measure the output voltage with an HP 1740A or similar Oscilloscope to make sure the supply is not oscillating. Check frequency compensation capacitors C12, C13, and C16.

Check the values of divider resistors R66 and R67.

Make sure the feedback path to U3 is not open. Check C13 and C14 by removing them from the circuit.

C13 and C14 are likely to cause supply noise or temperature instability if bad (current leakage).

A52 REPAIR PROCEDURE

CAUTION

The thermal connection between the voltage regulator A35U2 and the main heat sink is the dominant factor in its long term reliability. Be sure to properly apply thermal compound (HP Part Number 6040-0454 CD0) when installing or replacing this part.

CAUTION

Use only oil based thermal compound. The use of silicone based thermal compound may cause reliability problems. Silicone based oil migrates to pass element sockets, switch contacts, or printed circuit board finger contacts. The compound then tends to raise contact resistance or electrically isolate the contacts. Silicone based thermal compounds disperse into the air and deposit themselves anywhere in the instrument. Applying this material to a warm component (e.g. a heat sink or series pass element) increases the rate of dispersion.

Thermal Compound Application

When installing or replacing a pass transistor or voltage regulator make sure thermal compound is applied as described below:

Apply a thin coating of thermal compound (HP Part Number 6040-0454 CD0) to both sides of the insulating washer. The coating should be just thick enough to provide a thin but continuous layer of compound from component-to-washer and washer-to-heat sink. An excessive amount of heat sink compound impairs its ability to transfer heat. The pass element mounting screws should be tightened with seven inch-pounds of force. Tightening with less force diminishes the heat transfer capability of the thermal compound. Tightening with greater force may damage the mounting hardware.

Table 8J-3. A52 Positive Regulator, Regulated Supply Limits

Power Supply	DMM Probe	Ground	Limits
+20V	A52TP4	A52P1-19	+19.00V to +21.00V
+12V	A52TP5	A52P1-19	+11.4V to +12.6V
+5.2V	A52P1-17	A52P1-19	+4.94V to +5.46V

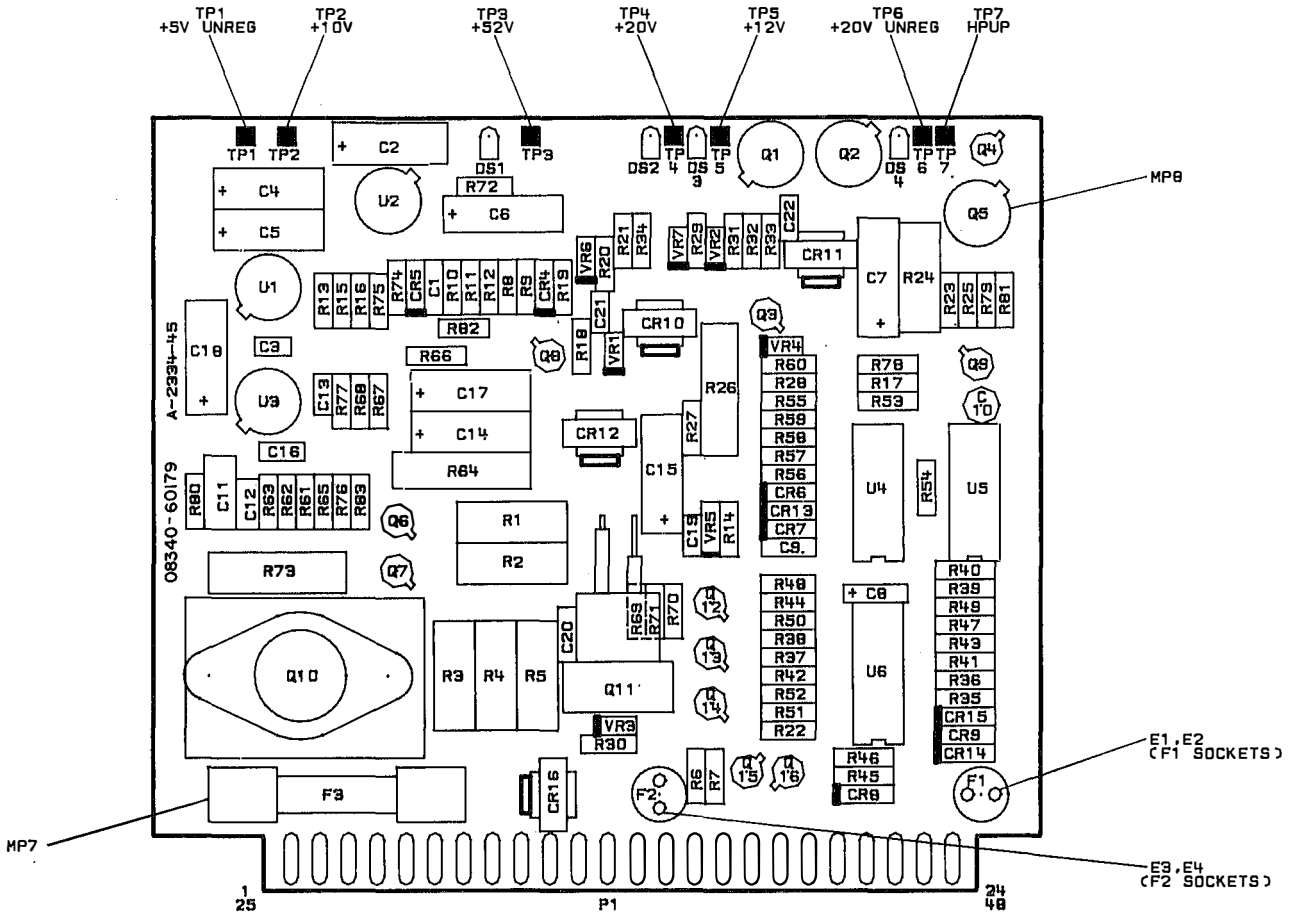


Figure 8J-9. A52 Positive Regulator, Component Location Diagram

A52 Positive Regulator P1 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 25	Q4C Q4C		A62Q4-COLLECTOR A62Q4-COLLECTOR	G G
2 26	Q4C Q4C		A62Q4-COLLECTOR A62Q4-COLLECTDR	G G
3 27	Q4B Q4B		A62Q4-BASE A62Q4-BASE	G G
4 28	Q4E Q4E		A62Q4-EMITTER A62Q4-EMITTER	G G
5 29	Q4E Q4E		A62Q4-EMITTER A62Q4-EMITTER	G G
6 30	Q3C Q3C		A62Q3-COLLECTOR A62Q3-COLLECTOR	A B E A B E
7 31	Q3B		A62Q3-BASE	B B
8 32	Q3E Q3E		A62Q3-EMITTER A62Q3-EMITTER	B B
9 33	+12V +12V	+12V +12V	J K J K	*L *L
10 34	+12V UI ADJ	+10.5V	J	*I L
11 35	+12V UNREG +12V UNREG	+20V +20V	J J	*J *J
12 36	LHSOT LIPS	TTL (LOW TRUE) TTL (LOW TRUE)	A62J31-26 *L	E *
13 37	+5V UNREG +5V UNREG	+7 TO +9V +7 TO +9V	XA35P1-1-3, 19-21 XA35P1-1-3, 19-21	*G *G
14 38	+5V UNREG +5V UNREG	+7 TO +9V +7 TO +9V	XA35P1-1-3, 19-21 XA35P1-1-3, 19-21	*G *G
15 39	+5V SENSE (+) +5V SENSE (−)	+5.2V 0V	G F	L F
16 40	+20V +20V	+20V +20V	B C B C	*D J L *D J L
17 41	+5.2V +5.2V	+5.2V +5.2V	G H G H	* *
18 42	+5.2V +5.2V	+5.2V +5.2V	G H G H	* *
19 43	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
20 44	+20V REF OSC HNUP	0V/+20V TTL (HIGH TRUE)	D XA53P1-17; XA56P1-1, 16	A62J3-1 *L
21 45	HSTD LSBY	TTL (HIGH TRUE) 0V TO +22V	XA59P1-66 A62J1-20	D E
22 46	−5.2V HPUP	−5.2V TTL (HIGH TRUE)	XA53P1-18, 36 L	*I *
23 47	+20V UNREG +20V UNREG	+31.2V +31.2V	XA35P1-7, 25 XA35P1-7, 25	*A *A
24 48	+20V UNREG +20V UNREG	+31.2V +31.2V	XA35P1-7, 25 XA35P1-7, 25	*A *A

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

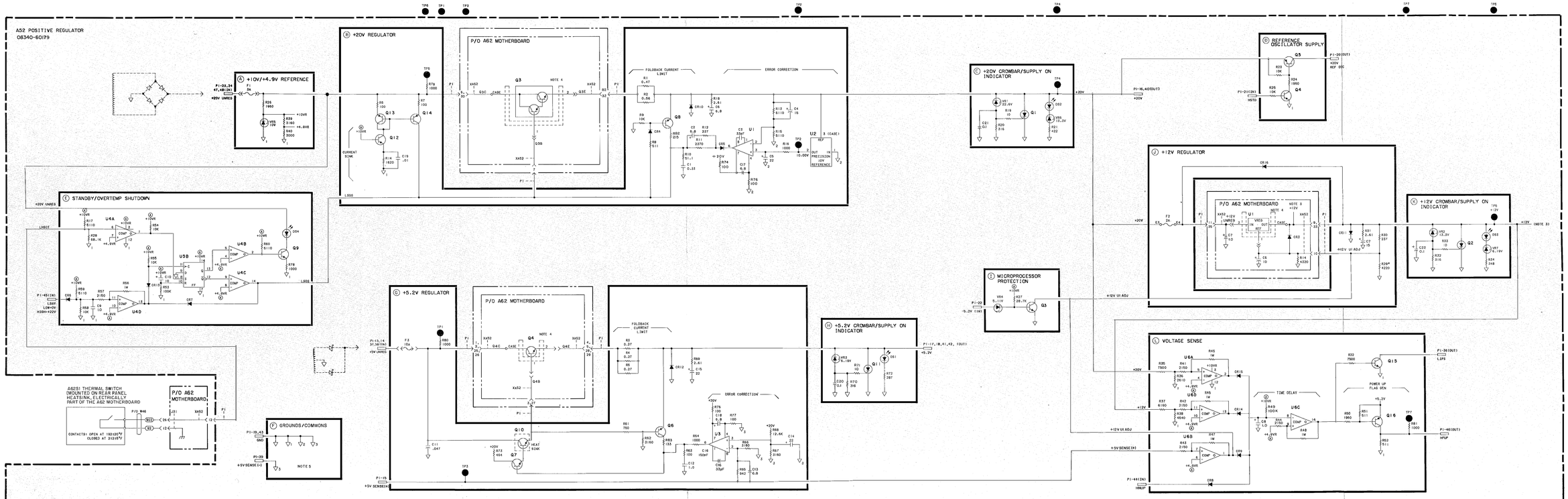


Figure 8J-10. A52 Positive Regulator, Schematic Diagram

A53 NEGATIVE REGULATOR/A56 -15V REGULATOR

INTRODUCTION

This service section pertains to the following assemblies:

- The A53 Negative Regulator Assembly.
- The A56 -15V Regulator Assembly.
- Parts of the A62 Motherboard Assembly.

A53 NEGATIVE REGULATOR, CIRCUIT DESCRIPTION

Introduction

The A53 assembly contains all circuitry for the -10V, -5.2V, and -40V power supplies, as well as voltage sensing circuitry to flag the A52 Positive Regulator board should one of these supplies go out of tolerance.

NOTE

The -10V and -40V supplies are critical, low-noise supplies. They are limited to a Periodic and Random Deviation (PARD) less than 100 microvolts peak. The -5.2V supply is primarily a digital (ECL) supply, and has a PARD specification of 5mV.

-10V REGULATOR Circuit A

+20 VREF (P1 pin 29) comes onto the board from the A52 Positive Regulator. It is used as a reference through voltage divider chain R8, R9, and R10, and it powers up error amp U4. C5 is the "soft-start" element (it slows down the -10V supply turn-on transient). CR6 protects the input stage of U5 during startup. The DC feedback loop is completed through R7, CR5, and darlington driver A62Q1. This power supply differs from many others in that the return side of the supply is regulated and the unregulated side is common to the output. A62Q1 regulates the voltage difference between the -10V RETURN and ground. The amplitude of the -10V RETURN is regulated as necessary so that the -10V UNREG line is always -10V with respect to ground. This allows the use of an NPN pass transistor used as an emitter follower rather than in the common emitter configuration, which is more sensitive to supply loading.

C1, C4, R6, and C3 are frequency compensation components. C6

provides a minimum load capacitance and lower output impedance. Foldback current limiting is used here as on the +5.2 and +20V supplies. The parallel combination of R1, R2, and R3 forms the current sense resistor.

The voltage at the base of Q4 is set by the voltage divider formed by R4 and R5. The voltage at the R4 end of the divider is set by the voltage drop across the current sense resistors (R1 - R3). The voltage at the R5 end of the divider is set by the output voltage of the supply. When the voltage at the base of Q4 reaches Vbe (threshold), Q4 will begin to conduct and will remove some portion of the base current being supplied to Q1 by U4. When the output voltage of the supply is low (during turn on or short circuit) a relatively small sense resistor (R1 - R3) current will bring Q4's base voltage above threshold. Q4 will turn on limiting the current supplied to Q1.

When the output of the supply is negative (-10V) the base of Q4 will be biased more negative and it will require a larger sense resistor current to bias the base of Q4 above threshold.

CR4 partially compensates for the base-emitter voltage of A62Q1. R55 provides sufficient current to bias CR4 in its linear region. CR7 in protects load circuits from reverse polarity power should a short develop between the -10V output and a high current positive supply.

-10V CROWBAR/SUPPLY ON INDICATOR Circuit B

Should -10V OUT exceed approximately 11V, VR1 will conduct, biasing crowbar SCR Q6 on and shorting the supply output to ground. This protects load circuits from an overvoltage condition. C15 prevents very fast transients from firing Q6. Yellow LED DS3 provides a visual indication of the -10V supply operational status.

-10V Supply Tolerance

The -10V supply tolerance is -10V $\pm$5% (0.5V).

-5.2V REGULATOR Circuit C

U1 is a monolithic three-terminal adjustable negative regulator. The adjustment terminal is nominally 1.25V above the output terminal.

C14 increases ripple rejection for U1. CR15 provides a discharge path for C14 when Vout is shorted to ground. C8 is required by the regulator for stability, and C7 is required to reduce the apparent electrical length of the supply input leads. R15 lowers

the power dissipation in U1 by reducing its operating junction temperature. CR8 is provided to protect load circuits from damage due to reverse polarity power caused by an instrument failure.

-5.2V CROWBAR/SUPPLY ON INDICATOR Circuit D

When -5.2V OUT exceeds approximately 6.2 volts, VR2 conducts, biasing crowbar SCR Q1 on and shorting the -5.2V supply to ground. Yellow LED DS1 provides a visual indication of the operational status of the supply.

-5.2V Supply Tolerance

The -5.2V supply tolerance is -5.2V +-5% (0.26V).

CAUTION

After repairing the -5V supply the operation of the MICROPROCESSOR PROTECTION Circuit (located on the A52 Positive Regulator Assembly) must be checked prior to turning the instrument on with a 08340-60018 Processor board in the instrument.

-40V REGULATOR Circuit E

This circuit is similar in operation to the -10V REGULATOR in that the -40V RETURN line is regulated, not the -40V UNREG line. See the **"-10V REGULATOR Circuit A"** description, above. +20V REF provides reference (through divider R27, R28, R29) for the regulator, and powers error amplifier U3. VR4 limits the negative supply to U3 at -10V. C12 is the "soft-start" element, slowing down the power supply turn-on transient. CR11 protects the input stage of U3 during startup. The forward path is completed through R26, CR10, darlington driver Q3, and pass transistor A62Q2. CR9 protects the base-collector junction of Q3 during startup. (When the supply is beginning to energize, A62Q2 has a low collector current and a beta (gain) of less than one. The collector-base junction of Q3 could be forward biased and become susceptible to failure from excessive current flow.) Current limit operation is similar to the -10V current limit. R22 is the current sense resistor, Q2 is the active element, and R23/R24 provide Q2 bias.

Feedback is completed off the board using remote sense at the main -40V distribution point on the A62 Motherboard. -40V SENSE comes back onto the board to complete the loop. Ground reference (Ground 2) connects to main ground on the board at the edge finger to reduce the perturbations in the supply due to noise currents in the ground trace on the board. R31 and C13 provide a

minimum load capacitance. CR12 protects load circuits from damage due to reverse polarity supply power caused by an instrument failure.

-40V CROWBAR/SUPPLY ON INDICATOR Circuit F

When -40V OUT exceeds appproximately 44.2 volts, VR3 conducts, biasing crowbar SCR Q5 on and shorting the -40V supply to ground. This protects load circuits from an overvoltage condition. C16 prevents very fast transients from firing Q5. Yellow LED DS2 provides a visual indication of supply operational status.

-40V Supply Tolerance

The -40V supply tolerance is -40V ±5% (2.0V).

VOLTAGE SENSE Circuit H

VR5, in the -4.64V REFERENCE (Block **G**), provides a -4.64V reference to compare with each supply output. Should any supply be out of regulation (low output), the corresponding comparator output will go LOW, forcing U2D pin 13 HIGH. This turns Q7 on which pulls HIGH NEGATIVE UP (HNUP) LOW (the logic level on HNUP is: HIGH = +20V, LOW = +.2V).

U2A monitors the -5.2V supply, U2B monitors the -10V supply, and U2C monitors the -40V supply. The input common mode range of U2 includes its negative supply (U2A pin 12, connected to -10V). However, if Vin goes more negative than U2A pin 12, the device will be damaged. In the event of a crowbar (or short to ground) on the -10V supply, U2 pin 12 is pulled up to ground. The -40V supply, however, is still up, and can source sufficient current to damage U2. Clamp diode CR14 and current limit resistor R51 prevent this problem from occuring. U2C pin 8 follows the -10V supply at U2 pin 12 when it is shorted. Diodes CR1, CR2, and CR3 isolate the outputs of U2A, U2B and U2C. This will allow checking each supply independently for low output.

GROUNDS and COMMONS I

This block depicts the critical power and signal ground distribution system implemented on the board. Caution has been used in the distibution of loads, and in isolating critical ground paths from non-critical or high current ground paths.

A56 -15V SUPPLY, CIRCUIT DESCRIPTION

The A56 board contains the -15V REGULATOR and VOLTAGE SENSE circuitry to flag the A52 Positive Regulator if an out of tolerance condition in the supply occurs.

-15V REGULATOR Circuit A

U1 is a monolithic three-terminal adjustable negative regulator. It is designed to maintain a constant -1.25V difference between the OUT terminal and the ADJ terminal.

C2 improves the ripple rejection of U1, and CR1 provides a discharge path for C2 in the event of a short from -15V OUT to ground. C3 is required to compensate for the effective line length in the input circuit due to R1 and R6. R1 and R6 will reduce the power dissipation in U1 during crowbar. CR2 protects against an inadvertant short between -15V OUT and a high current positive supply (CR2 clamps -15V OUT at approximately +0.8V, protecting load curcuits from damage).

-15V CROWBAR/SUPPLY ON INDICATOR Circuit B

When V OUT exceeds approximately 17.8 Volts, VR1 conducts, biasing crowbar SCR Q1 on and shorting the -15V supply to ground. This protects instrument load circuits from an overvoltage condition. Yellow LED DS1 gives a visual indication of the supply status.

-15V Supply Tolerance

The -15V supply tolerance is -15V $\pm$5% (0.75V).

LOW VOLTAGE SENSE Circuit C

When -15V OUT exceeds 12.1V, Q2 turns OFF and HIGH NEGATIVE UP (HNUP) goes HIGH. HNUP is used on the A52 Positive Regulator board to monitor the -15V output and determine if it is within tolerance.

A53 NEGATIVE REGULATOR, TROUBLESHOOTING

WARNING

When connected to ac mains, there are voltages at points inside the instrument that can cause personal injury or even death. Any servicing of this instrument with protective covers removed should be performed only by trained personnel who are aware of the hazard involved.

CAUTION

Do not remove the crowbar and operate the supply without it. This could cause severe damage to the instrument if the supply is faulty and the crowbar has engaged to protect the instrument.

WARNING

If the A19 POWER-ON SAFETY INDICATOR LED is on there are voltages present inside the instrument (the A62 Motherboard, the A35 and A19 Rectifier Assemblies, line filter module/transformer wiring, etc.) that can cause personal injury or even death.

CAUTION

The A53 Assembly contains static sensitive components. Troubleshoot this assembly only at a work station that is equipped with an anti-static surface. Any persons working on this instrument should wear a grounding strap that provides a path to ground of no less than 1 Megohms and no more than 2.5 Megohms. All anti-static safeguards must conform to state and federal safety standards and statutes. When handling a printed circuit board, always hold it by the edges. Never touch the finger contacts.

Operation and troubleshooting of the negative regulators are virtually the same as their positive counterparts.

If more than one supply has failed, refer to the "**POWER SUPPLY**

TROUBLESHOOTING TO ASSEMBLY LEVEL" Flowchart.

-10V REGULATOR Troubleshooting

The -10V supply tolerance is -10V ±5% (0.5V). Make sure the -10V supply (crowbar, etc) is not pulling the -10V supply down. Remove the -5.2V fuse, F1, and check to see if the -10V supply operates properly. If the -10V supply is still not functional, proceed as follows:

SUPPLY/LOAD FAILURE DETERMINATION

Disconnect the instrument from ac mains. After the POWER-ON SAFETY INDICATOR goes out remove the A53 Assembly and place it on an extender board. Apply thin, colored, non-conductive tape to the extender board -10V output pins (use of transparent tape is not recommended because it may be forgotten and left on the extender board, causing unnecessary troubleshooting). Re-install the A53 Assembly and connect ac mains to the instrument. If the power supply now operates properly suspect a short on one of the instrument assemblies that use -10V. Refer to Table 8J-11, Power Supply Destination Chart at the end of the **"POWER SUPPLY - FAN"** functional group, for a list of these assemblies. After removing tape from extender board fingers clean fingers according to the following instructions:

CAUTION

Cleaning P.C. Board fingers by any other method than the one described below may cause serious reliability problems. NEVER clean fingers with any kind of eraser. NEVER use tap water in the cleaning solution described below. Tap water contains chlorine. Chloride contamination from tap water, salt (from skin contact), or any other source may cause serious reliability problems. Always wear a ground strap when handling any internal 8340 component or assembly. Always hold a printed circuit board by the edges.

Printed Circuit Board Finger Cleaning Procedure

Mix one part deionized water with two parts isopropyl alcohol. Apply this solution to a clean, lint free, cloth (HP Part Number 9310-0039 CD3). Rub the fingers vigorously and then dry with a clean part of the cloth.

Refer to the appropriate section below:

- -10V Load Failure
- -10V Power Supply Failure

-10V Load Failure

If the problem is load related repeat the above procedure for safe removal of the A53 Assembly, remove the tape from the extender board -10V output pins, clean the fingers as described above, and reinstall the A53 assembly. It will be necessary to remove each assembly that uses -10V, one at a time, to determine which one is faulty. Likewise remove any cables listed that carry the affected supply. Refer to Table 8J-11, Power Supply Destination Chart at the end of the **"POWER SUPPLY - FAN"** functional group, for a list of these assemblies. Always remove ac mains and wait for the POWER-ON SAFETY INDICATOR to go out before removing or installing any assembly or cable.

-10V Power Supply Failure

If the power supply output does not return to normal after the extender board -10V output pins are taped off, refer to the appropriate section below:

- -10V output voltage approximately -.8V to -1.0V.
- -10V output voltage approximately 0V to +.7V.
- -10V output voltage incorrect. Tolerance is -10V $\pm$5% (0.5V).

-10V output voltage approximately -.8V to -1.0V.

Crowbar circuit verification - If the output voltage is approximately -.8V to -1.0V the crowbar circuit is engaged. Connect the instrument to an auto-transformer set for 0V output. While monitoring the supply output voltage slowly increase the auto-transformer output voltage. If the crowbar fires before the supply output reaches -10V suspect VR1.

Regulator and error amp verification - If the power supply output reaches -10V stop increasing auto-transformer voltage. Check the operation of transistor Q4 and A62Q1. The emitter-base voltage across A62Q1 should be approximately 1.2v. Check for emitter-collector shorts. The emitter-base voltage across Q4 should be .35 to .5 volts, which indicates that the transistor is biased off.

-10V output voltage approximately 0V to +.7V.

Initial checks - Ensure that ac mains voltage is nominal and that the line voltage selector printed circuit board is installed properly in the line filter module, FL1. Make sure the proper fuse value is installed. If the above is correct and the power supply input fuse (F3) is blown, suspect transistor A62Q1.

Measure the -10V RETURN (P1-2) with respect to the -10V UNREG (P1-9). If this voltage is less than approximately -16V, troubleshoot the -10V Rectifier. Refer to the A19 troubleshooting guide.

Regulator verification - Check transistor Q4, and A62Q1 for proper operation. The base-emitter voltage across A62Q1 should be approximately 1.2V. The base-emitter voltage across Q4 should be .35 to .5 volts, which indicates that the transistor is biased off.

Current limit checks - Check for .6V across the emitter-base junction of Q4. This condition indicates that the current foldback circuit is engaged and that it is shutting down pass transistor A62Q1. Measure Q4 emitter to collector. If the voltage is approximately .2V or less, Q4 may be shorted.

Examine the -10V supply for burnt or discolored components. Suspect a shorted capacitor, diode, or crowbar SCR if the above mentioned procedures do not isolate the problem.

-10V output voltage incorrect. Tolerance is -10V $\pm$5% (0.5V).

Ensure that ac mains voltage is nominal and that the line voltage selector printed circuit board is installed with the proper line voltage selected.

Measure the -10V RETURN (P1-2) with respect to the -10V UNREG (P1-9). If the voltage is less than Approximately -16V troubleshoot the -10V Rectifier. Refer to the A19 Troubleshooting Guide.

Measure the output voltage with an HP 1740A or similar Oscilloscope to make sure the supply is not oscillating.

Check the values of divider resistors R8, R9, and R10. Make sure the feedback path to U4 is not open. Check C5 by removing it from the circuit. C5 is likely to cause supply noise or temperature instability if bad (current leakage)..

-40V REGULATOR Troubleshooting

The -40V supply tolerance is -40V $\pm$5% (2.0V). The -40V REGULATOR

circuit is very similar to the -10V REGULATOR circuit. Therefore, troubleshooting techniques are very similar. Refer to the **"-10V REGULATOR Troubleshooting"** section, above. The major difference between the two supplies is that the -10V supply uses a darlington series pass element for supply regulation whereas the -40V supply uses a descrete transistor. When checking for proper A62Q2 operation measure its base-emitter voltage. If this voltage is not approximately .6V to .7V, suspect A62Q2.

-5.2V REGULATOR Troubleshooting

The -5.2V supply tolerance is -5.2V ±5% (0.26V). Determine if the -5.2V supply has failed or is being forced into current limit by a short elsewhere in the instrument. Refer to "SUPPLY/LOAD FAILURE DETERMINATION" in the above -10V troubleshooting section. If the problem is load related, troubleshooting is similar to the -10V "Load Failure" section. If the -5.2V supply is at fault, proceed as follows:

-5.2V Power Supply Failure

If the power supply output does not return to normal after the extender board -5.2V output pins are taped off, refer to the appropriate sections below:

- -5.2V output voltage approximately -.8V to -1.0V.
- -5.2V output voltage approximately 0V.
- -5.2V output voltage incorrect. Tolerance is -5.2V ±5% (0.26V).

-5.2V output voltage approximately -.8V to -1.0V.

Crowbar circuit verification - If the output voltage is approximately -.8V to -1.0V the crowbar circuit is engaged. Connect the instrument to an auto-transformer set for 0V output. While monitoring the supply output voltage slowly increase the auto-transformer output voltage. If the crowbar fires before the supply output reaches -5.2V suspect VR2.

Regulator verification - If the power supply output reaches -5.2V stop increasing auto-transformer voltage. Measure the voltage across pin 1 and the case of U1 (regulator). If the voltage is not approximately 1.25V suspect U1. Measure the voltage from the input and the output of U1. If there is little or no voltage U1 is probably shorted.

-5.2V output voltage approximately 0V.

Initial checks - Ensure that ac mains voltage is nominal and that the line voltage selector printed circuit board is installed properly in the line filter module, FL1. Make sure the proper fuse value is installed.

If the above is correct and the power supply input fuse (F1) is blown, suspect regulator U1.

Measure the -10V REGULATOR output (TP5). If this voltage is incorrect, troubleshoot the -10V power supply. Refer to the **"-10V REGULATOR Troubleshooting"** section, above.

Regulator verification - Measure across pin 1 and the case of U1. If the voltage is not approximately 1.25V suspect U1.

Examine the -5.2V supply for burnt or discolored components. Suspect a shorted capacitor, diode, or crowbar SCR if the above mentioned procedures to not isolate the problem.

-5.2V output voltage incorrect. Tolerance is -5.2V ±5% (0.26V).

Ensure that ac mains voltage is nominal and that the line voltage selector printed circuit board is installed with the proper line voltage selected.

Measure the -10V REGULATOR output (TP5). If the voltage is incorrect, troubleshoot the -10V power supply. Refer to the **"-10V REGULATOR Troubleshooting"** section, above.

Measure the -5.2V output voltage with an HP 1740A or similar Oscilloscope to make sure the supply is not oscillating. If the output is approximately 1.25V C14 is probably shorted.

A56 -15V SUPPLY, TROUBLESHOOTING

CAUTION

The A56 Assembly contains static sensitive components. Troubleshoot this assembly only at a work station that is equipped with an anti-static surface. Any persons working on this instrument should wear a grounding strap that provides a path to ground of no less than 1 Megohms and no more than 2.5 Megohms. All anti-static safeguards must conform to state and federal safety standards and

statutes. When handling a printed circuit board, always hold it by the edges. Never touch the finger contacts.

The -15V supply is very similar to the -5.2V supply. Therefore, troubleshooting techniques are also similar. Refer to the **"-5.2V REGULATOR Troubleshooting"** section, above. The -15V supply tolerance is -15V ±5% (0.75V).

A53/A56 REPAIR PROCEDURE

CAUTION

The thermal connection between the pass transistors/voltage regulators and the main heat sink is the dominant factor in their long term reliability. Be sure to properly apply thermal compound (HP Part Number 6040-0454 CD0) when installing or replacing these parts.

CAUTION

Use only oil based thermal compound. The use of silicone based thermal compound may cause serious reliability problems. Silicone based oil migrates to pass element sockets, switch contacts, or printed circuit board edge connectors. The compound then tends to raise contact resistance or electrically isolate the contacts. Silicone based thermal compounds disperse into the air and deposit themselves anywhere in the instrument. Applying this material to a warm component (e.g. a heat sink or pass element) increases the rate of dispersion.

Thermal Compound Application

When installing or replacing a pass transistor or voltage regulator make sure thermal compound is applied as described below:

Apply a thin coating of thermal compound (HP Part Number 6040-0454 CD0) to both sides of the insulating washer. The coating should be just thick enough to provide a thin but continuous layer of compound from component-to-washer and washer-to-heat sink. An excessive amount of heat sink compound impairs its ability to transfer heat. The pass element mounting screws should be tightened with seven inch-pounds of force. Tightening with less force diminishes the heat transfer capability of the thermal compound. Tightening with greater force may damage the mounting hardware.

Table 8J-4. A53 Negative Regulator, Regulated Supply Limits

Power Supply	DMM Probe	Ground	Limits
-40V	A53TP4	A53P1-14	-42.00V to -38.00V
-10V	A53TP5	A53P1-14	-10.5V to -9.5V
-5.2V	A53TP3	A53P1-14	-5.46V to -4.94V

Table 8J-5. A56 −15V Supply, Regulated Supply Limit

Power Supply	DMM Probe	Ground	Limit
-15V	A56TP2	A56P1-5	-15.75V to -14.25V

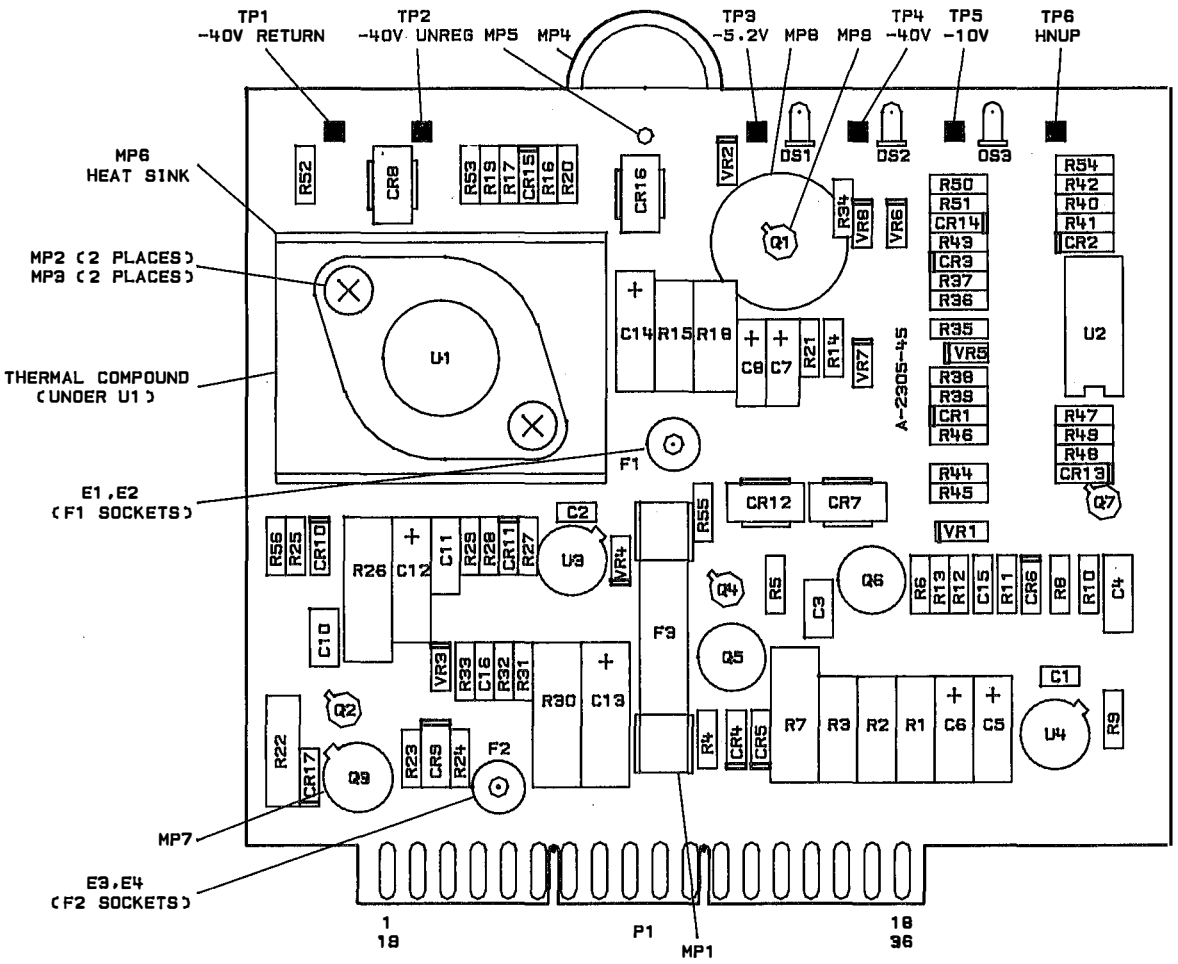


Figure 8J-11. A53 Negative Regulator, Component Location Diagram

A53 Negative Regulator P1 Pin I/O

A53

Pin	Mnemonic	Levels	Source	Destination
1 19	Q2E Q2E		A62Q2-EMITTER A62Q2-EMITTER	E E
2 20	−10V RETURN −10V RETURN	+6.4V AT 13.3 GHZ +6.4V AT 13.3 GHZ	A62Q1-COLLECTOR A62Q1-COLLECTOR	XA19P1-7, 8, 19, 20 A XA19P1-7, 8, 19, 20 A
3 21	−40V RETURN Q2B	12.7 AT 13.3 GHZ	A62Q2-COLLECTOR A62Q2-BASE	*E E
4 22	Q1B −40V RETURN	12.7V AT 13.3 GHZ	A62Q1-BASE A62Q2-COLLECTOR	A *E
5 23	−40V SENSE (+) −40V SENSE (−)	0V −40V	D E	*E *
6 24	−40V UNREG −40V UNREG	−40V −40V	XA35P1-6, 24 XA35P1-6, 24	*E *E
7 25	Q1E Q1E		A62Q1-EMITTER A62Q1-EMITTER	A A
8 26	Q1E Q1E		A62Q1-EMITTER A62Q1-EMITTER	A A
9 27	−10V UNREG −10V UNREG	−10V −10V	XA19P1-11, 12, 23, 24 XA19P1-11, 12, 23, 24	A A
10 28	−10V UNREG −10V UNREG	−10V −10V	XA19P1-11, 12, 23, 24 XA19P1-11, 12, 23, 24	A A
11 29	−40V +20V	−40V +20V	E F XA52P1-16, 40	*H *A E H
12 30	−10V −40V	−10V −40V	A B E F	*C G H *H
13 31	−10V −10V	−10V −10V	A B A B	*C G H *C G H
14 32	GND −10V	0V −10V	A62 STAR GND A B	*D *C G H
15 33	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*D *D
16 34	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*D *D
17 35	HNUP GND	TTL (HIGH TRUE) 0V	*H A62 STAR GND	* *D
18 36	−5.2V −5.2V	−5.2V −5.2V	C D C D	*H *H

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

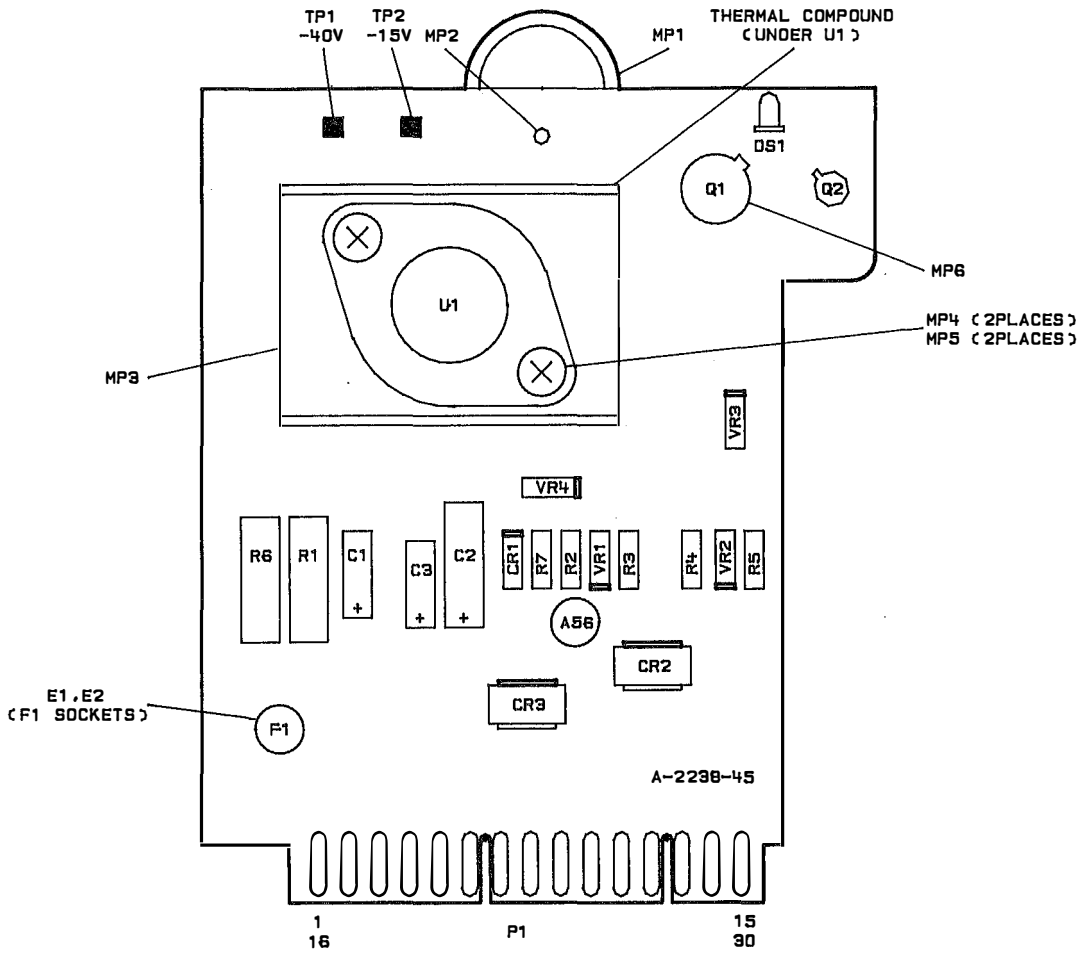


Figure 8J-12. A56 −15V Regulator, Component Location Diagram

A56 −15V Regulator P1 Pin I/O

A56

Pin	Mnemonic	Levels	Source	Destination
1 16	HNUP HNUP	TTL (HIGH TRUE) TTL (HIGH TRUE)	*C *C	* *
2 17				
3 18	−40V/−40V SENSE(−) −40V/−40V SENSE(−)	−40V −40V	XA53P1-11, 30/XA53P1-23 XA53P1-11, 30/XA53P1-23	*A *A
4 19	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*NOT USED *NOT USED
5 20	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*D *D
6 21				
7 22				
8 23				
9 24				
10 25				
11 26				
12 27				
13 28				
14 29				
14 30	−15V −15V	−15V −15V	A B A B	*C *C

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterick (*) denotes multiple sources or destinations; refer to the A62 Motherboard Wiring List for a complete representation of signal sources and destinations.

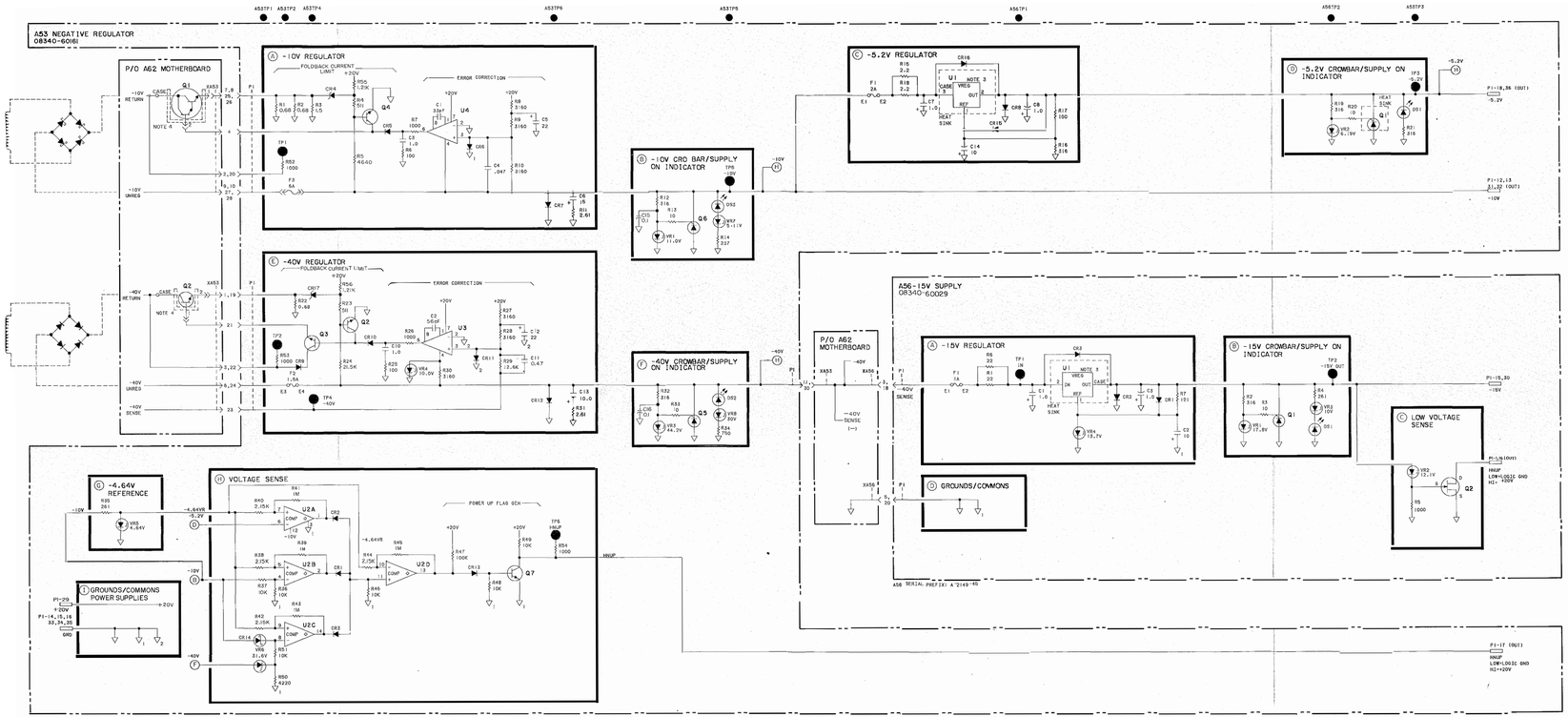


Figure 8-13. A53 Negative Regulator and A56 −15V Regulator, Schematic Diagram

Table 8J-6. Power Supply Destination Chart

Assembly	Power Supply	Destination Assemblies/Connectors
A19	+20V UNREG	A35, A52
	−10V UNREG	A53
A35	−40V UNREG	A53
	+5V UNREG	A52, A62J1,A62J31
	+22V	A61, A62J1, A62J3
A52	+20V	A21 through A28, A34, A36, A38, A40 through A43, A53 through A55, A57 through A61
	+5.2V	A21 through A28, A34, A36, A37, A39 through A43, A54, A55, A57 through A60, A62J2, A62J19
	+12V	A23, A57 through A61, A62J1
A53	−10V	A21 through A28, A34, A36, A38 through A43, A54, A55, A57 through A61, A62J2, A62J18, A62J19
	−40V	A22, A23, A28, A34, A40, A54, A55, A56, A62J2, A62J19
	−5.2V	A23, A27, A34, A52, A57 through A61, A62J1, A62J2, A62J19
A56	−15V	A27, A28, A54, A57 through A61

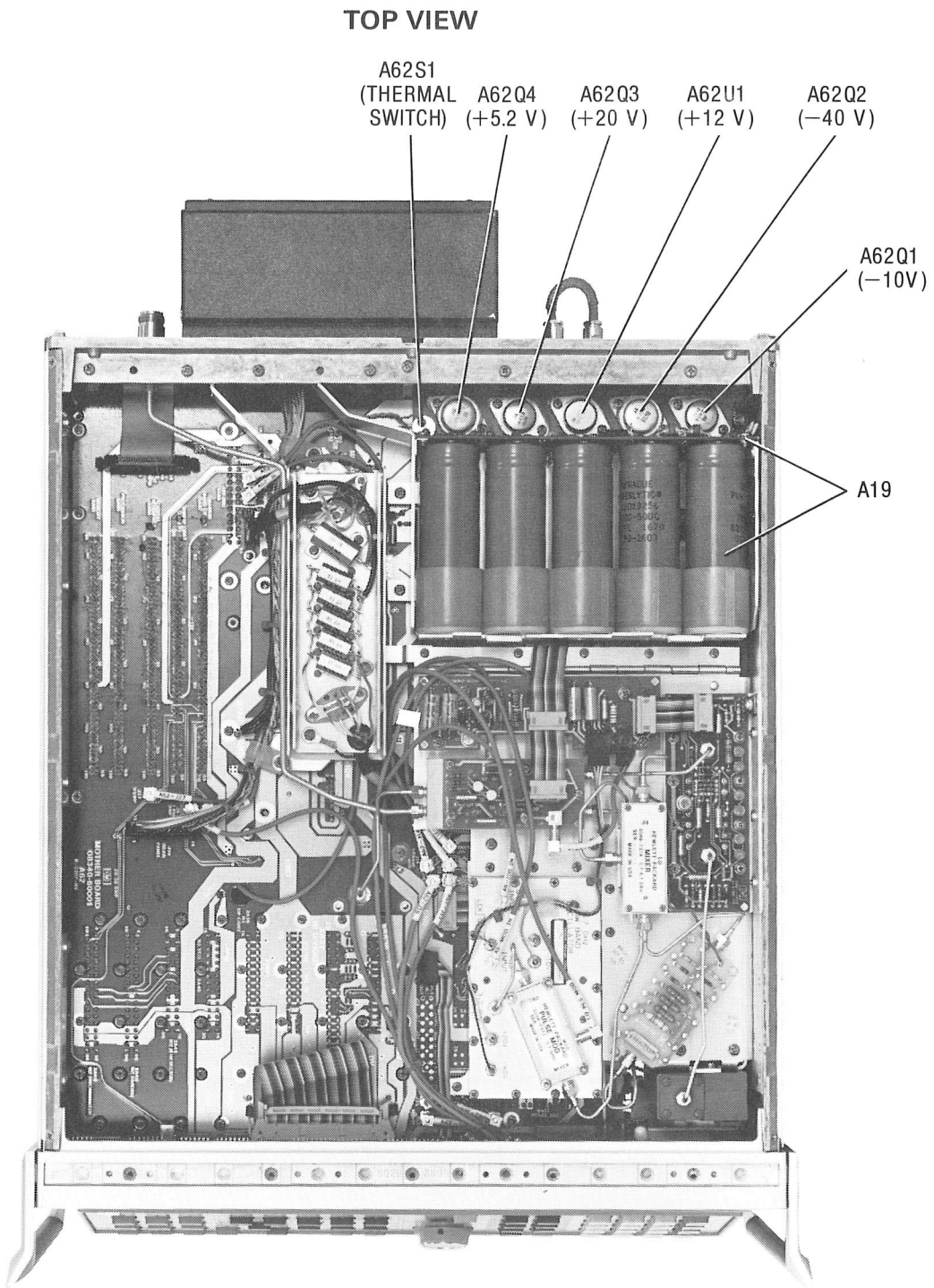


Figure 8J-14. Power Supply Major Assemblies Location Diagram (1 of 2)

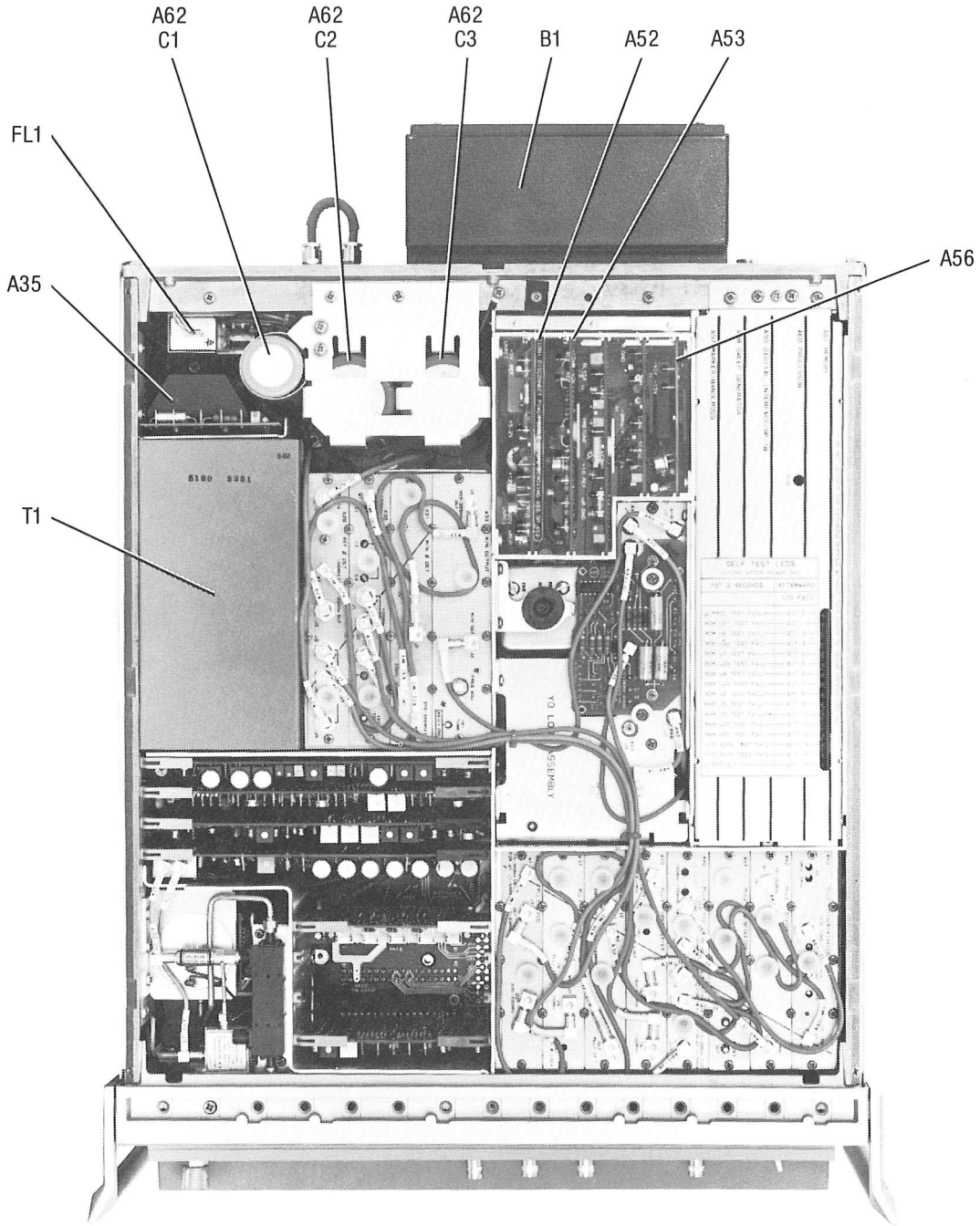
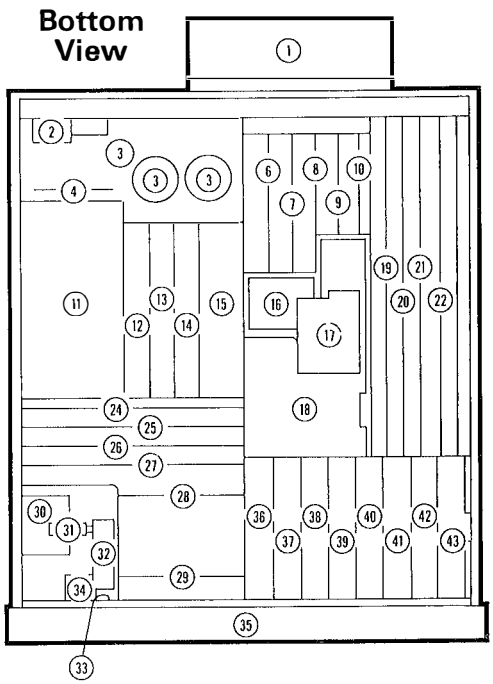
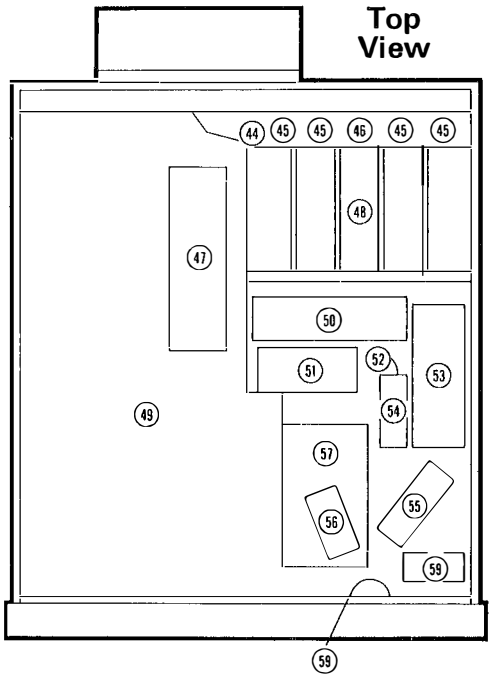


Figure 8J-14. Power Supply Major Assemblies Location Diagram (2 of 2)

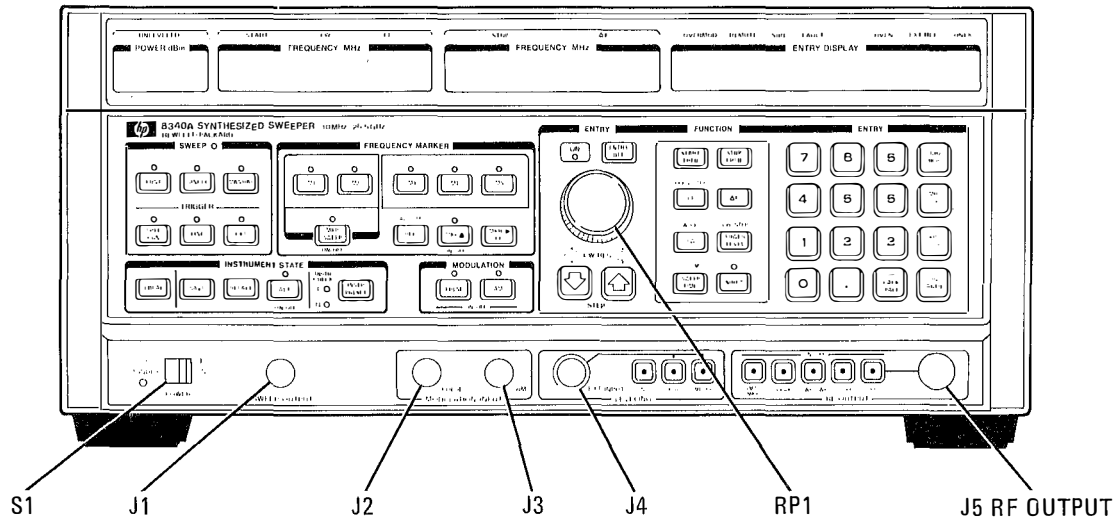
REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 3					Volume 4		
			Ref.-M/N Loops	20-30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	33					●			
A2	Display Driver	33					●			
A3	Display Processor	33					●			
A4	Not Assigned	-								
A5	Keyboard	35					●			
A6	Keyboard Interface	35					●			
A7	Lower Keyboard	35					●			
A8	3.7 GHz Oscillator	57						●		
A9	Band 0 Pulse Modulator	56						●		
A10	Directional Coupler	32						●		
A11	Band 1-4 Detector	31						●		
A12	Band 0 Splitter/Detector	34						●		
A13	SYTM (Switched YIG Tuned Multiplier)	30						●		
A14	Band 1-4 Power Amplifier	53						●		
A15	Band 0 Low Pass Filter	52						●		
A16	Band 1-4 Modulator/Splitter	51						●		
A17	Band 0 Mixer	54						●		
A18	Band 0 Power Amplifier	55						●		
		60						●		
A19	Capacitor Assembly	48								●
A20	RF Section Filter	50						●		
A21	Pulse Modulator Driver	29						●		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						●		
A25	ALC Detector	27						●		
A26	Linear Modulator	26						●		
A27	Level Control	25						●		
A28	SYTM Driver	24						●		
A29	Reference Phase Detector	12	●							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	●							
A31	M/N Phase Detector	14	●							
A32	M/N VCO (Voltage Controlled Osc.)	15	●							
A33	M/N Output	15	●							
A34	Reference-M/N Motherboard	5	●							
A35	Rectifier	4								●
A36	PLL1 VCO (Voltage Controlled Osc.)	36		●						
A37	PLL1 Divider	37		●						
A38	PLL1 IF	38		●						
A39	PLL3 Upconverter	39		●						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		●						
A41	PLL2 Phase Detector	41		●						
A42	PLL2 Divider	42		●						
A43	PLL2 Discriminator	43		●						
A44	YIG Oscillator (YO)	18			●					
A45	Directional Coupler	18			●					
A46	7 GHz Low Pass Filter	18			●					
A47	Sense Resistor Assembly (YO circuit)	47			●					
	(SYTM circuit)	47						●		
A48	YO Loop Sampler	18			●					
A49	YO Loop Phase/Detector	18			●					
A50	YO Loop Interconnect	17			●					
A51	Reference Oscillator	16	●							
A52	Positive Regulator	6								●
A53	Negative Regulator	7								●
A54	YO Pretune/Delay Compensation	8			●					
A55	YO Driver	9			●					
A56	−15V Regulator	10								●
A57	Marker/Bandcross	19					●			
A58	Sweep Generator	20			●					
A59	Digital Interface	21					●			
A60	Processor	22					●			
A61	Not Assigned	23					●			
A62	Motherboard	49				●				
A63	90 dB RF Attenuator	59						●		
AT1	Peripheral Mode Isolator	58						●		
AT2	15 dB Attenuator	18			●					
B1	Fan Assembly	1								●
A62C1-3	Power Supply Filter Capacitors	3								●
FL1	AC Line Module	2								●
A62Q1-4	Power Supply Regulating Transistors	45								●
A62S1	Power Supply Thermal Switch	44								●
T1	Power Supply Transformer	11								●
A62U1	Power Supply Regulator	46								●

FRONT PANEL



REAR PANEL

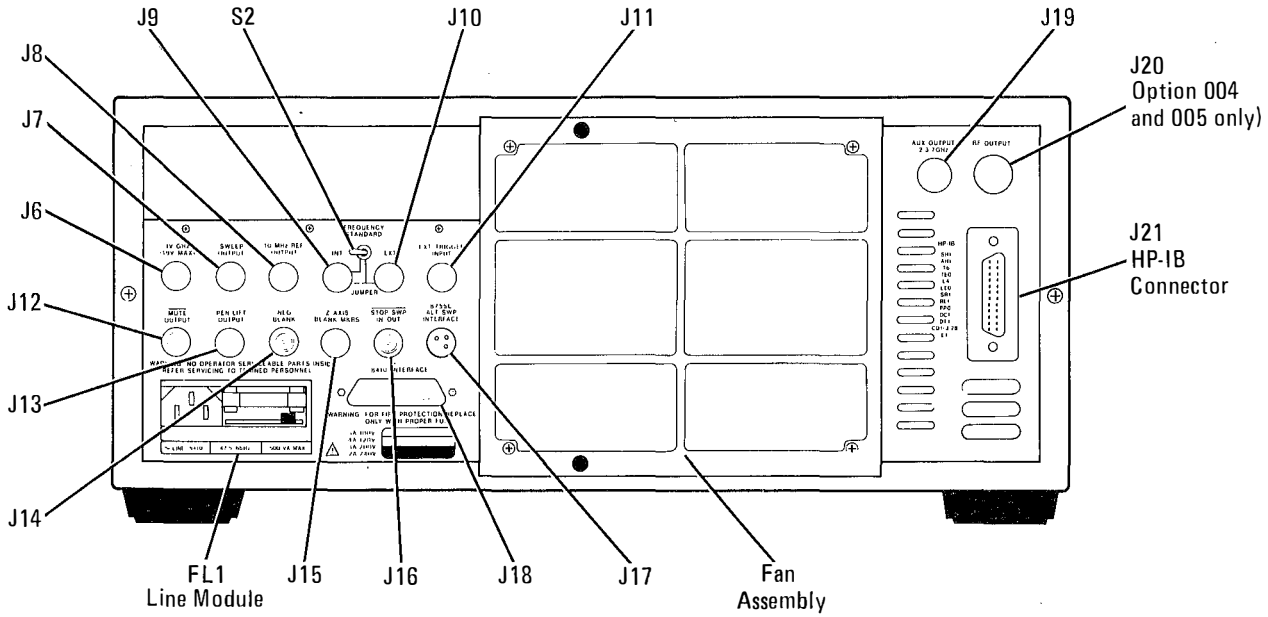


Figure 8K-1. Front and Rear Panels

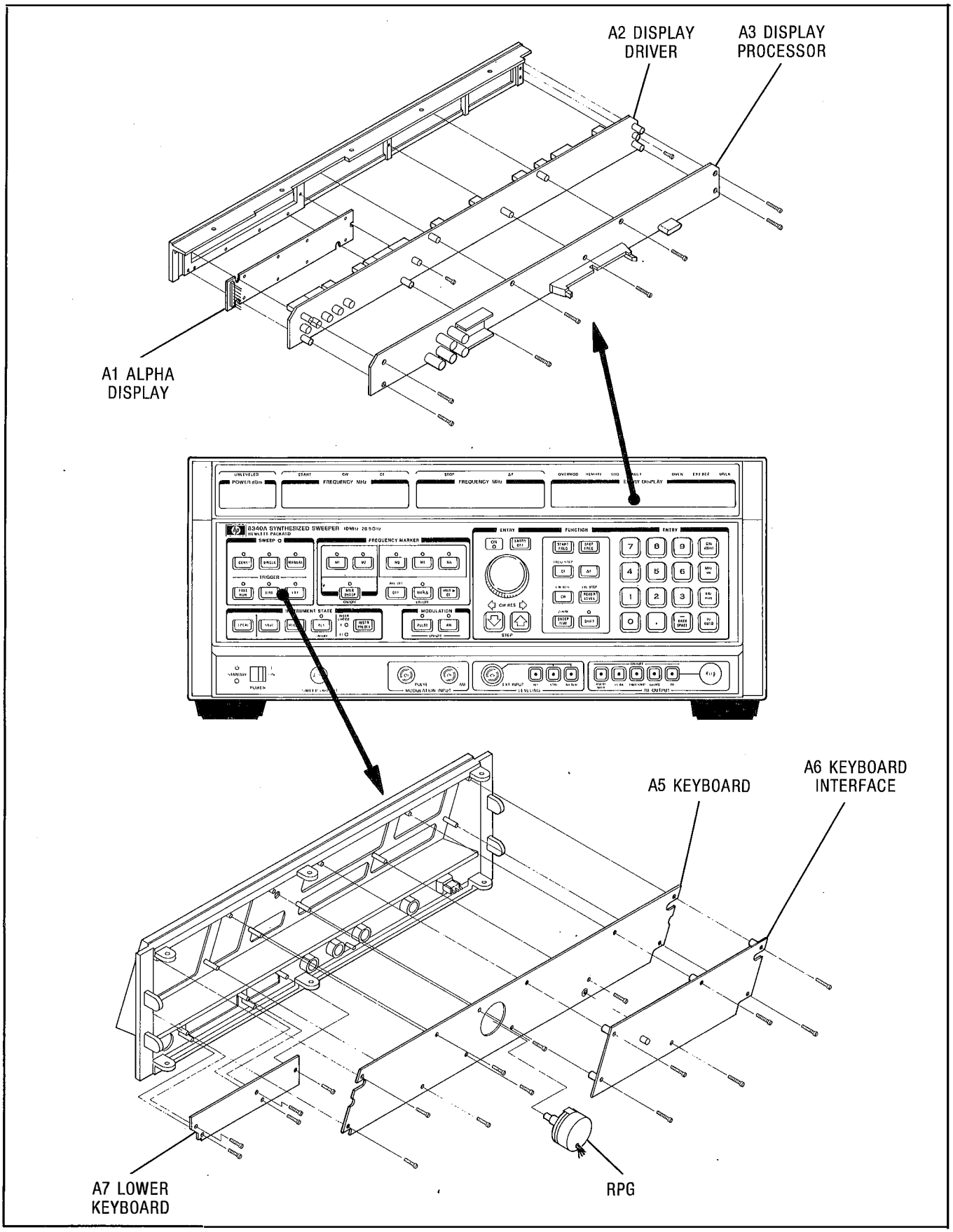


Figure 8K-2. Front Panel Assemblies

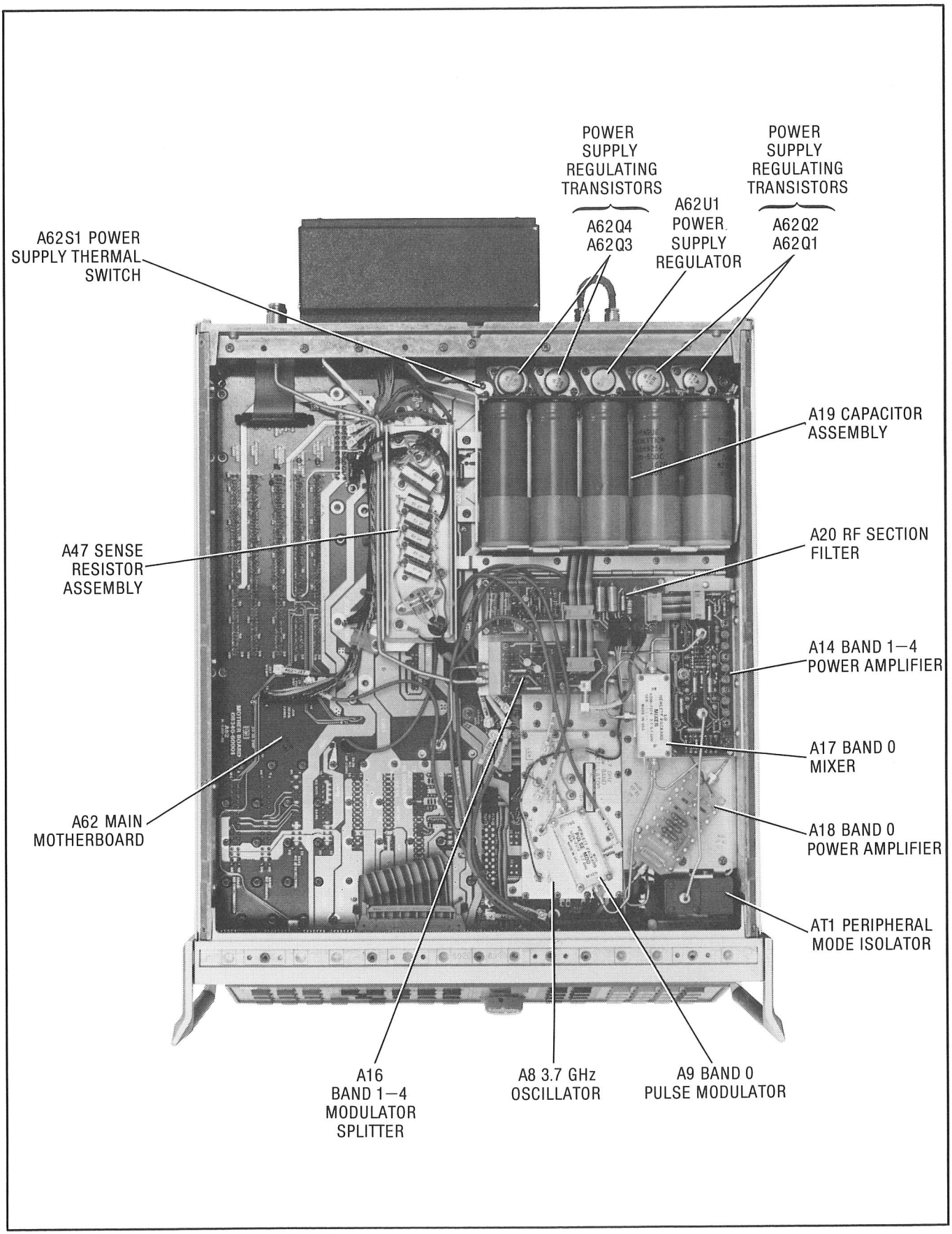


Figure 8K-3. 8340A - Top View (1 of 3)

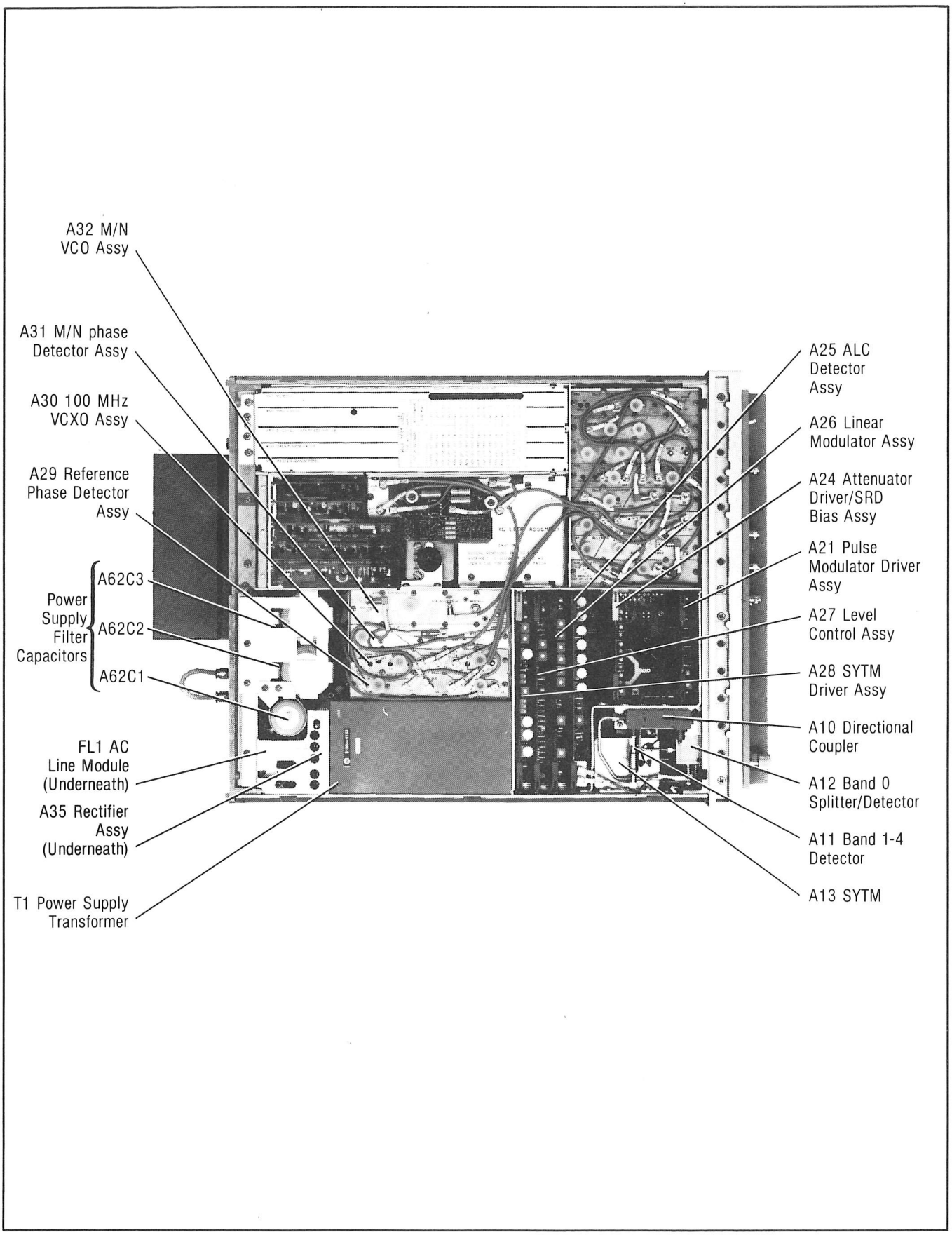


Figure 8K-3. 8340A - Bottom View (2 of 3)

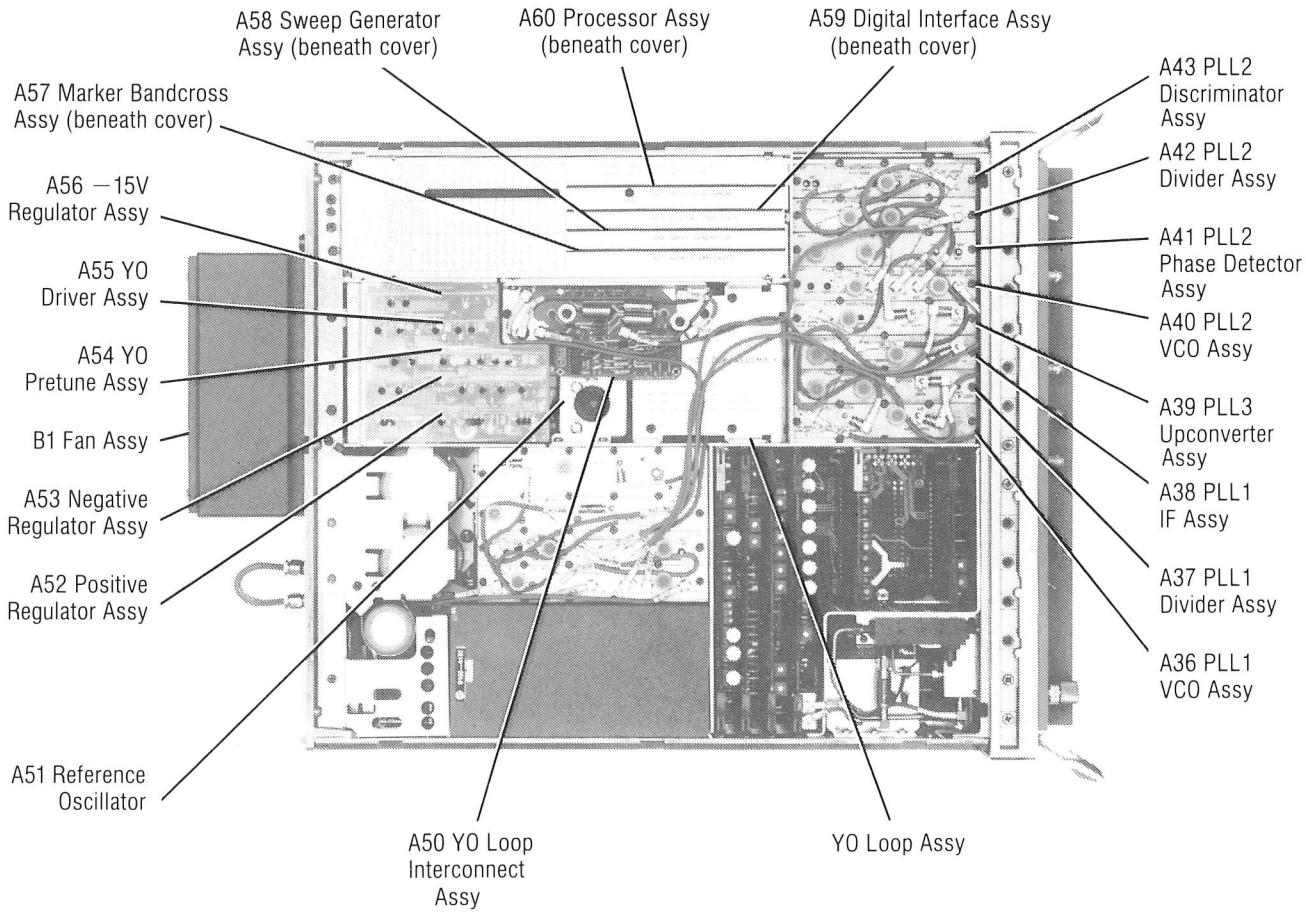
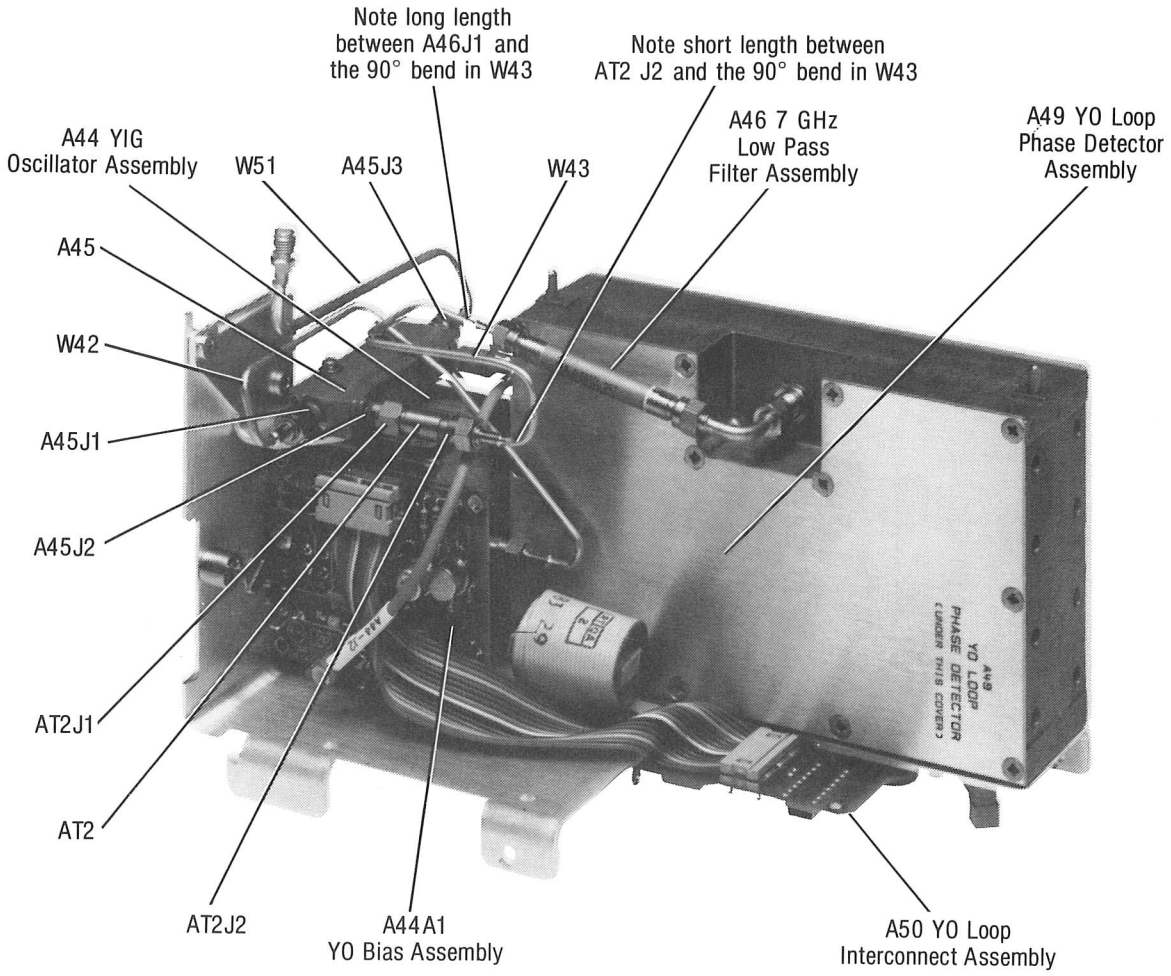


Figure 8K-3. 8340A - Bottom View (3 of 3)



CAUTION: W51 Must be disengaged from W3 before removing the YO Loop from the instrument or damage to these cables will result. Refer to Figure 8I-8, View C, in the RF Section (Volume 4).

Figure 8K-4. YO Loop Assembly (1 of 3)

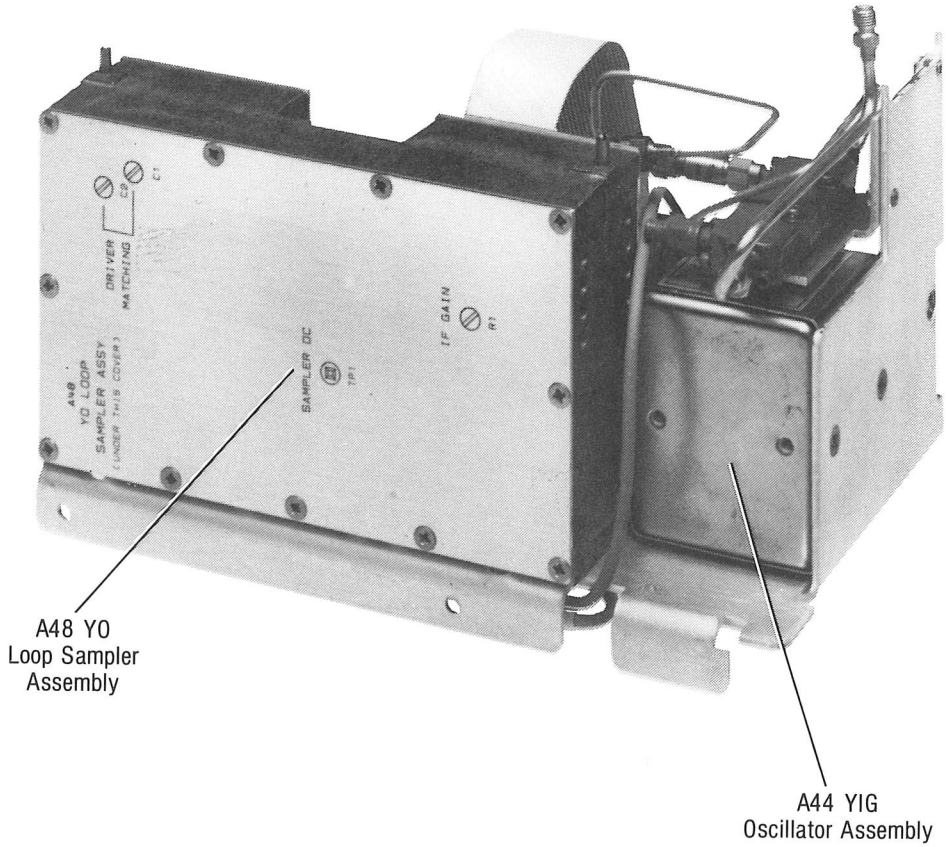


Figure 8K-4. YO Loop Assembly (2 of 3)

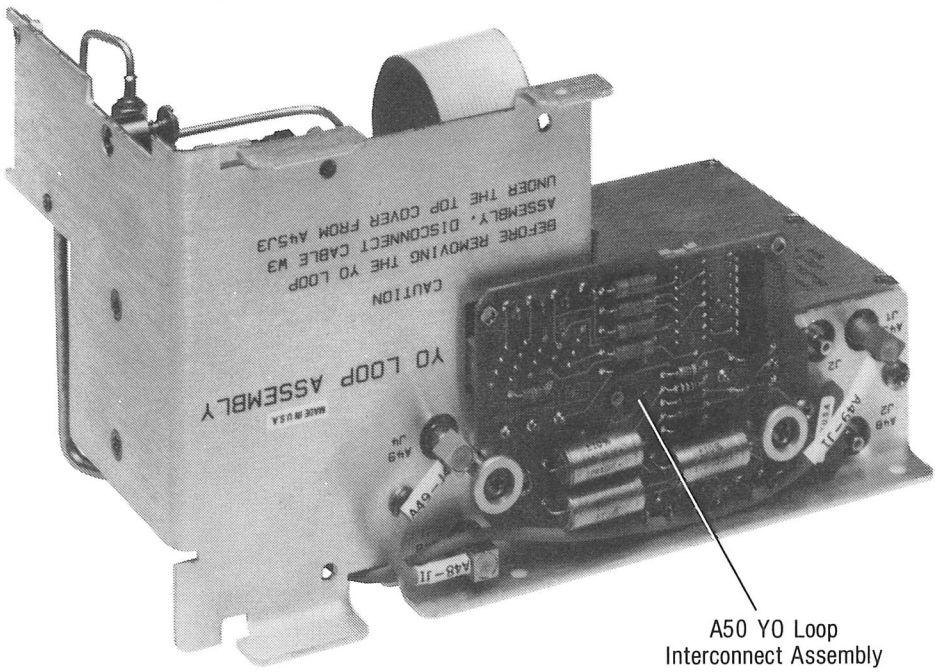


Figure 8K-4. YO Loop Assembly (3 of 3)

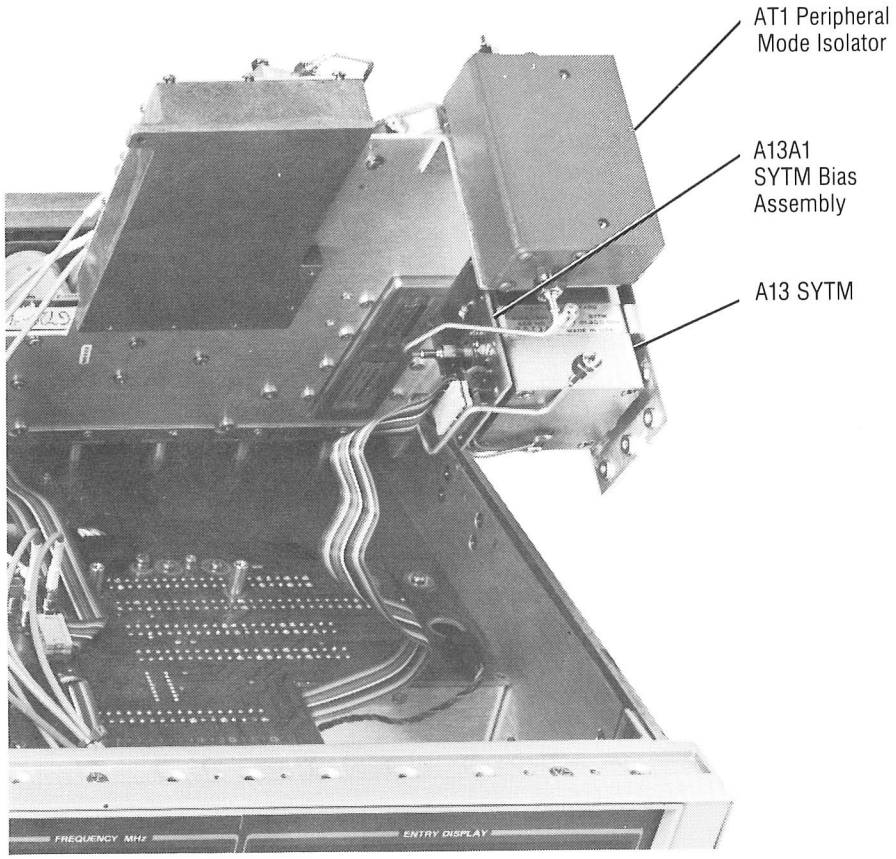


Figure 8K-5. RF Section Swing Out